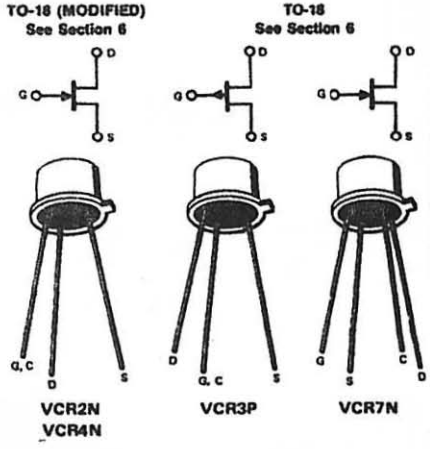
voltage-controlled resistor FETs *designed for . . .*

Siliconix

Performance Curves
NCB, NPA, NT, PSB
See Section 4

- **Small Signal Attenuators**
- **Filters**
- **Amplifier Gain Control**
- **Oscillator Amplitude Control**



ABSOLUTE MAXIMUM RATING (25°C)

Gate-Drain or Gate-Source Voltage . . . . . 15 V
Gate Current . . . . . 10 mA
Total Device Dissipation at T_A = 25°C
(Derate at 2.0 mW/°C to 175°C) . . . . . 300 mW
Storage Temperature Range . . . . . −55 to +175°C

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

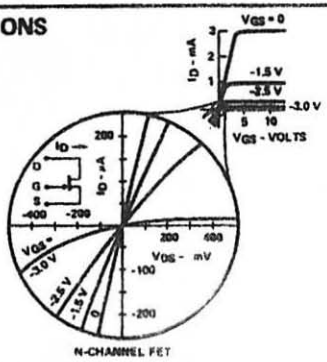
N-Channel VCR FETs

		Characteristic		VCR2N Min	VCR2N Max	VCR4N Min	VCR4N Max	VCR7N Min	VCR7N Max	Unit	Test Conditions	
1	STATIC	I_{GSS}	Gate Reverse Current		-5		-0.2		-0.1	nA	V_{GS} = -15 V, V_{DS} = 0	
2	STATIC	BV_{GSS}	Gate-Source Breakdown Voltage	-15		-15		-15		V	I_G = -1 μA, V_{DS} = 0	
3	STATIC	$V_{GS(off)}$	Gate-Source Cutoff Voltage	1.0	3.5	-3.5	-7	-2.5	-5	V	I_D = 1 μA, V_{DS} = 10 V	
4	STATIC	$r_{ds(on)}$	Drain Source ON Resistance	20	60	200	600	4,000	8,000	Ω	V_{GS} = 0, I_D = 0	f = 1 kHz
5	DY	C_{dgo}	Drain-Gate Capacitance		7.5		3		1.5	pF	V_{GD} = -10 V, I_S = 0	f = 1 MHz
6	DY	C_{sgo}	Source-Gate Capacitance		7.5		3		1.5	pF	V_{GS} = -10 V, I_D = 0	f = 1 MHz
				NCB		NPA		NT				

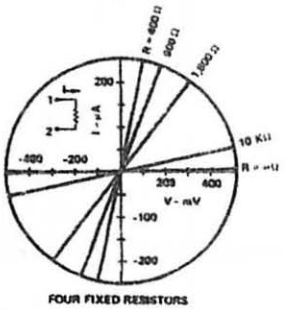
P-Channel VCR FETs

				VCR3P				
1	STATIC	I_{GSS}	Gate Reverse Current		20	nA	V_{GS} = 15 V, V_{DS} = 0	
2	STATIC	BV_{GSS}	Gate-Source Breakdown Voltage	15		V	I_G = 1 μA, V_{DS} = 0	
3	STATIC	$V_{GS(off)}$	Gate-Source Cutoff Voltage	1.0	5	V	I_D = -1 μA, V_{DS} = -10 V	
4	STATIC	$r_{ds(on)}$	Drain-Source ON Resistance	70	200	Ω	V_{GS} = 0, I_D = 0	f = 1 kHz
5	DY	C_{dgo}	Drain-Gate Capacitance		25	pF	V_{GD} = 10 V, I_S = 0	f = 1 MHz
6	DY	C_{sgo}	Source-Gate Capacitance		15	pF	V_{GS} = 10 V, I_D = 0	f = 1 MHz
				PSA/PSB				

APPLICATIONS



N-Channel JFET Output Characteristic
Enlarged Around $V_{DS} \approx 0$
Figure 1



V-I Characteristic of Four Fixed Resistors
Figure 2

The VCR FET has an a-c drain-source resistance, evaluated around $V_{DS} = 0$, that is controlled by d-c bias voltage V_{GS} applied to the high-impedance gate terminal. Minimum r_{ds} occurs when $V_{GS} = 0$ and, as V_{GS} approaches the pinch-off voltage, r_{ds} rapidly increases. Comparing Fig. 1 and 2, for $V_{DS} < \pm 0.1$ volt and V_{GS} = constant, the VCR FET has a bilateral characteristic with no offset voltage, just like a fixed resistor. However, when $V_{DS} > \pm 0.1$ volts, the VCR FET characteristic has noticeable curvature.

This series of junction FETs is intended for applications where the drain-source voltage is a low-level a-c signal with no d-c component. Thus the FET operating point will swing symmetrically around $V_{DS} = 0$. In the first quadrant, signal distortion depends on what extent the FET output characteristic deviates from a straight line or linear relation. Besides the linearity problem in the third quadrant, when V_{GS} is near zero and $v_{ds} > 0.5$ volt rms, the gate-channel junction will become forward biased and cause additional curvature in the characteristic. Also, whenever the gate becomes forward biased due to any combination of V_{GS} and v_{ds}, it ceases to be a high-impedance control terminal for the VCR.

Fig. 3 presents a normalized plot of r_{DS} versus normalized V_{GS} where $V_{GS(off)}$ is defined as that value of V_{GS} at $I_D/I_{DSS} = 0.001$. The dynamic range of r_{DS} is shown as greater than 100:1. For best control of r_{DS} the normalized V_{GS} should lie between 0 and 0.8 $V_{GS(off)}$ because as V_{GS} approaches $V_{GS(off)}$, r_{DS} increases very rapidly so that r_{ds} control becomes very critical and unit-to-unit matching is almost impossible. In Fig. 4, $r_{ds(on)}$ (drain-source resistance at $V_{DS} = V_{GS} = 0$) varies as an inverse function of $V_{GS(off)}$. In Fig. 5 r_{ds} has a typical 0.7%/°C temperature coefficient for P-channels which decreases as V_{GS} approaches the zero t.c. point. N-channel devices have a typical 0.3%/°C t.c. Specific bias voltage to set operation at the zero t.c. point varies, as does $V_{GS(off)}$, from device to device.*

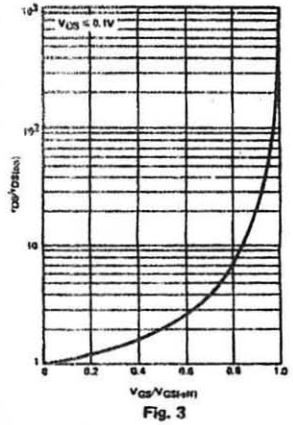


Fig. 3

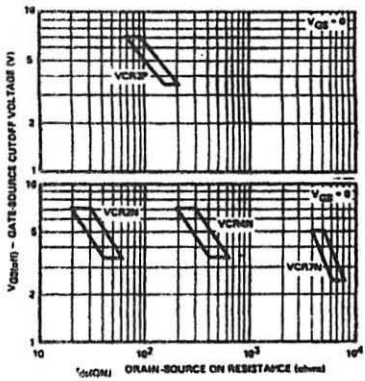


Fig. 4

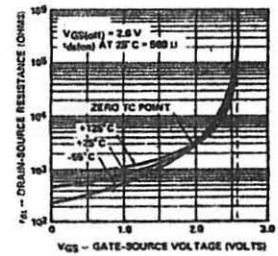


Fig. 5

For further information on using FETs as voltage-variable resistors, consult Siliconix Application Note AN73-1.

* L. Evans; "Biasing FETs for Zero DC Drift"; Electro Technology, August 1964.

FETs As Voltage-Controlled Resistors

INTRODUCTION

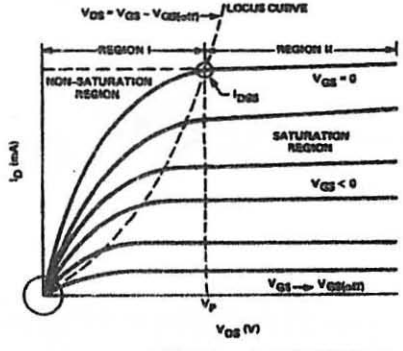
The Nature of VCRs

A voltage-controlled resistor (VCR) may be defined as a three-terminal variable resistor where the resistance value between two of the terminals is controlled by a voltage potential applied to the third.

A junction field-effect transistor (JFET) may be defined as a field-controlled majority carrier device where the conductance in the channel between the source and the drain is modulated by a transverse electric field. The field is controlled by a combination of gate-source bias voltage, V_{GS}, and the net drain-source voltage, V_{DS}.

Under certain operating conditions, the resistance of the drain-source channel is a function of the gate-source voltage alone and the JFET will behave as an almost pure ohmic resistor.(1) Maximum drain-source current, I_{DSS}, and minimum resistance, $r_{DS(on)}$, will exist when the gate-source voltage is equal to ze.o volts ($V_{GS}=0$). If the gate voltage is increased (negatively for N-Channel JFETs and positively for P-Channel) the resistance will also increase. When the drain current is reduced to a point where the FET is no longer conductive, the maximum resistance is reached. The voltage at this point is referred to as the pinchoff or cutoff voltage and is symbolized by $V_{GS} = V_{GS(off)}$. Thus the device functions as a voltage-controlled resistor.

Figure 1 details typical operating characteristics of an N-Channel JFET. Most amplification or switching operations of FETs occur in the constant-current (saturated) region, shown as Region II. A close inspection of Region I (the unsaturated or pre-pinchoff area) reveals that the effective slope indicative of conductance across the channel from drain to source is different for each value of gate-source bias voltage.(2) The slope is relatively constant over a range of applied drain voltages, so long as the gate voltage is also constant and the drain voltage is low.



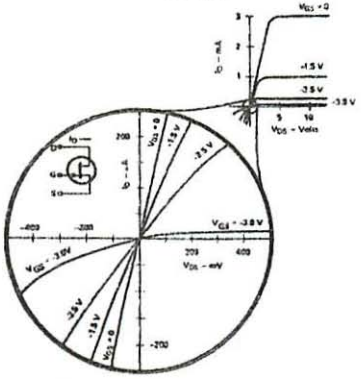
Typical N-Channel JFET Operating Characteristics
Figure 1

7

Resistance Properties of FETs

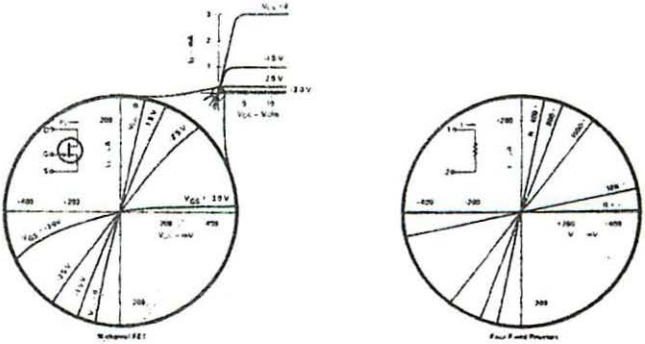
The unique resistance-controlling properties of FETs can be deduced from Figure 2, which is an expanded-scale plot of the encircled area in the lower left-hand corner of Figure 1. The output characteristics all pass through the origin, near which they become almost straight lines so that the incremental value of channel resistance, r_{ds}, is essentially the same as that of d.c. resistance, r_{DS}, and is a function of V_{GS}.(3)

Figure 2 shows extension of the operating characteristics into the third quadrant for a typical N-Channel JFET. While such devices are normally operated with a positive drain-source voltage, small negative values of V_{DS} are possible. This is because the gate-channel PN junction must be slightly forward-biased before any significant amount of gate current flows. The slope of the V_{GS} bias line is equal to $\Delta I_D/\Delta V_{DS} = 1/r_{DS}$. This value is controlled by the amount of voltage applied to the gate. Minimum r_{DS}, usually expressed as $r_{DS(on)}$, occurs at $V_{GS} = 0$ and is dictated by the geometry of the FET. A device with a channel of small cross-sectional area will exhibit a high $r_{DS(on)}$ and a low I_{DSS}. Thus a FET with high I_{DSS} should be chosen where design requirements indicate the need for a low $r_{DS(on)}$.



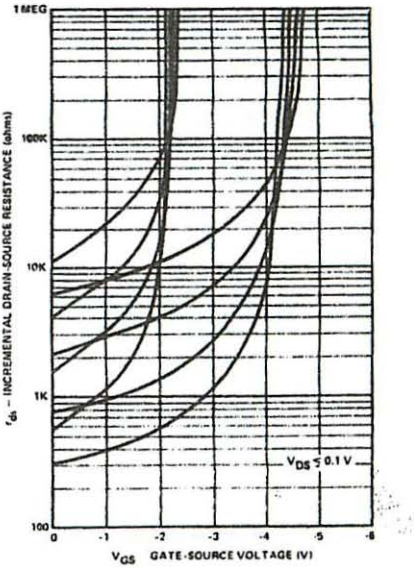
N-Channel JFET Output Characteristic Enlarged Around $V_{DS} = 0$
Figure 2

Figure 3 extends the r_{ds} characteristics of a FET to a comparison with the performance of 4 fixed resistors. Note the pronounced similarity between the two types of devices.



Comparison of FET and Resistor Characteristics
Figure 3

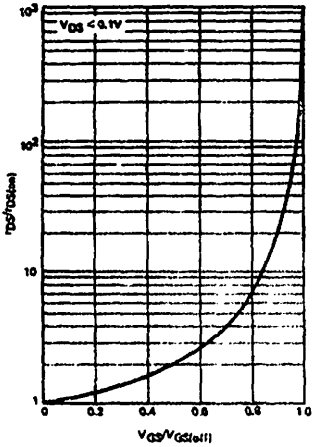
Typical r_{DS} curves for several Siliconix N-channel JFETs are plotted in Figure 4.(4) The graphs are useful in estimating r_{DS} values at any given value of V_{GS}. All quantities given in Figure 4 are for typical units, so some variation should be expected for the full range of production devices. It is therefor deisrable to convert Figure 4 to a normalized plot. This



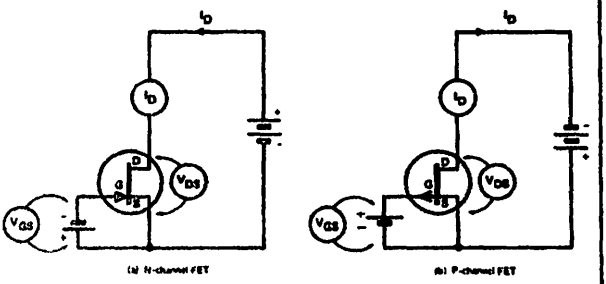
Incremental Drain-Source Resistance for Typical N-Channel FETs
Figure 4

has been done in Figure 5. The resistance is normalized to its specific value at $V_{GS} = 0$ V. The dynamic range of r_{DS} is shown as greater than 100:1, although for best control of r_{DS} a range of 10:1 is normally used.

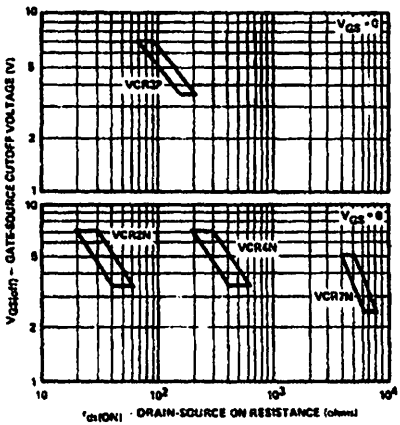
Siliconix offers a family of FETs specifically intended for use as voltage-controlled resistors. The devices are available in both N-Channel and P-Channel configurations (Figures 6A and 6B) and have $r_{DS(on)}$ values ranging from 20 Ω to 4,000 Ω (Figure 7).



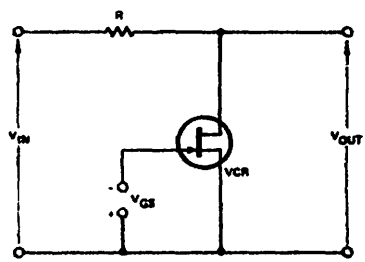
Normalized r_{ds} Data
Figure 5



Circuit Arrangement for Both an N and P Channel FET
Figure 6



$r_{ds(on)}$ (Drain-Source Resistance at $V_{DS} = V_{GS} = 0$)
Varies as an Inverse Function of $V_{GS(off)}$
Figure 7



Simple Attenuator Circuit
Figure 8

Applications for VCRs

The FET is ideal for use as a voltage-controlled resistor in applications requiring high reliability, minimum component size, and circuit simplicity. The FET VCR will conveniently replace numerous elements of conventional resistance control systems, such as servomotors, potentiometers, idler pulleys, and associated linkage. FET power consumption is minimal, packages are very small, and cost comparisons with conventional control schemes are most favorable.

A simple application of a FET VCR is shown in Figure 8, the circuit for a voltage divider attenuator.(5)

The output voltage is

$$v_{OUT} = \frac{V_{in}\, r_{DS}}{R + r_{DS}} \qquad (1)$$

It is assumed that the output voltage is not so large as to push the VCR out of the linear resistance region, and that the r_{DS} is not shunted by the load.

The lowest value which v_{OUT} can assume is

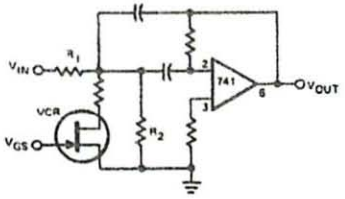
$$v_{OUT(min)} = \frac{V_{in}\, r_{DS(on)}}{R + r_{DS(on)}} \qquad (2)$$

The highest value is

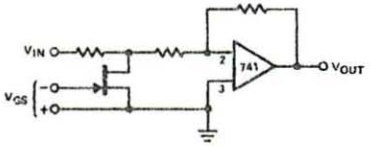
$$V_{OUT(max)} = V_{in} \qquad (3)$$

since r_{DS} can be extremeley large.

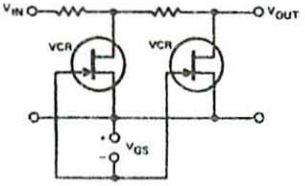
A number of other FET VCR applications are shown in Figures 9-16.



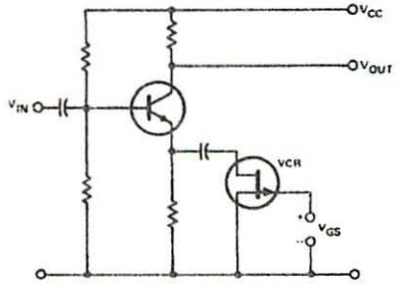
Voltage-Tuned Filter Octave Range with Lowest Frequency at JFET $V_{GS(off)}$ and Tuned by R_2. Upper Frequency is Controlled by R_1
Figure 9



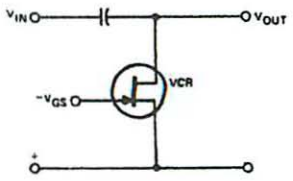
Electronic Gain Control
Figure 10



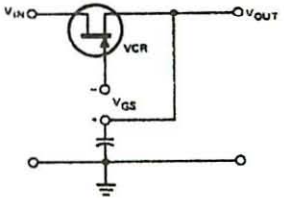
Cascaded VCR Attenuator
Figure 11



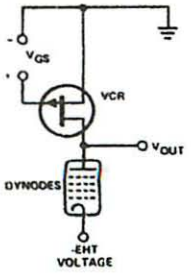
Wide Dynamic Range AGC Circuit. No Gain through FET with Distortion Proportional to Input Signal Level
Figure 12



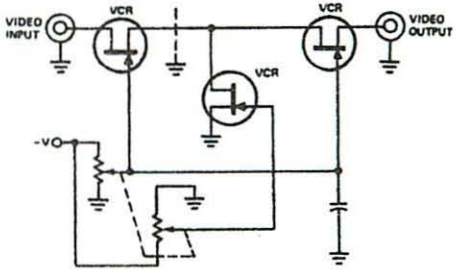
VCR Phase Advance Circuit
Figure 13



VCR Phase Retard Circuit
Figure 14



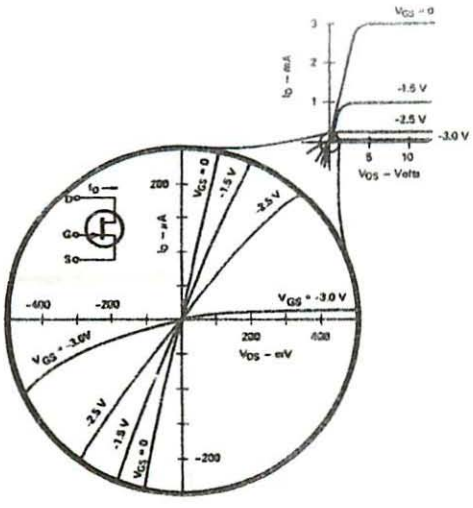
P-Channel VCR Photomultiplier Load. Required Low Photomultiplier Anode Current (Usually < 1 μA) Implies that VCR will Always Perform in Linear Region Near Origin
Figure 15



Voltage Controlled Variable Gain Amplifier. The Tee Attenuator Provides for Optimum Dynamic Linear Range Attenuation
Figure 16

Signal Distortion: Causes

Figure 17A repeats the FET output characteristic curves of Figure 2, to show that the bias lines bend down as V_{DS} increases in a positive direction toward the pinch-off voltage of the FET. The bending of the bias lines results in a change in r_{DS}, and hence the distortion encountered in VCR circuits; note that the distortion occurs in both the first and third quadrants. Distortion results because the channel depletion layer increases as V_{DS} reduces the drain current, so that a pinch-off condition is reached when $V_{DS} = V_{GS} - V_{GS(off)}$. Figure 17B shows how the current has an opposite effect



N-Channel JFET Output Characteristic Enlarged Around V_{DS} = 0

Figure 17A

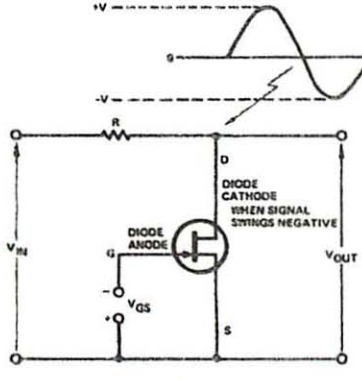


Figure 17B

in the third quadrant, rising negatively with an increasingly negative V_{DS}. This is due to the forward conduction of the gate-to-channel junction when the drain signal exceeds the negative gate bias voltage.

Reducing Signal Distortion

The majority of VCR applications require that signal distortion be kept to a minimum. Also, numerous applications require large signal handling capability. A simple feedback technique may be used to reduce distortion while permitting large signal handling capability; a small amount of drain signal is coupled to the gate through a resistor divider network, as shown in Figure 18.

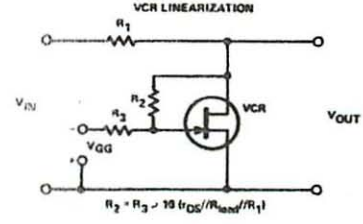


Figure 18

The application of a part of the positive drain signal to the gate causes the channel depletion layer to decrease, with a corresponding increase in drain current. Increasing the drain current for a given drain voltage tends to linearize the V_{GS} bias curves. On the negative half-cycle, a small negative voltage is coupled to the gate to reduce the amount of drain-gate forward bias. This in turn reduces the drain current and linearizes the bias lines. Now the channel resistance is dependent on the DC gate control voltage and not on the drain signal, unless the $V_{DS} = V_{GS} - V_{GS(off)}$ locus is approached. Resistors R_2 and R_3 in Figure 18 couple the drain signal to the gate; the resistor values are equal, so that symmetrical voltage-current characteristics are produced in both quadrants. The resistors must be sufficiently large to provide minimum loading to the circuit:

$$R_2 = R_3 \geq 10\,[R_1 \,||r_{ds}\,(\max)\,||R_L] \qquad (4)$$

Typically, 470K Ω resistors will work well for most applications. R_1 is selected so that the ratio of $r_{DS(on)}\,||R_L$ to $[(r_{DS(on)}\,||R_L) + R_1]$ gives the desired output voltage, or:

$$e_o = e_i \,\frac{r_{DS(on)}\,||R_L}{(r_{DS(on)}\,||R_L) + R_1} \qquad (5)$$

The feedback technique used in Figure 18 requires that the gate control voltage, V_{GG}, be twice as large as V_{GS} in Figure 17B for the same r_{DS} value. Use of a floating supply between the resistor junction and the FET gate will overcome this problem. The circuit is shown in Figure 19, and allows the gate control voltage to be the same value as that voltage used without a feedback circuit, while preserving the advantages to be gained through the feedback technique.

Appendix A to this Application Note is an analytical approximation of VCR FET distortion characteristics, both calculated and measured.

JFET Voltage-Controlled Resistors

Product Summary

Part Number	$V_{GS(off)}$ Max (V)	$V_{(BR)GSS}$ Min (V)	$r_{DS(on)}$ Max (Ω)
VCR2N	–7	–25	60
VCR4N	–7	–25	600
VCR7N	–5	–25	8000

Features

- Continuous Voltage-Controlled Resistance
- High Off-Isolation
- High Input Impedance

Benefits

- Gain Ranging Capability/Wide Range Signal Attenuation
- No Circuit Interaction
- Simplified Drive

Applications

- Variable Gain Amplifiers
- Voltage Controlled Oscillator
- AGC

Description

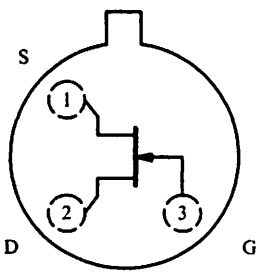
The VCR2N/4N/7N JFET voltage controlled resistors have an ac drain-source resistance that is controlled by a dc bias voltage (V_{GS}) applied to their high impedance gate terminal. Minimum r_{DS} occurs when V_{GS} = 0 V. As V_{GS} approaches the pinch-off voltage, r_{DS} rapidly increases. This series of junction FETs is intended for applications where the drain-source voltage is a low-level ac signal with no dc component.

Key to device performance is the predictable r_{DS} change versus V_{GS} bias where:

$$r_{DS}\text{bias} \approx \frac{r_{DS}(@\ V_{GS} = 0)}{1 - \left|\frac{V_{GS}}{V_{GS(off)}}\right|}$$

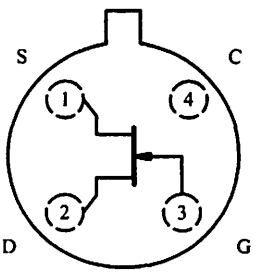
These n-channel devices feature $r_{DS(on)}$ ranging from 20 to 8000 Ω. All packages are hermetically sealed and may be processed per MIL-S-19500 (see Military Information).

TO-206AA
(TO-18)



Top View
VCR2N, VCR4N

TO-206AF
(TO-72)



Top View
VCR7N

Updates to this data sheet may be obtained via facsimile by calling Siliconix FaxBack, 1-408-970-5600. Please request FaxBack document #70293. Applications information may also be obtained via FaxBack, request document #70598.

Absolute Maximum Ratings[a]

Gate-Source, Gate-Drain Voltage ..... -25 V
Gate Current ..... 10 mA
Power Dissipation[b] ..... 300 mW
Operating Junction Temperature Range ..... -55 to 175°C
Storage Temperature ..... -65 to 200°C
Lead Temperature ($^1/_{16}$" from case for 10 sec.) ..... 300°C

Notes:
a. T_A = 25°C unless otherwise noted.
b. Derate 2 mW/°C above 25°C.

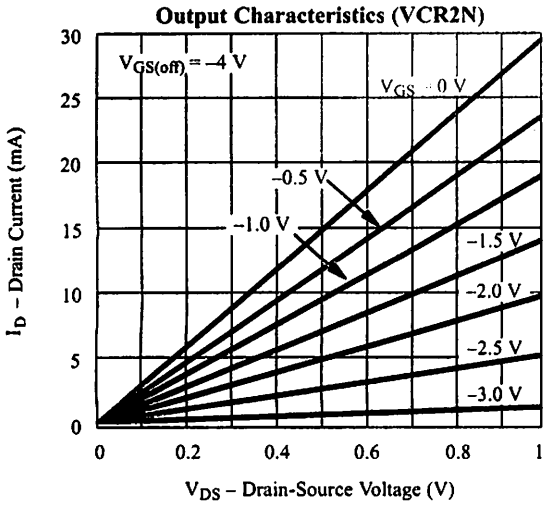
Specifications[a]

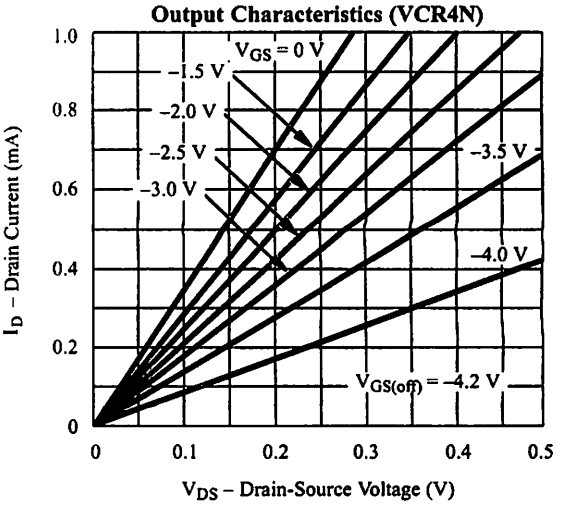
Parameter	Symbol	Test Conditions	Typ[b]	Limits VCR2N Min	Limits VCR2N Max	Limits VCR4N Min	Limits VCR4N Max	Limits VCR7N Min	Limits VCR7N Max	Unit
Static										
Gate-Source Breakdown Voltage	$V_{(BR)GSS}$	I_G = -1 µA, V_{DS} = 0 V	-55	-25		-25		-25		V
Gate-Source Cutoff Voltage	$V_{GS(off)}$	V_{DS} = 10 V, I_D = 1 µA		-3.5	-7	-3.5	-7	-2.5	-5	V
Gate Reverse Current	I_{GSS}	V_{GS} = -15 V, V_{DS} = 0 V			-5		-0.2		-0.1	nA
Drain-Source On-Resistance	$r_{DS(on)}$	V_{GS} = 0 V, I_D = 10 mA		20	60					Ω
		V_{GS} = 0 V, I_D = 1 mA				200	600			Ω
		V_{GS} = 0 V, I_D = 0.1 mA						4000	8000	Ω
Gate-Source Forward Voltage	$V_{GS(F)}$	V_{DS} = 0 V, I_G = 1 mA	0.7							V
Dynamic										
Drain-Source On-Resistance	$r_{ds(on)}$	V_{GS} = 0 V, I_D = 0 mA f = 1 kHz		20	60	200	600	4000	8000	Ω
Drain-Gate Capacitance	C_{dg}	V_{GD} = -10 V, I_S = 0 mA f = 1 MHz			7.5		3		1.5	pF
Source-Gate Capacitance	C_{sg}	V_{GS} = -10 V, I_D = 0 mA f = 1 kHz			7.5		3		1.5	pF

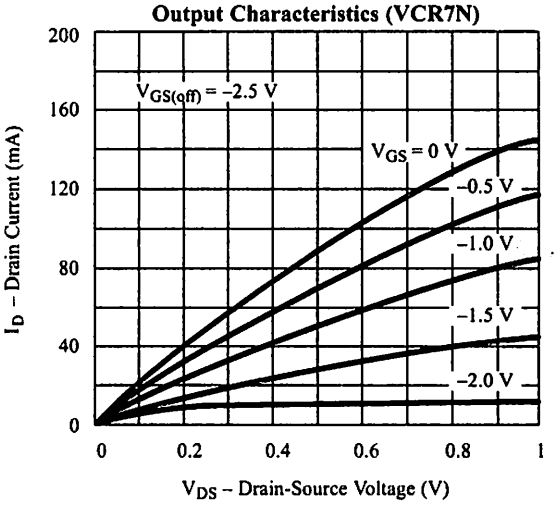
Notes:
a. T_A = 25°C unless otherwise noted.
b. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.

NCB NPA NT

Typical Characteristics







Applications

A simple application of a FET VCR is shown in Figure 1, the circuit for a voltage divider attenuator.

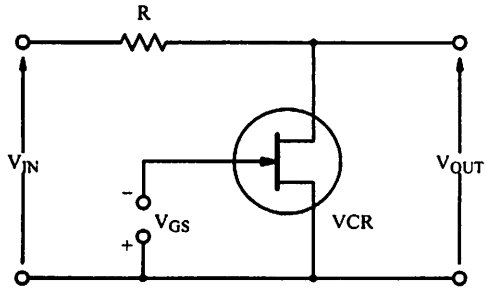


Figure 1. Simple Attenuator Circuit

The output voltage is:

$$V_{OUT} = \frac{V_{IN}\, r_{DS}}{R + r_{DS}}$$

It is assumed that the output voltage is not so large as to push the VCR out of the linear resistance region, and that the r_{DS} is not shunted by the load.

The lowest value which V_{OUT} can assume is:

$$V_{OUT(min)} = \frac{V_{IN}\, r_{DS(on)}}{R + r_{DS(on)}}$$

Since r_{DS} can be extremely large, the highest value is:

$$V_{OUT(max)} = V_{IN}$$