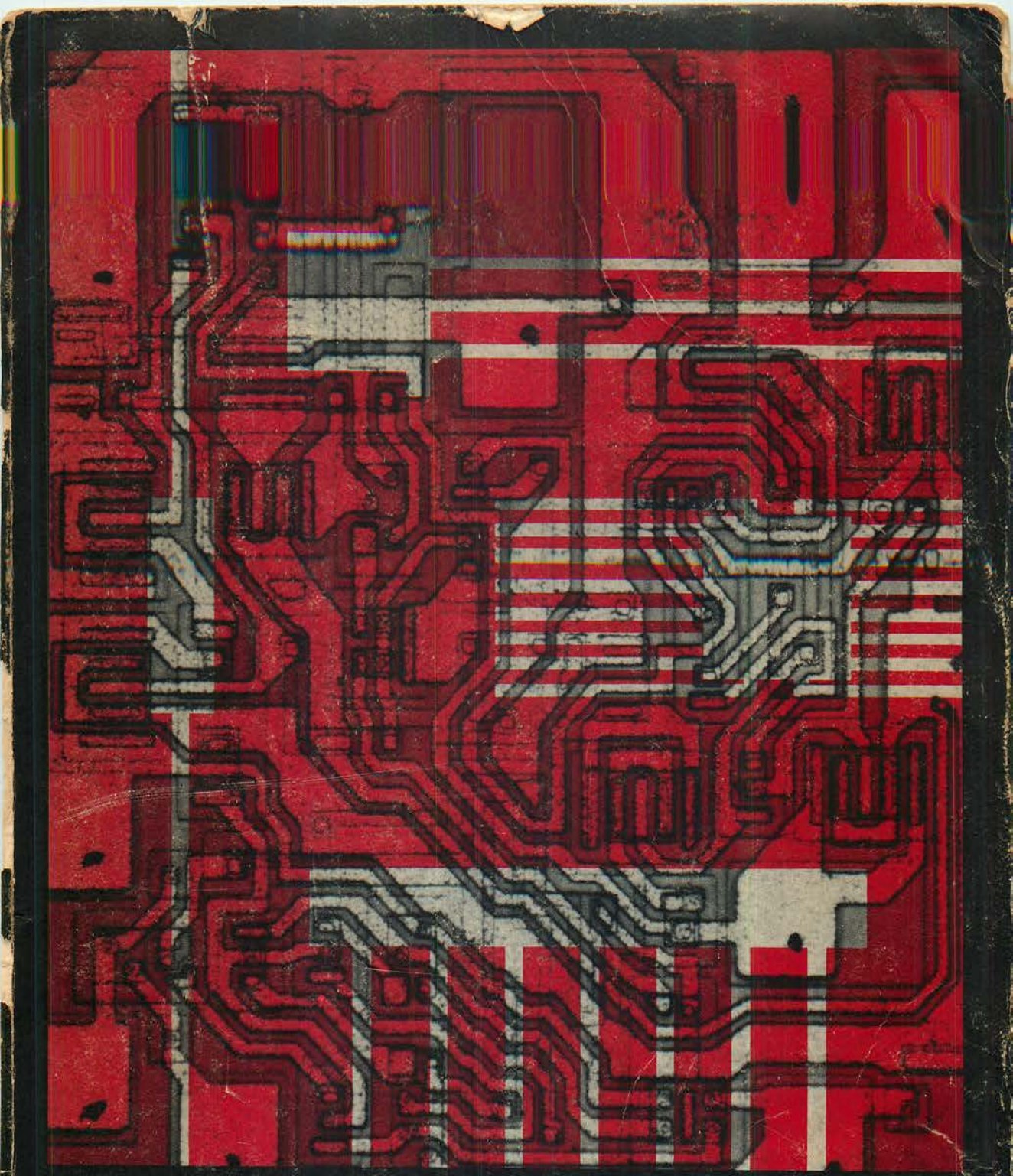


PRODUCT CATALOG 1972/1973

ITT
SEMICONDUCTORS

CONTENTS

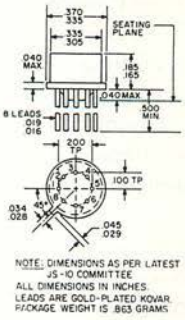
725M72

Printed In U.S.A.

HIGH PERFORMANCE OPERATIONAL AMPLIFIER

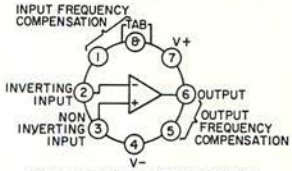
- **Tight Transient Response Specs**
- **Low Input Offset Voltage**
- **Large Input Common Mode Range**
- **High Output Voltage Swing**

DIMENSIONS
SIMILAR TO TO-5



NOTE: DIMENSIONS AS PER LATEST JS-10 COMMITTEE
ALL DIMENSIONS IN INCHES
LEADS ARE GOLD-PLATED KOVAR
PACKAGE WEIGHT IS .863 GRAMS

CONNECTION DIAGRAM
(Top View)



NOTE: PIN 4 CONNECTED TO CASE.

The MIC 709-A is a high-gain operational amplifier constructed on a single silicon chip using the ITT Planar epitaxial process. It features low offset, high input impedance, large input common mode range, high output swing under load and low power consumption. The device displays exceptional temperature stability and will operate over a 14-36 voltage range with little degradation of performance. The amplifier is intended for use in DC servo systems, high impedance analog computers, in low-level instrumentation applications and for the generation of special linear and nonlinear transfer functions. The 709A is a direct plug in replacement for the 709.

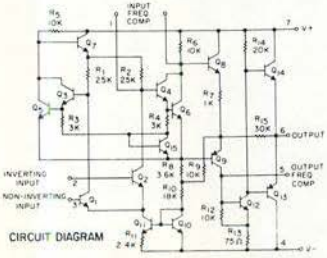
ABSOLUTE MAXIMUM RATINGS

CHARACTERISTICS		UNITS
Supply Voltage	36	Volts
Internal Power Dissipation (Note 1)	300	mW
Differential Input Voltage	±5.0	Volts
Input Voltage	±10	Volts
Output Short-Circuit Duration (T_A = 25°C)	5	sec
Storage Temperature Range	−65 to +150	°C
Operating Temperature Range	−55 to +125	°C
Lead Temperature (Soldering, 60 sec)	300	°C

NOTE 1: Rating applies for case temperatures to +125°C; derate linearly at 5.6 mW/°C for ambient temperatures above +95°C.

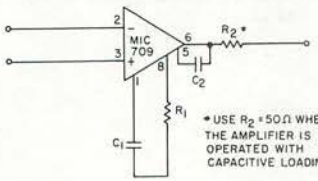
ELECTRICAL CHARACTERISTICS ($T_A = +25°C$, $\pm 9V \leq V_S \leq \pm 15V$ unless otherwise noted)

PARAMETER (see definitions)	MIN.	TYP.	MAX.	UNITS	CONDITIONS
Input Offset Voltage		0.6	2.0	mV	$R_S \leq 10K\Omega$
Input Offset Current		10	50	nA	
Input Bias Current		100	200	nA	
Input Resistance	350	700		KΩ	
Output Resistance		150		Ω	
Power Consumption		75	108	mW	$V_S = \pm 15V$
Transient Response Risetime			1.5	μs	$V_{in} = 20mV$, $R_L = 2K\Omega$, $C_1 = 5000$ pF, $R_1 = 1.5$ KΩ, $C_2 = 200pF$, $R_2 = 50\Omega$
Overshoot			30	%	$C_L \leq 100pF$
The following specifications apply for $-55°C \leq T_A \leq +125°C$:					
Input Offset Voltage			3.0	mV	$R_S \leq 10K\Omega$
Average Temperature Coefficient of Input Offset Voltage		1.8	10	μV/°C	$R_S = 50\Omega$ $T_A = +25°C$ TO $T_A = +125°C$
		1.8	10	μV/°C	$R_S = 50\Omega$ $T_A = +25°C$ TO $T_A = -55°C$
		2.0	15	μV/°C	$R_S \leq 10K\Omega$ $T_A = +25°C$ TO $T_A = +125°C$
		4.8	25	μV/°C	$R_S = 10K\Omega$ $T_A = +25°C$ TO $T_A = -55°C$
		0.08	0.5	nA/°C	$T_A = +25°C$ TO $T_A = +125°C$
		0.45	2.8	nA/°C	$T_A = +25°C$ TO $T_A = +55°C$
Large-Signal Voltage Gain	25,000		70,000		$V_S = \pm 15V$, $R_L \geq 2K\Omega$, $V_{out} = \pm 10V$
Output Voltage Swing	±12	±14		V	$V_S = \pm 15V$, $R_L \geq 10K\Omega$
	±10	±13		V	$V_S = \pm 15V$, $R_L \geq 2K\Omega$
Input Voltage Range	±8.0			V	$V_S = \pm 15V$
Common Mode Rejection Ratio	80	110		db	$R_S \leq 10K\Omega$
Supply Voltage Rejection Ratio		40	100	μV/V	$R_S \leq 10K\Omega$
Supply Current		2.1	3.0	mA	$T_A = +125°C$, $V_S = \pm 15V$
		2.7	4.5	mA	$T_A = -55°C$, $V_S = \pm 15V$
Power Consumption		63	90	mA	$T_A = +125°C$, $V_S = \pm 15V$
		81	135	mA	$T_A = -55°C$, $V_S = \pm 15V$
Input Offset Current		35	50	nA	$T_A = +125°C$
		40	250	nA	$T_A = -55°C$
Input Bias Current		300	600	nA	$T_A = -55°C$
Input Resistance	85	170		kΩ	

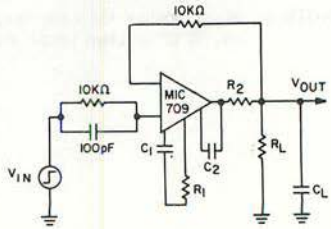


CIRCUIT DIAGRAM

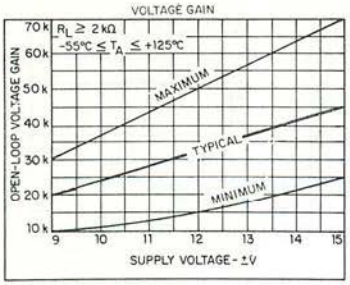
FREQUENCY COMPENSATION CIRCUIT

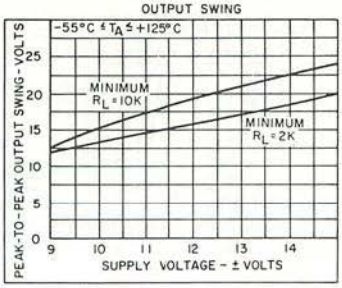


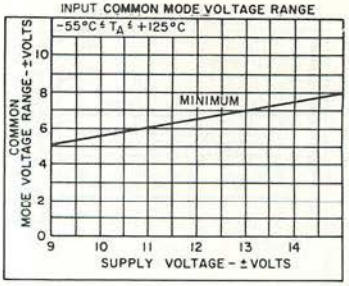
TRANSIENT RESPONSE TEST CIRCUIT



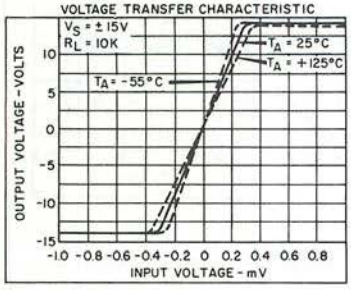
GUARANTEED ELECTRICAL CHARACTERISTICS

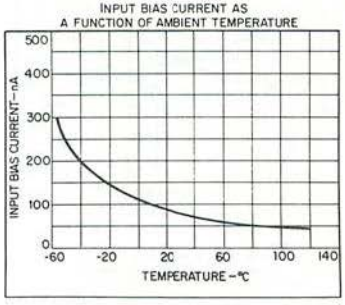


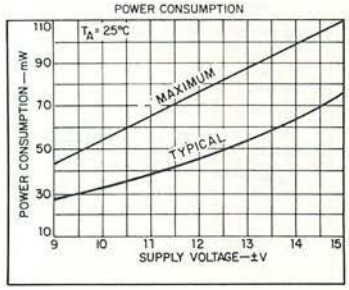


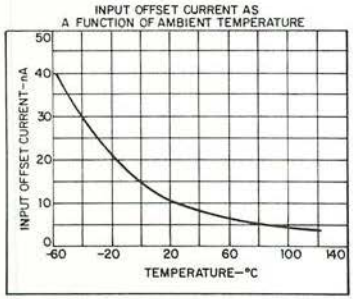


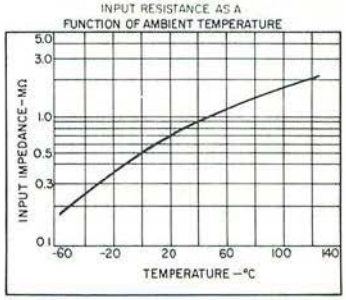
TYPICAL PERFORMANCE CURVES

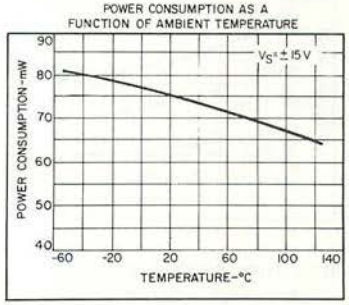


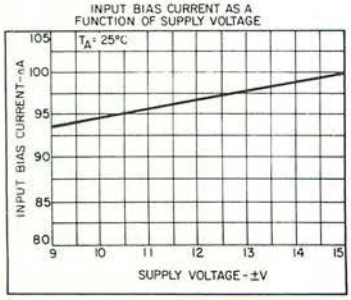


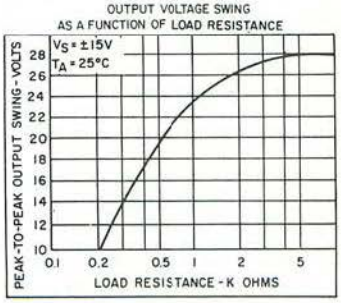


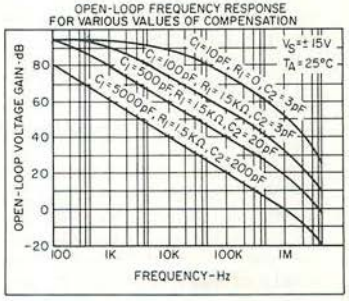






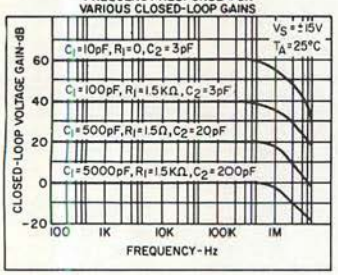




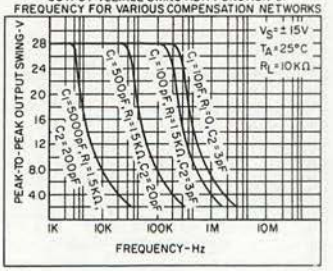


TYPICAL PERFORMANCE CURVES, continued

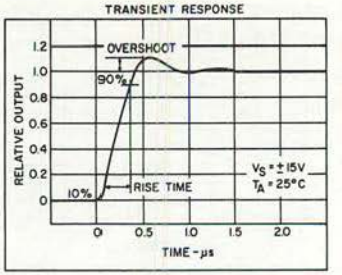
FREQUENCY RESPONSE FOR VARIOUS CLOSED-LOOP GAINS



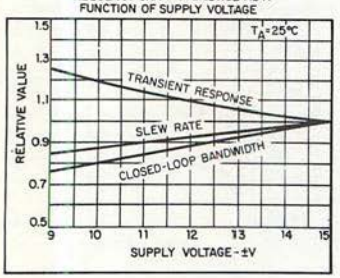
OUTPUT VOLTAGE SWING AS A FUNCTION OF FREQUENCY FOR VARIOUS COMPENSATION NETWORKS



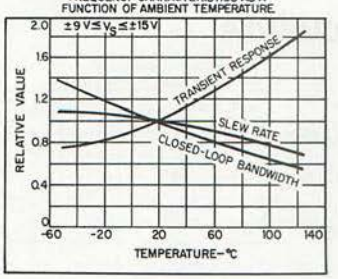
TRANSIENT RESPONSE



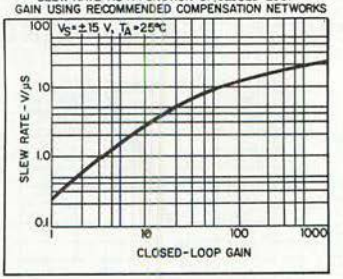
FREQUENCY CHARACTERISTICS AS A FUNCTION OF SUPPLY VOLTAGE



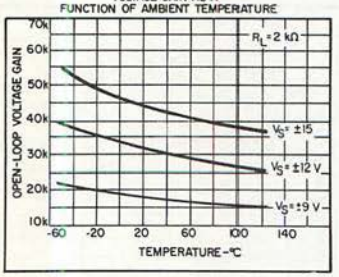
FREQUENCY CHARACTERISTICS AS A FUNCTION OF AMBIENT TEMPERATURE



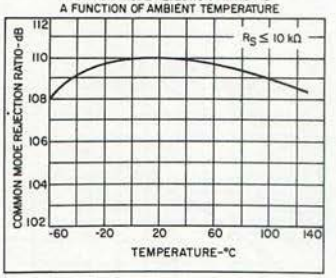
SLEW RATE AS A FUNCTION OF CLOSED-LOOP GAIN USING RECOMMENDED COMPENSATION NETWORKS



VOLTAGE GAIN AS A FUNCTION OF AMBIENT TEMPERATURE



COMMON MODE REJECTION RATIO AS A FUNCTION OF AMBIENT TEMPERATURE



DEFINITION OF TERMS:

INPUT OFFSET VOLTAGE—That voltage which must be applied between the input terminals to obtain zero output voltage. The input offset voltage may also be defined for the case where two equal resistances are inserted in series with the input leads.

INPUT OFFSET CURRENT—The difference in the currents into the two input terminals with the output at zero volts.

INPUT RESISTANCE—The resistance looking into either input terminal with the other grounded.

INPUT BIAS CURRENT—The average of the two input currents.

INPUT VOLTAGE RANGE—A range of voltage which, if exceeded on either input terminal, could cause the amplifier to cease functioning properly.

INPUT COMMON MODE REJECTION RATIO—The ratio of the input voltage range to the maximum change in input offset voltage over this range.

LARGE-SIGNAL VOLTAGE GAIN—The ratio of the maximum output voltage swing with load to the change in input voltage required to drive the output from zero to this voltage.

OUTPUT VOLTAGE SWING—The peak output swing, referred to zero, that can be obtained without clipping.

OUTPUT RESISTANCE—The resistance seen looking into the output terminal with the output at null. This parameter is defined only under small signal conditions at frequencies above a few hundred cycles to eliminate the influence of drift and thermal feedback.

POWER CONSUMPTION—The DC power required to operate the amplifier with the output at zero and with no load current.

SUPPLY VOLTAGE REJECTION RATIO—The ratio of the change in input offset voltage to the change in supply voltage producing it.

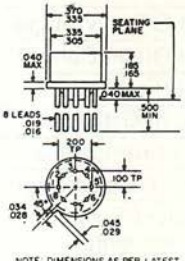
TRANSIENT RESPONSE—The closed-loop step function response of the amplifier under small-signal conditions.

HIGH PERFORMANCE OPERATIONAL AMPLIFIER

- **Tight Transient Response Specs**
- **Low Input Offset Voltage**
- **Large Input Common Mode Range**
- **High Output Voltage Swing**

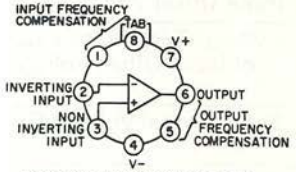
The MIC709-1 and MIC709-5 are high-gain operational amplifiers constructed on a single silicon chip using the ITT Planar epitaxial process. They feature low offset, high input impedance, large input common mode range, high output swing under load and low power consumption. The devices display exceptional temperature stability and will operate over a wide voltage range with little degradation of performance. These amplifiers are intended for use in DC servo systems, high impedance analog computers, in low-level instrumentation applications and for the generation of special linear and nonlinear transfer functions. The devices utilize the same pin configuration.

DIMENSIONS
SIMILAR TO TO-5



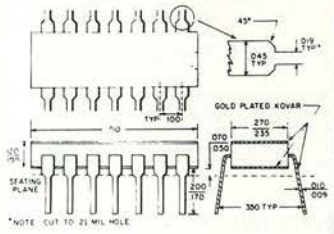
NOTE: DIMENSIONS AS PER LATEST JS-10 COMMITTEE
ALL DIMENSIONS IN INCHES
LEADS ARE GOLD-PLATED KOVAR
PACKAGE WEIGHT IS .863 GRAMS

CONNECTION DIAGRAM
(Top View)

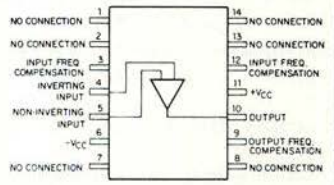


NOTE: PIN 4 CONNECTED TO CASE.

DUAL IN-LINE PACKAGE



CONNECTION DIAGRAM



ABSOLUTE MAXIMUM RATINGS

CHARACTERISTICS		UNITS
Supply Voltage	±18	Volts
Internal Power Dissipation (Note 1)	300	mW
Differential Input Voltage	±5.0	Volts
Input Voltage	±10	Volts
Output Short-Circuit Duration ($T_A = 25°C$)	5	sec.
Storage Temperature Range	−65 to +150	°C
Operating Temperature Range (Note 2)	−55 to +125	°C
Lead Temperature (Soldering, 60 sec)	300	°C

NOTE 1: Rating applies to the MIC709-1 at case temperatures to +125°C; derate linearly at 5.6 mW/°C for ambient temperatures above +95°C. The rating for the MIC709-5 is 250mW and applies for case temperatures to +70°C.

NOTE 2: Rating for the MIC709-5 is 0° to +70°C.

ELECTRICAL CHARACTERISTICS ($T_A = +25°C$, $\pm 9V \leq V_S \leq \pm 15V$ unless otherwise noted)

PARAMETER (see definitions)	MIN.	TYP.	MAX.	UNITS	CONDITIONS
Input Offset Voltage		1.0	5.0	mV	$R_S \leq 10K\Omega$
Input Offset Current		50	200	nA	
Input Bias Current		200	500	nA	
Input Resistance	150	400		KΩ	
Output Resistance		150		Ω	
Power Consumption		80	165	mW	$V_S = \pm 15V$
Transient Response Risetime Overshoot		 0.3 10	 1.0 30	 μs %	$V_{in} = 20mV$, $R_L = 2K\Omega$, $C_1 = 5000$ pF, $R_1 = 1.5$ KΩ, $C_2 = 200pF$, $R_2 = 50\Omega$ $C_L \leq 100pF$
The following specifications apply for $-55°C \leq T_A \leq +125°C$:					
Input Offset Voltage			6.0	mV	$R_S \leq 10K\Omega$
Average Temperature Coefficient of Input Offset Voltage		3.0 6.0		μV/°C μV/°C	$R_S = 50\Omega$ $R_S \leq 10K\Omega$
Large-Signal Voltage Gain	25,000	45,000	70,000		$V_S = \pm 15V$, $R_L \geq 2K\Omega$, $V_{out} = \pm 10V$
Output Voltage Swing	± 12 ± 10	± 14 ± 13		V V	$V_S = \pm 15V$, $R_L \geq 10K\Omega$ $V_S = \pm 15V$, $R_L \geq 2K\Omega$
Input Voltage Range	± 8.0	± 10		V	$V_S = \pm 15V$
Common Mode Rejection Ratio	70	90		db	$R_S \leq 10K\Omega$
Supply Voltage Rejection Ratio		25	150	μV/V	$R_S \leq 10K\Omega$
Input Offset Current		20 100	200 500	nA nA	$T_A = +125°C$ $T_A = -55°C$
Input Bias Current		0.5	1.5	μA	$T_A = -55°C$
Input Resistance	40	100		kΩ	

DEFINITION OF TERMS:

INPUT OFFSET VOLTAGE—That voltage which must be applied between the input terminals to obtain zero output voltage. The input offset voltage may also be defined for the case where two equal resistances are inserted in series with the input leads.

INPUT OFFSET CURRENT—The difference in the currents into the two input terminals with the output at zero volts.

INPUT RESISTANCE—The resistance looking into either input terminal with the other grounded.

INPUT BIAS CURRENT—The average of the two input currents.

INPUT VOLTAGE RANGE—A range of voltage which, if exceeded on either input terminal, could cause the amplifier to cease functioning properly.

INPUT COMMON MODE REJECTION RATIO—The ratio of the input voltage range to the maximum change in input offset voltage over this range.

LARGE-SIGNAL VOLTAGE GAIN—The ratio of the maximum output voltage swing with load to the change in input voltage required to drive the output from zero to this voltage.

OUTPUT VOLTAGE SWING—The peak output swing, referred to zero, that can be obtained without clipping.

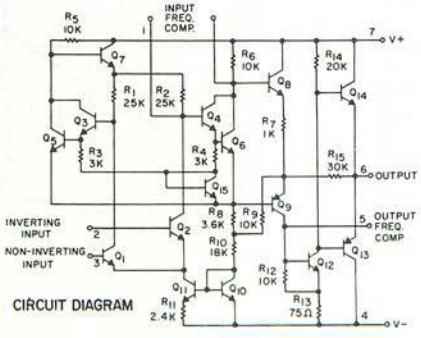
OUTPUT RESISTANCE—The resistance seen looking into the output terminal with the output at null. This parameter is defined only under small signal conditions at frequencies above a few hundred cycles to eliminate the influence of drift and thermal feedback.

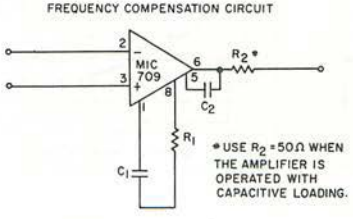
POWER CONSUMPTION—The DC power required to operate the amplifier with the output at zero and with no load current.

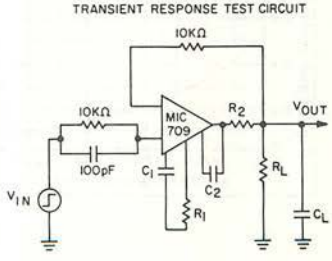
SUPPLY VOLTAGE REJECTION RATIO—The ratio of the change in input offset voltage to the change in supply voltage producing it.

ELECTRICAL CHARACTERISTICS (V_S = ±15V, T_A = 25°C unless otherwise specified)

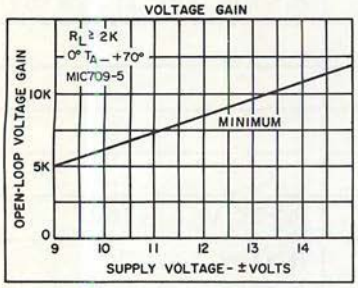
PARAMETER	MIN.	TYP.	MAX.	UNITS	CONDITIONS
Input Offset Voltage		2.0	7.5	mV	$R_S \leq 10K$, $\pm 9V \leq V_S \leq \pm 15V$
Input Offset Current		100	500	nA	
Input Bias Current		0.3	1.5	μA	
Input Resistance	50	250		KΩ	
Output Resistance		150		Ω	
Large-Signal Voltage Gain	15,000	45,000			$R_L \geq 2K$, $V_{OUT} = \pm 10V$
Output Voltage Swing	±12 ±10	±14 ±13		V V	$R_L \geq 10K$ $R_L \geq 2K$
Input Voltage Range	±8.0	±10		V	
Common Mode Rejection Ratio	65	90		db	$R_S \leq 10K$
Supply Voltage Rejection Ratio		25	200	μV/V	$R_S \leq 10K$
Power Consumption		80	200	mW	
Transient Response Risetime Overshoot		 0.3 10	 1.0 30	 μs %	$V_{in} = 20mV$, $R_L = 2K\Omega$, $C_1 = 5000$ pF, $R_1 = 1.5$ KΩ, $C_2 = 200$pF, $R_2 = 50\Omega$ $C_L \leq 100$pF
The following specifications apply for $0°C \leq T_A \leq +70°C$					
Input Offset Voltage			10	mV	$R_S \leq 10K$, $\pm 9V \leq V_S \leq \pm 15V$
Input Offset Current			750	nA	
Input Bias Current			2.0	μA	
Large-Signal Voltage Gain	12,000				$R_L \geq 2K$, $V_{OUT} = \pm 10V$
Input Resistance	35			kΩ	

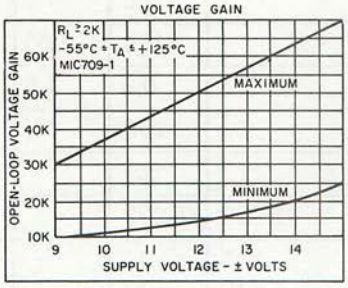


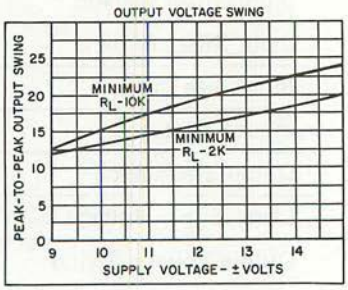




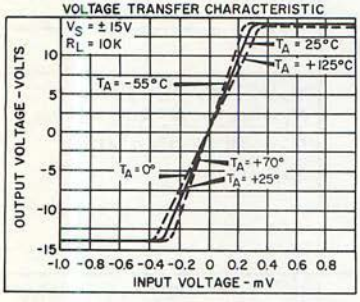
GUARANTEED ELECTRICAL CHARACTERISTICS

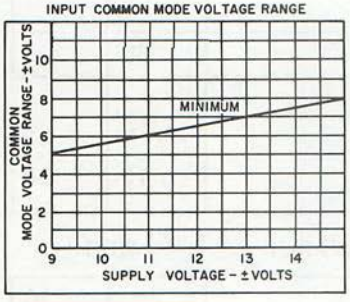


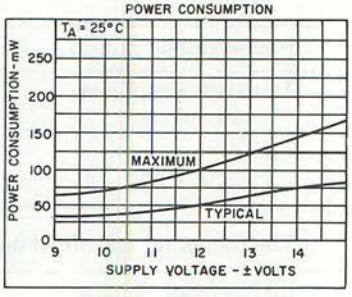


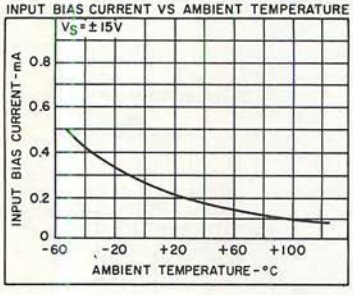


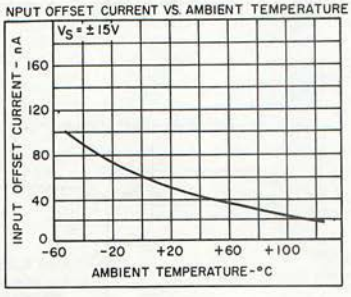
TYPICAL PERFORMANCE CURVES

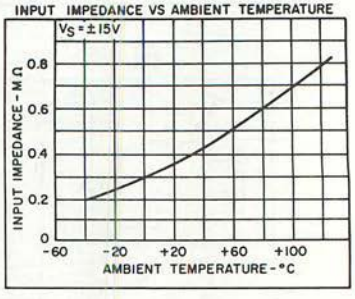






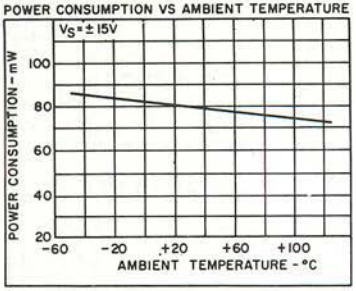




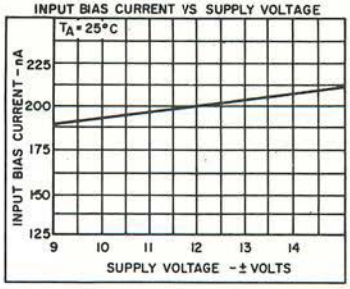


TYPICAL PERFORMANCE CURVES, continued

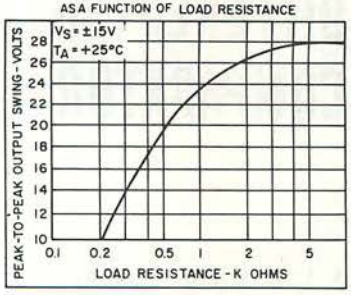
POWER CONSUMPTION VS AMBIENT TEMPERATURE



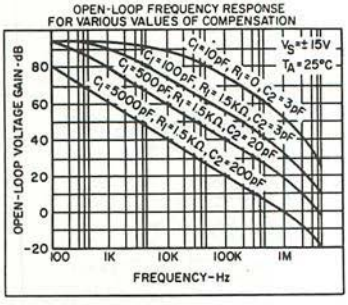
INPUT BIAS CURRENT VS SUPPLY VOLTAGE



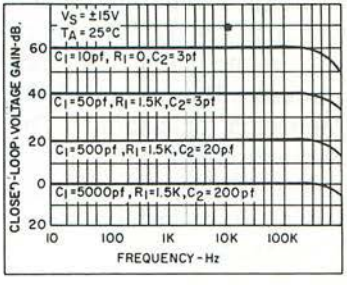
OUTPUT VOLTAGE SWING AS A FUNCTION OF LOAD RESISTANCE



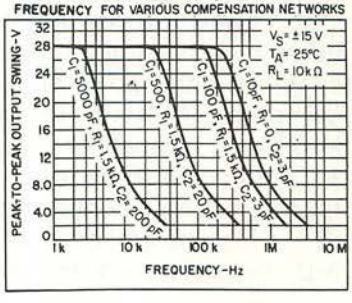
OPEN-LOOP FREQUENCY RESPONSE FOR VARIOUS VALUES OF COMPENSATION



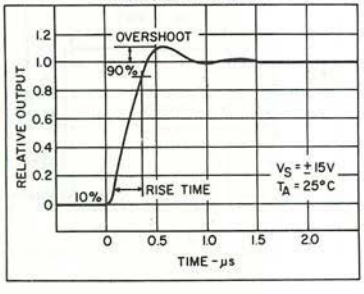
FREQUENCY RESPONSE FOR VARIOUS CLOSED-LOOP GAINS



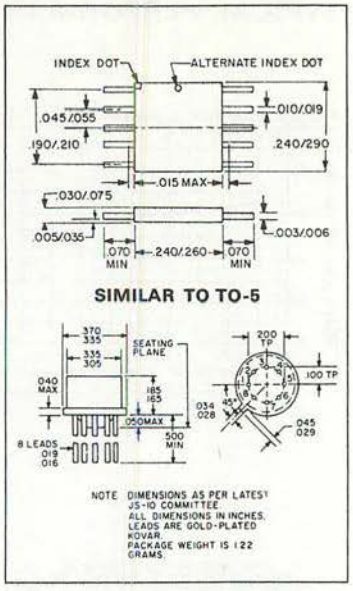
OUTPUT VOLTAGE SWING AS A FUNCTION OF FREQUENCY FOR VARIOUS COMPENSATION NETWORKS



TRANSIENT RESPONSE



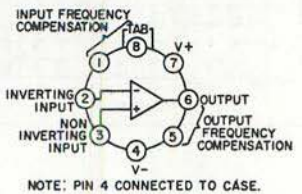
HIGH SPEED DIFFERENTIAL COMPARATOR



- **Low Offset Voltage**
- **Low Offset Current**
- **High Voltage Gain**
- **Fast Response Time**

The ITT MIC 710 is a differential voltage comparator which offers high accuracy and fast response times. The entire circuit is contained on one silicon chip and is manufactured using the ITT Planar Epitaxial process. The output of the MIC 710 is compatible with all integrated logic forms. The MIC 710 can also be used as a variable threshold Schmidt trigger, a pulse height discriminator, a memory sense amplifier, a high noise immunity line receiver, or in high speed A-D conversion and multivibrator functions.

CONNECTION DIAGRAM
(Top View)

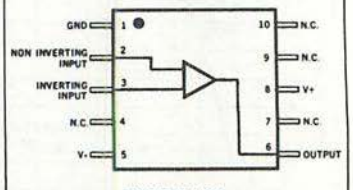


NOTE: PIN 4 CONNECTED TO CASE.

ABSOLUTE MAXIMUM RATINGS

CHARACTERISTICS	UNITS
Positive Supply Voltage	+14.0 V
Negative Supply Voltage	−7.0 V
Peak Output Current	10 mA
Differential Input Voltage	±5.0 V
Input Voltage	±7.0 V
Internal Power Dissipation (MIC710-1 Note 1, MIC710-5 Note 2)	300 mW
Operating Temperature Range MIC710-1	−55° to +125°C
MIC710-5	0° to +70°C
Storage Temperature Range	−65° to +150°C
Lead Temperature (Soldering, 60 sec.)	300°C

CONNECTION DIAGRAM
(Top View)



FLAT PACK

ELECTRICAL CHARACTERISTICS for 710-5 (TA = 25°C, V = 12.0V, V = −6.0V unless otherwise specified)

PARAMETER (see definitions)	MIN.	TYP.	MAX.	UNITS	CONDITIONS (Note 5)
Input Offset Voltage		1.6	5.0	mV	$R_S \leqslant 200\Omega$
Input Offset Current		1.8	5.0	uA	
Input Bias Current		16	25	uA	
Voltage Gain	1000	1500			
Output Resistance		200		Ω	
Output Sink Current	1.6	2.5		mA	$\Delta V_{in} \geqslant 5mV$, $V_{out} = 0$
Response Time (Note 3)		40		ns	
The following specifications apply for 0°C ≤TA ≤+70°C:					
Input Offset Voltage			6.5	mV	$R_S \leqslant 200\Omega$
Average Temperature Coefficient of Input Offset Voltage		5.0	20	uV/°C	$R_S = 50\Omega$, TA = 0°C to TA = +70°C
Input Offset Current			7.5	uA	
Average Temperature Coefficient of Input Offset Current		15	50	nA/°C	TA = 25°C to TA = +70°C
		24	100	nA/°C	TA = 25°C to TA = 0°C
Input Bias Current		25	40	uA	TA = 0°C
Input Voltage Range	±5.0			V	V⁻ = −7.0V
Common Mode Rejection Ratio	70	98		dB	$R_S \leqslant 200$
Differential Input Voltage Range	±5.0			V	
Voltage Gain	800				
Positive Output Level	2.5	3.2	4.0	V	$\Delta V_{in} \geqslant 5mV$, $0 \leqslant I_{out} \leqslant 5.0mA$
Negative Output Level	−1.0	−0.5	0	V	$\Delta V_{in} \geqslant 5mV$
Output Sink Current	0.5			mA	$\Delta V_{in} \geqslant 5mV$, $V_{out} = 0$
Positive Supply Current		5.2	9.0	mA	$V_{out} \leqslant 0$
Negative Supply Current		4.6	7.0	mA	
Power Consumption		90	150	mW	

DEFINITION OF TERMS:

LOGIC THRESHOLD VOLTAGE — The approximate voltage at the output of the comparator at which the loading logic circuitry changes its digital state.

INPUT OFFSET VOLTAGE* — The voltage between the input terminals when the output is at the logic threshold voltage. The input offset voltage may also be defined for the case where two equal resistances are inserted in series with the input leads.

INPUT OFFSET CURRENT* — The difference in the currents into the two input terminals with the output at the logic threshold voltage.

INPUT BIAS CURRENT* — The average of the two input currents.

INPUT VOLTAGE RANGE* — The range of voltage on the input terminals for which the comparator will operate within specifications.

DIFFERENTIAL INPUT VOLTAGE RANGE* — The range of voltage between the input terminals for which operation within specifications is assured.

VOLTAGE GAIN* — The ratio of the change in output voltage to the change in voltage between the input terminals producing it with the DC output level in the vicinity of the logic threshold voltage.

RESPONSE TIME* — The interval between the application of an input step function and the time when the output crosses the logic threshold voltage. The input step drives the comparator from some initial, saturated input voltage to an input level just barely in excess of that required to bring the output from saturation to the logic threshold voltage. This excess is referred to as the voltage overdrive.

STROBE RELEASE TIME* — The time required for the output to rise to the logic threshold voltage after the strobe terminal has been driven from the zero to the one logic level. Appropriate input conditions are assumed.

POSITIVE OUTPUT LEVEL* — The DC output voltage in the positive direction with the input voltage equal to or greater than a minimum specified amount.

NEGATIVE OUTPUT LEVEL* — The DC output voltage in the negative direction with the input voltage equal to or greater than a minimum specified amount.

OUTPUT SINK CURRENT — The maximum negative current that can be delivered by the comparator.

PEAK OUTPUT CURRENT — The maximum current that may flow into the output load without causing damage to the comparator.

OUTPUT RESISTANCE* — The resistance seen looking into the output terminal with the DC output level at the logic threshold voltage.

STROBED OUTPUT LEVEL* — The DC output voltage, independent of input voltage with the voltage on the strobe terminal equal to or less than a minimum specified amount.

STROBE CURRENT — The maximum current drawn by the strobe terminal when it is at the zero logic level.

POWER CONSUMPTION — The DC power into the amplifier with no output load. The DC power will vary with signal level, but is specified as a maximum for the entire range of input-signal conditions.

*These definitions apply for either side with the other disabled with the strobe.

ELECTRICAL CHARACTERISTICS for 710-1 ($T_A = +25°C$, $V = 12.0V$, $V = -6.0V$ unless otherwise specified)

PARAMETER (see definitions)	MIN.	TYP.	MAX.	UNITS	CONDITIONS (Note 4)
Input Offset Voltage		0.6	2.0	mV	$Rs \leq 200\Omega$
Input Offset Current		0.75	3.0	uA	
Input Bias Current		13	20	uA	
Voltage Gain	1250	1700			
Output Resistance		200		Ω	
Output Sink Current	2.0	2.5		mA	$\Delta V_{in} \leq 5mV$, $V_{out} = 0$
Response Time (Note 3)		40		ns	
The following specifications apply for $-55°C \leq T_A \leq +125°C$:					
Input Offset Voltage			3.0	mV	$Rs \leq 200\Omega$
Average Temperature Coefficient		3.5	10	uV/°C	$Rs = 50\Omega$, TA = 25°C to TA = +125°C
of Input Offset Voltage		2.7	10	uV/°C	$Rs 50\Omega$, TA = 25°C to TA = −55°C
Input Offset Current		0.25	3.0	uA	TA = +125°C
		1.8	7.0	uA	$T_A = -55°C$
Average Temperature Coefficient		5.0	25	nA/°C	$T_A = 25°C$ to $T_A = +125°C$
of Input Offset Current		15	75	nA/°C	$T_A = 25°C$ to $T_A = -55°C$
Input Bias Current		27	45	uA	$T_A = -55°C$
Input Voltage Range	±5.0			V	V = −7.0V
Common Mode Rejection Ratio	80	100		dB	$Rs \leq 200\Omega$
Differential Input Voltage Range	±5.0			V	
Voltage Gain	1000				
Positive Output Level	2.5	3.2	4.0	V	$V_{in} \leq 5mV$, $0 \leq I_{out} \leq 5.0mA$
Negative Output Level	−1.0	−0.5	0	V	$\Delta V_{in} \leq 5mV$
Output Sink Current	0.5	1.7		mA	$T_A = +125°C$, $\Delta V_{in} \leq 5mV$, $V_{out} = 0$
	1.0	2.3		mA	$T_A = -55°C$, $\Delta V_{in} \leq 5mV$, $V_{out} = 0$
Positive Supply Current		5.2	9.0	mA	$V_{out} \leq 0$
Negative Supply Current		4.6	7.0	mA	
Power Consumption		90	150	mW	

NOTES:

(1) Rating applies for case temperatures to +125°C; derate linearly at 5.6mW/°C for ambient temperatures above +105°C.

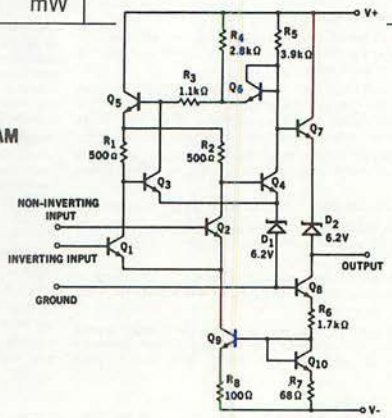
(2) Ratings apply for ambient temperatures to +70°C.

(3) The response time specified (see definitions) is for a 100-mV input step with 5-mV overdrive.

(4) The input offset voltage and input offset current (see definitions) are specified for a logic threshold voltage of 1.8V at −55°C, 1.4V at +25°C and 1.0V at +125°C.

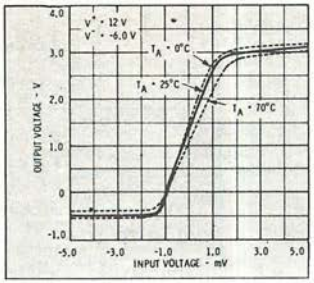
(5) The input offset voltage and input offset current (see definitions) are specified for a logic threshold voltage of 1.5V at 0°C, 1.4V at +25°C and 1.2V at +70°C.

SCHEMATIC DIAGRAM

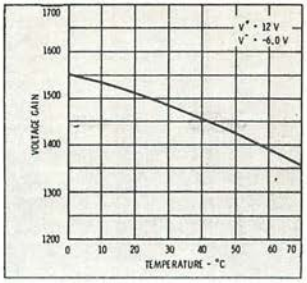


TYPICAL CHARACTERISTICS MIC 710-5 (TA = 25°C, V = 12.0V, V = −6.0V unless otherwise specified)

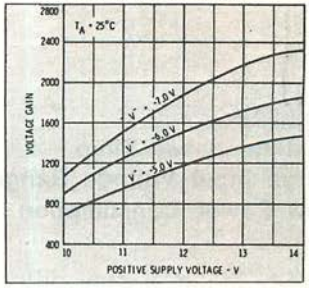
VOLTAGE TRANSFER CHARACTERISTIC



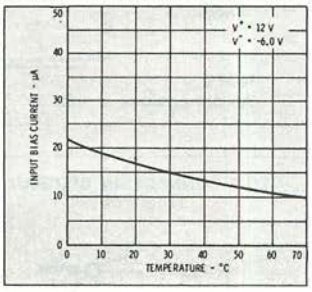
VOLTAGE GAIN AS A FUNCTION OF AMBIENT TEMPERATURE



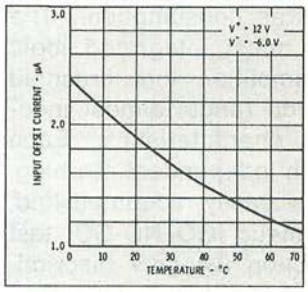
VOLTAGE GAIN AS A FUNCTION OF SUPPLY VOLTAGES



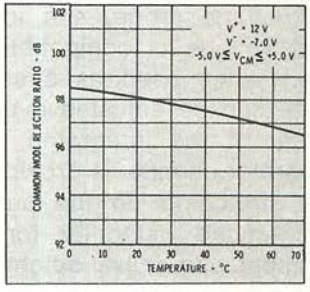
INPUT BIAS CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



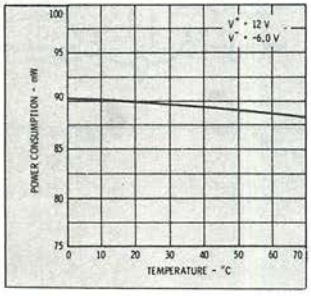
INPUT OFFSET CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



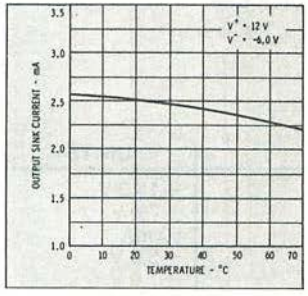
COMMON MODE REJECTION RATIO AS A FUNCTION OF AMBIENT TEMPERATURE



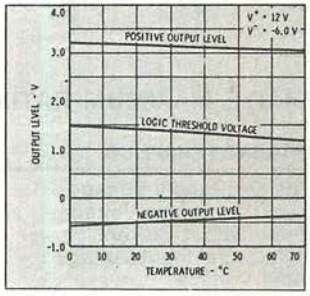
POWER CONSUMPTION AS A FUNCTION OF AMBIENT TEMPERATURE



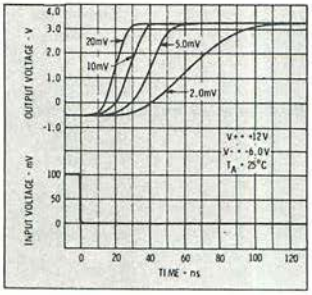
OUTPUT SINK CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



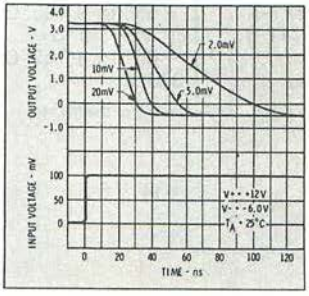
OUTPUT VOLTAGE LEVELS AS A FUNCTION OF AMBIENT TEMPERATURE



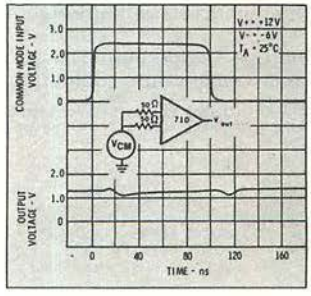
RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES



RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES



COMMON MODE PULSE RESPONSE

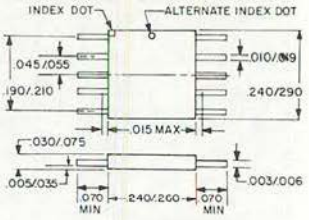


DUAL COMPARATOR

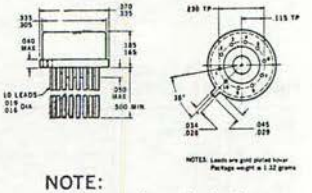
- **High Accuracy**
- **Fast Response Time**
- **Large Input Voltage Range**
- **Low Power Consumption**

The MIC 711 is a dual differential voltage comparator. It was primarily designed for core-memory sense amplifiers which require high accuracy, fast response times, large input voltage range, and low power consumption. The output voltage is compatible with most integrated logic forms. When used as a sense amplifier, the threshold voltage can be adjusted over a wide range, almost independent of the integrated circuit characteristics. Each comparator channel is provided with independent strobing. Pulse stretching on the output is easily accomplished. Double-ended detection for automatic GO/NO-GO test equipment and pulse height detection (window discriminator) are additional applications of the dual comparator. The entire circuit is contained on a silicon chip and is manufactured using ITT Planar Epitaxial process.

PHYSICAL DIMENSIONS
FLAT PACKAGE (TOP VIEW)

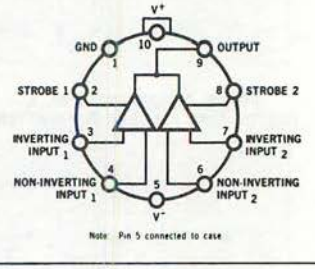


SIMILAR TO TO-5



NOTE:
All dimensions in inches

TO-5 CONNECTION DIAGRAM
(Top View)



ABSOLUTE MAXIMUM RATINGS

CHARACTERISTICS		UNITS
Positive Supply Voltage		+14.0 V
Negative Supply Voltage		−7.0 V
Peak Output Current		50 mA
Differential Input Voltage		±5.0 V
Input Voltage		±7.0 V
Strobe Voltage		0 to +6.0 V
Internal Power Dissipation (MIC711-1 Note 1, MIC711-5 Note 2)		300 mW
Operating Temperature Range	MIC711-1	−55° to +125°C
	MIC711-5	0° to +50°C
Storage Temperature Range		−65° to +150°C
Lead Temperature (Soldering, 60 sec.)		300°C

NOTES: (1) Rating applies for case temperatures to +125°C; derate linearly at 5.6mW/°C for ambient temperatures above +95°C.
(2) Rating applies for ambient temperatures to +70°C.

ELECTRICAL CHARACTERISTICS FOR 711-1 ($T_A = 25°C$, $V^+ = 12.0V$, $V^- = -6.0V$ unless otherwise specified)

PARAMETER (see definitions)	MIN.	TYP.	MAX.	UNITS	CONDITIONS
Input Offset Voltage		1.0 1.0	3.5 5.0	mV mV	$V_{out} = +1.4V, R_S \leq 200\Omega, V_{CM} = 0$ $V_{out} = +1.4V$, $R_S \leq 200\Omega$,
Input Offset Current		0.5	10.0	uA	$V_{out} = +1.4V$
Input Bias Current		25	75	uA	
Voltage Gain	750	1500			
Response Time (Note 3)		40		ns	
Strobe Release Time		12		ns	
Input Voltage Range	±5.0			V	$V^- = -7.0V$
Differential Input Voltage Range	±5.0			V	
Output Resistance		200		Ω	
Positive Output Level		4.5	5.0	V	$V_{in} \geq 10mV$
Loaded Positive Output Level	2.5	3.5		V	$V_{in} \geq 10mV$, $I_O = 5mA$
Negative Output Level	−1.0	−0.5	0	V	$V_{in} \geq 10mV$
Strobed Output Level	−1.0		0	V	$V_{strobe} \leq 0.3V$
Output Sink Current	0.5	0.8		mA	$V_{in} \geq 10mV$, $V_{out} \geq O$
Strobe Current		1.2	2.5	mA	$V_{strobe} = 100mV$
Positive Supply Current		8.6		mA	$V_{out} \leq 0$
Negative Supply Current		3.9		mA	
Power Consumption		130	200	mW	
The following specifications apply for $-55°C \leq T \leq 125°C$:					
Input Offset Voltage (Note 4)			4.5 6.0	mV mV	$R_S \leq 200\Omega$, $V_{CM} = 0$ $R_S \leq 200\Omega$
Input Offset Current (Note 4)			20	uA	
Input Bias Current			150	uA	
Temperature Coefficient of Input Offset Voltage		5.0		uV/°C	
Voltage Gain	500				

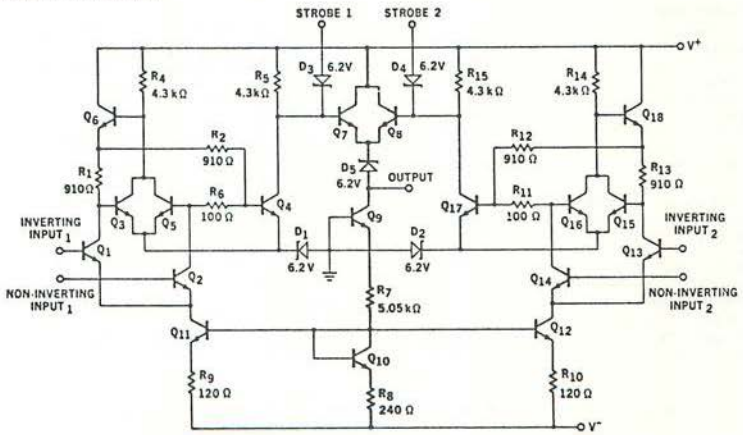
NOTES:

(3) The response time specified (see definitions) is for a 100-mV input step with 5-mV overdrive.

(4) The input offset voltage (see definitions) is specified for a logic threshold voltage of 1.8V at −55°C, 1.4V at +25°C and 1.0V at +125°C.

(5) The input offset voltage is specified for a logic threshold voltage of 1.5V at 0°C, 1.4V at +25°C and 1.2V at +70°C.

SCHEMATIC DIAGRAM



ELECTRICAL CHARACTERISTICS FOR 711-5 ($T_A = 25°C$, $V^+ = 12.0V$, $V^- = -6.0V$ unless otherwise specified)

PARAMETER	MIN.	TYP.	MAX.	UNITS	CONDITIONS
Input Offset Voltage		1.0 1.0	5.0 7.5	mV mV	$V_{out} = +1.4V, R_S \leq 200\Omega, V_{CM} = 0$ $V_{out} = +1.4V, R_S \leq 200\Omega,$
Input Offset Current		0.5	15	uA	$V_{out} = +1.4V$
Input Bias Current		25	100	uA	
Voltage Gain	700	1500			
Response Time (Note 3)		40		ns	
Strobe Release Time		12		ns	
Input Voltage Range	±5.0			V	$V^- = -7.0V$
Differential Input Voltage Range	±5.0			V	
Output Resistance		200		Ω	
Positive Output Level		4.5	5.0	V	$V_{in} \geq 10mV$
Loaded Positive Output Level	2.5	3.5		V	$V_{in} \geq 10mV, I_O = 5mA$
Negative Output Level	−1.0	−0.5	0	V	$V_{in} \geq 10mV$
Strobed Output Level	−1.0		0	V	$V_{strobe} \leq 0.3V$
Output Sink Current	0.5	0.8		mA	$V_{in} \geq 10mV, V_{out} \geq 0$
Strobe Current		1.2	2.5	mA	$V_{strobe} = 100mV$
Positive Supply Current		8.6		mA	$V_{out} \leq 0$
Negative Supply Current		3.9		mA	
Power Consumption		130	230	mW	
The following specifications apply for $0°C \leq T \leq +70°C$:					
Input Offset Voltage (Note 5)			6.0 10	mV mV	$R_S \leq 200\Omega, V_{CM} = 0$ $R_S \leq 200\Omega$
Input Offset Current (Note 5)			25	uA	
Input Bias Current			150	uA	
Temperature Coefficient of Input Offset Voltage		5.0		uV/°C	
Voltage Gain	500				

DEFINITION OF TERMS:

LOGIC THRESHOLD VOLTAGE — The approximate voltage at the output of the comparator at which the loading logic circuitry changes its digital state.

INPUT OFFSET VOLTAGE* — The voltage between the input terminals when the output is at the logic threshold voltage. The input offset voltage may also be defined for the case where two equal resistances are inserted in series with the input leads.

INPUT OFFSET CURRENT* — The difference in the currents into the two input terminals with the output at the logic threshold voltage.

INPUT BIAS CURRENT* — The average of the two input currents.

INPUT VOLTAGE RANGE* — The range of voltage on the input terminals for which the comparator will operate within specifications.

DIFFERENTIAL INPUT VOLTAGE RANGE* — The range of voltage between the input terminals for which operation within specifications is assured.

VOLTAGE GAIN* — The ratio of the change in output voltage to the change in voltage between the input terminals producing it with the DC output level in the vicinity of the logic threshold voltage.

RESPONSE TIME* — The interval between the application of an input step function and the time when the output crosses the logic threshold voltage. The input step drives the comparator from some initial, saturated input voltage to an input level just barely in excess of that required to bring the output from saturation to the logic threshold voltage. This excess is referred to as the voltage overdrive.

STROBE RELEASE TIME* — The time required for the output to rise to the logic threshold voltage after the strobe terminal has been driven from the zero to the one logic level. Appropriate input conditions are assumed.

POSITIVE OUTPUT LEVEL* — The DC output voltage in the positive direction with the input voltage equal to or greater than a minimum specified amount.

NEGATIVE OUTPUT LEVEL* — The DC output voltage in the negative direction with the input voltage equal to or greater than a minimum specified amount.

OUTPUT SINK CURRENT — The maximum negative current that can be delivered by the comparator.

PEAK OUTPUT CURRENT — The maximum current that may flow into the output load without causing damage to the comparator.

OUTPUT RESISTANCE* — The resistance seen looking into the output terminal with the DC output level at the logic threshold voltage.

STROBED OUTPUT LEVEL* — The DC output voltage, independent of input voltage, with the voltage on the strobe terminal equal to or less than a minimum specified amount.

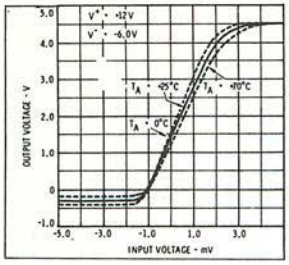
STROBE CURRENT — The maximum current drawn by the strobe terminal when it is at the zero logic level.

POWER CONSUMPTION — The DC power into the amplifier with no output load. The DC power will vary with signal level, but is specified as a maximum for the entire range of input-signal conditions.

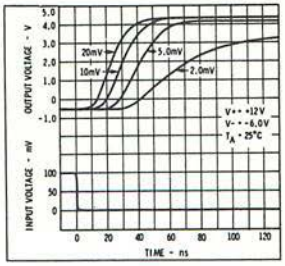
*These definitions apply for either side with the other disabled with the strobe.

TYPICAL PERFORMANCE CURVES MIC 711-5

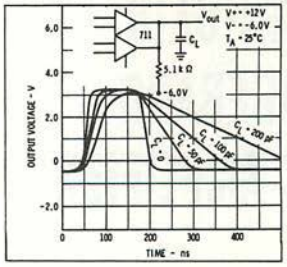
VOLTAGE TRANSFER CHARACTERISTIC



RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES

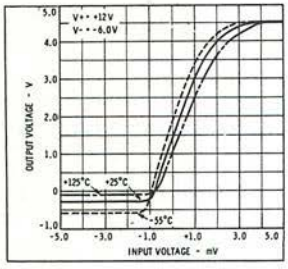


OUTPUT PULSE STRETCHING WITH CAPACITIVE LOADING

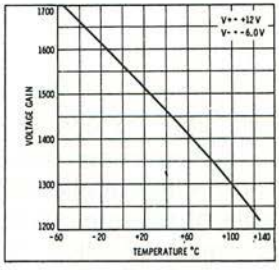


TYPICAL PERFORMANCE CURVES MIC 711-1

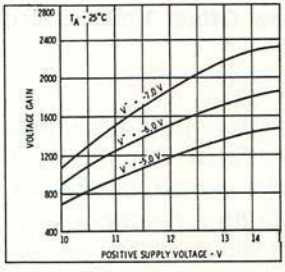
VOLTAGE TRANSFER CHARACTERISTIC



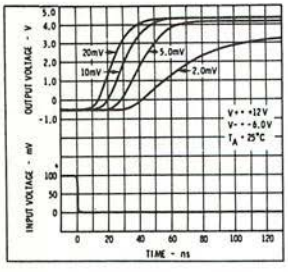
VOLTAGE GAIN AS A FUNCTION OF AMBIENT TEMPERATURE



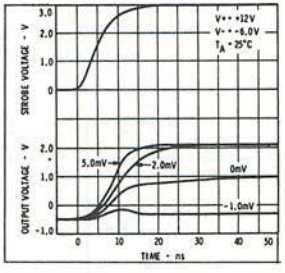
VOLTAGE GAIN AS A FUNCTION OF SUPPLY VOLTAGES



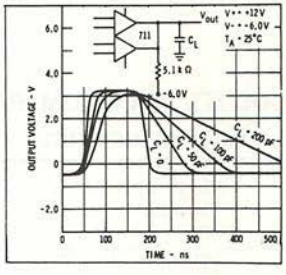
RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES



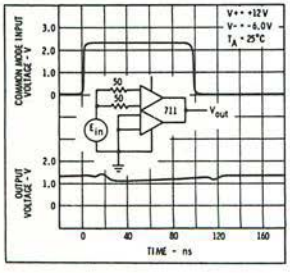
STROBE RELEASE TIME FOR VARIOUS INPUT OVERDRIVES



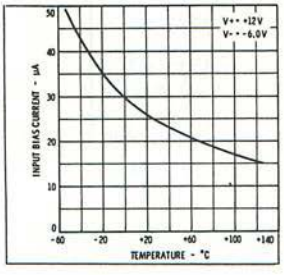
OUTPUT PULSE STRETCHING WITH CAPACITANCE LOADING



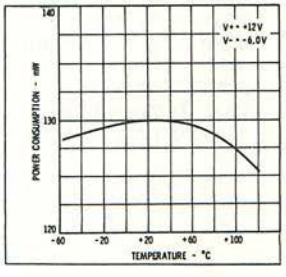
COMMON MODE PULSE RESPONSE



INPUT BIAS CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



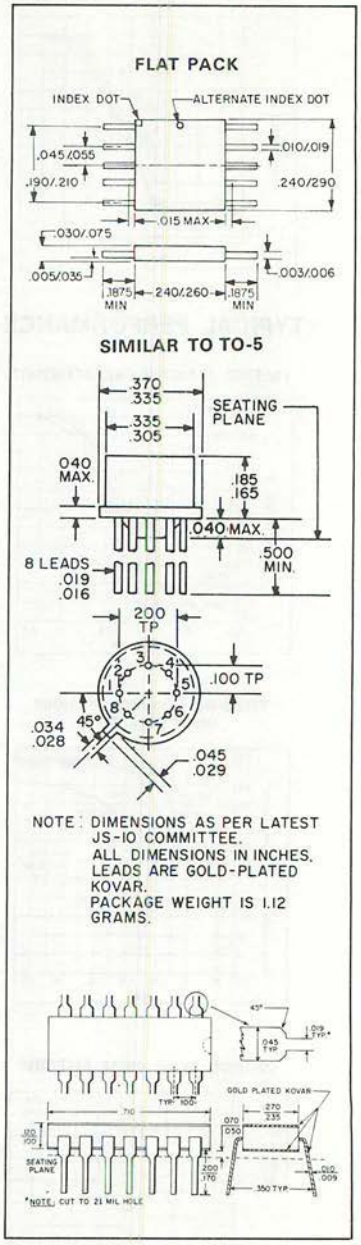
POWER CONSUMPTION AS A FUNCTION OF AMBIENT TEMPERATURE



HIGH-GAIN WIDEBAND DC AMPLIFIER

- **Low Offset Voltage**
- **High Voltage Gain**
- **Low Offset Voltage Drift**

The MIC 712 is a general purpose amplifier for use as an operational amplifier in high speed analog computers, a precision instrumentation amplifier or in other applications requiring a feedback amplifier capable of operating within the frequency ranges of DC to as high as 30MHz. The MIC 712 amplifier achieves low DC offset and low thermal drift, wideband operation and low power consumption as a result of ITT Planar epitaxial manufacturing process.



ABSOLUTE MAXIMUM RATINGS

CHARACTERISTICS		UNITS
Voltage between V^+ and V^- terminals	±21	Volts
Internal Power Dissipation (TO-5)	300	mW
(MIC 712-1 note 1, MIC 712-5 note 2)		
Differential Input Voltage	±5.0	Volts
Input Voltage	+1.5 to −6.0	Volts
Peak Output Voltage	50	mA
Storage Temperature Range	−65 to +150	°C
Operating Temperature Range		
MIC 712-1	−55 to +125	°C
MIC 712-5	0 to +70	°C
Lead Temperature (Soldering, 60 sec.)	300	°C

NOTES: (1) Rating applies for case temperatures to +125°C; derate linearly at 5.6mW/°C for ambient temperatures above +95°C.
(2) Rating applies for ambient temperatures to +70°C.

ELECTRICAL CHARACTERISTICS for MIC 712-1

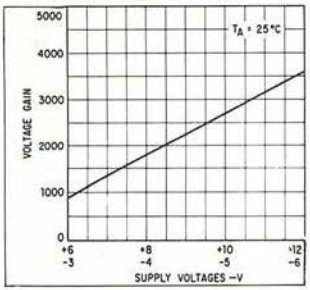
PARAMETER (See definitions)	MIN.	TYPE	MAX.	MIN.	TYPE	MAX	UNITS	CONDITIONS
	V+ = 12.0V, V− = 6.0V			V+ = 6.0V, V− = −3.0V				
Input Offset Voltage		0.5	2.0		0.7	3.0	mV	$R_s \leq 2k\Omega$
Input Offset Current		180	500		120	500	nA	
Input Bias Current		2.0	5.0		1.2	3.5	uA	
Input Resistance	16	40		22	67		kΩ	
Input Voltage Range	−4.0		+0.5	−1.5		+0.5	V	
Common Mode Rejection Ratio	80	100		80	100		dB	$R_s \leq 2k\Omega$, $f \leq 1kHz$
Large Signal Voltage Gain	2500	3600	6000					$R_L \geq 100k\Omega$, $V_{out} = \pm 5.0V$
				600	900	1500		R_L 100kΩ, $V_{out} = \pm 2.5V$
Output Resistance		200	500		300	700	Ω	
Supply Current		5.0	6.7		2.1	3.3	mA	$V_{out} = 0$
Power Consumption		90	120		19	30	mW	$V_{out} = 0$
Transient Response (Unity-Gain) Rise Time		25	120				ns	$C_l = 0.01$ uF, $R_l = 20\Omega$ $R_L \geq 100k\Omega$, $V_{in} = 10mW$
Overshoot		10	50				%	$C_L \leq 100pF$
Transient Response (x100 gain) Risetime		10	30				ns	$C_l = 50pF$, $R_L \geq 100k\Omega$ $V_{in} = 1$ mV
Overshoot		20	40				%	
The following specifications apply for $-55°C \leq T_A \leq +125°C$:								
Input Offset Voltage			3.0			4.0	mV	$R_s \leq 2k\Omega$
Average Temperature Coefficient of Input		2.5	10		3.5	15	uV/°C	$R_s = 50\Omega$ $T_A = 25°C$ to $T_A = +125°C$
Offset Voltage		2.0	10		3.0	15	uV/°C	$R_s = 50\Omega$ $T_A = 25°C$ to $T_A = -55°C$
Input Offset Current		80	500		50	500	nA	$T_A = +125°C$
		400	1500		280	1500	nA	$T_A = -55°C$
Average Temperature Coefficient of Input Offset Current		1.0	5.0		0.7	4.0	nA/°C	$T_A = 25°C$ to $T_A = +125°C$
		3.0	16		2.0	13	nA/°C	$T_A = 25°C$ to $T_A = -55°C$
Input Bias Current		4.3	10		2.6	7.5	uA	$T_A = -55°C$
Input Resistance	6.0			8.0			kΩ	
Common Mode Rejection Ratio	70	95		70	95		dB	$R_s \leq 2k\Omega$, $f \leq 1kHz$
Supply Voltage Rejection Ratio		75	200		75	200	uV/V	V+ = 12V, V− = −6Vto V+ = 6V, V− = −3V $R_s \leq 2k\Omega$
Large Signal Voltage Gain	2000		7000					$R_L \geq 100K\Omega$, $V_{out} = \pm 5.0V$
				500		1750		$R_L \geq 100k\Omega$, $V_{out} = \pm 2.5V$
Output Voltage Swing	±5.0	±5.3		±2.5	±2.7		V	$R_L \geq 100k\Omega$
	±3.5	±4.0		±1.5	±2.0		V	$R_L \geq 10k\Omega$
Supply Current		4.4	6.7		1.7	3.3	mA	$T_A = +125°C$, $V_{out} = 0$
		5.0	7.5		2.1	3.9	mA	$T_A = -55°C$, $V_{out} = 0$
Power Consumption		80	120		15	30	mW	$T_A = +125°C$, $V_{out} = 0$
		90	135		19	35	mW	$T_A = -55°C$, $V_{out} = 0$

ELECTRICAL CHARACTERISTICS for MIC 712-5

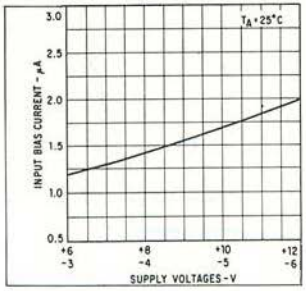
PARAMETER (see definitions)	V+ = 12.0V, V− = −6.0V MIN.	TYP.	MAX.	V+ = 6.0V, V− = −3.0V MIN.	TYP.	MAX.	UNITS	CONDITIONS
The following specifications apply for $T_A = 25°C$								
Input Offset Voltage		1.5	5.0		1.7	6.0	mV	$R_S \leqslant 2$ KΩ
Input Offset Current		0.5	2.0		0.3	2.0	μA	
Input Bias Current		2.5	7.5		1.5	5.0	μA	
Input Resistance	10	32		16	55		KΩ	
Input Voltage Range	−4.0		+0.5	−1.5		+0.5	V	
Common Mode Rejection Ratio	70	92		70	92		dB	$R_S \leqslant 2$KΩ, $f \leqslant 1$ KHz
Large Signal Voltage Gain	2000	3400	6000					$R_L \geqslant 100$ KΩ $V_{out} = \pm 5.0$ V
				500	800	1500		$R_L \geqslant 100$ KΩ $V_{out} = \pm 2.5$ V
Output Resistance		200	600		300	800	Ω	
Supply Current		5.0	6.7		2.1	3.3	mA	$V_{out} = 0$
Power Consumption		90	120		19	30	mW	$V_{out} = 0$
Transient Response (unity gain)								$C_1 = 0.01\mu F$, $R_1 = 20\Omega$ $R_L \geqslant 100$ KΩ $V_{in} = 10$ mV
Risetime		25	120				ns	
Overshoot		10	50				%	$C_L \leqslant 100$ pF
Transient Response (X100 gain)								$C_3 = 50$ pF $R_L \geqslant 100$ KΩ $V_{in} = 1$ mV
Risetime		10	30				ns	
Overshoot		20	40				%	
The following specifications apply for 0°C T_A +70°C								
Input Offset Voltage			6.5			7.5	mV	$R_S \leqslant 2$ KΩ
Average Temperature Coefficient of Input Offset Voltage		5.0	20		7.5	25	μV/°C	$R_S = 50\Omega$ $T_A = +70°C$ to $T_A = 0°C$
Input Offset Current			2.5			2.5	μA	
Average Temperature Coefficient of Input Offset Current		4.0 6.0	10 20		3.0 5.5	8.0 18	nA/°C nA/°C	$T_A = 25°C$ to $T_A = +70°C$ $T_A = 25°C$ to $T_A = 0°C$
Input Bias Current		4.0	12		2.7	8	μA	$T_A = 0°C$
Input Resistance	6.0	18		9.0	27		KΩ	
Common Mode Rejection Ratio	65	86		65	86		dB	$R_S \leqslant 2$ KΩ, $f \leqslant 1$ KHz
Supply Voltage Rejection Ratio		90	300		90	300	μV/V	V+ = 12V, V− = −6V to V+ = 6V, V− = −3V $R_S \leqslant 2$ KΩ
Large Signal Voltage Gain	1500		7000					$R_L \geqslant 100$ KΩ $V_{out} = \pm 5.0$V
				400		1750		$R_L \geqslant 100$KΩ $V_{out} = \pm 2.5$V
Output Voltage Swing	±5.0 ±3.5	±5.3 ±4.0		±2.5 ±1.5	±2.7 ±2.0		V V	$R_L \geqslant 100$ KΩ $R_L \geqslant 10$ KΩ
Supply Current		5.0	7.0		2.1	3.9	mA	$V_{out} = 0$
Power Consumption		90	125		19	35	mW	

TYPICAL PERFORMANCE CURVES MIC 712-1, 712-5

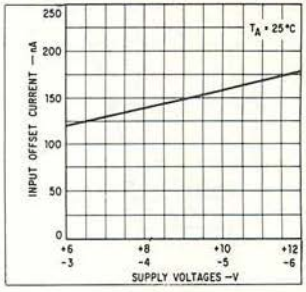
VOLTAGE GAIN AS A FUNCTION OF SUPPLY VOLTAGES



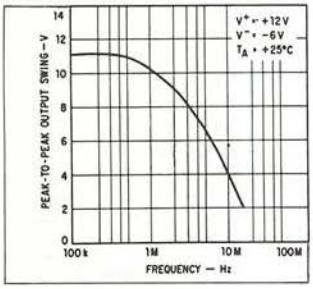
INPUT BIAS CURRENT AS A FUNCTION OF SUPPLY VOLTAGES



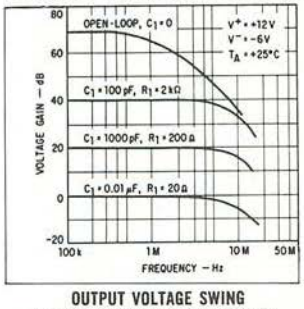
INPUT OFFSET CURRENT AS A FUNCTION OF SUPPLY VOLTAGES



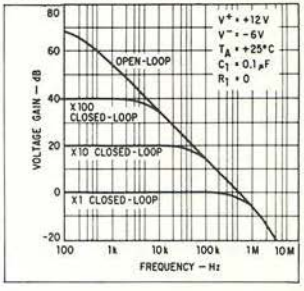
OUTPUT VOLTAGE SWING AS A FUNCTION OF FREQUENCY WITH LEAD-LAG COMPENSATION



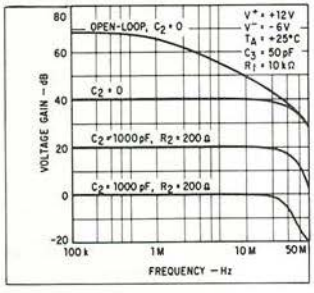
FREQUENCY RESPONSE FOR VARIOUS CLOSED-LOOP GAINS (LAG COMPENSATION)



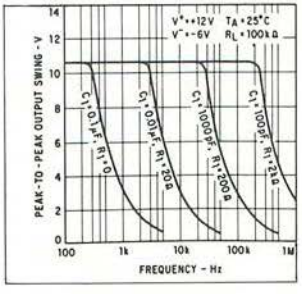
FREQUENCY RESPONSE WITH CONSERVATIVE COMPENSATION NETWORK



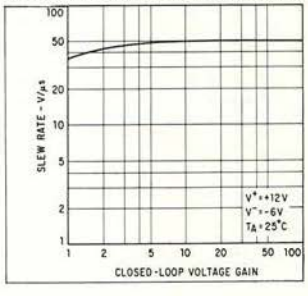
FREQUENCY RESPONSE FOR VARIOUS CLOSED-LOOP GAINS (LEAD-LAG COMPENSATION)



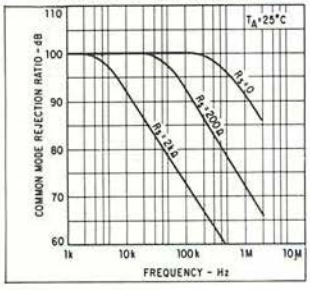
OUTPUT VOLTAGE SWING AS A FUNCTION OF FREQUENCY FOR VARIOUS LAG COMPENSATION NETWORKS



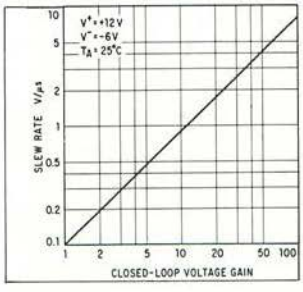
SLEW RATE AS A FUNCTION OF CLOSED-LOOP VOLTAGE GAIN (LEAD-LAG COMPENSATION)



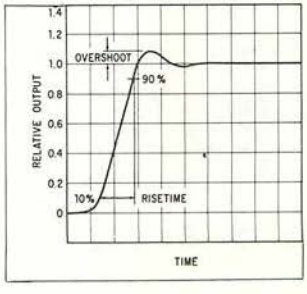
COMMON MODE REJECTION RATIO AS A FUNCTION OF FREQUENCY



SLEW RATE AS A FUNCTION OF CLOSED-LOOP VOLTAGE GAIN (LAG COMPENSATION)

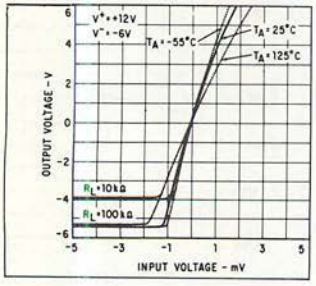


TRANSIENT RESPONSE

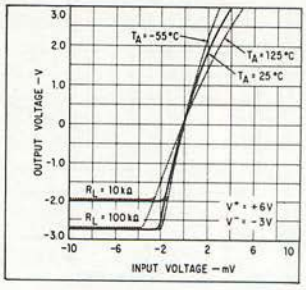


TYPICAL PERFORMANCE CURVES MIC 712-1

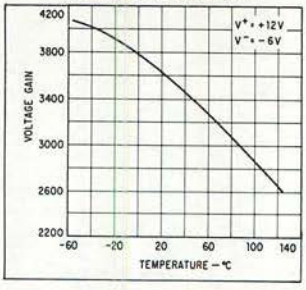
VOLTAGE TRANSFER CHARACTERISTIC



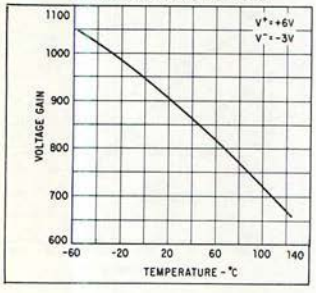
VOLTAGE TRANSFER CHARACTERISTIC



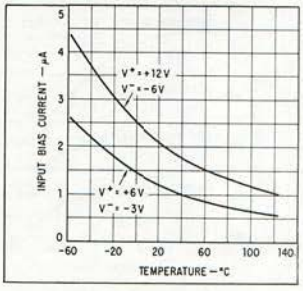
VOLTAGE GAIN AS A FUNCTION OF AMBIENT TEMPERATURE



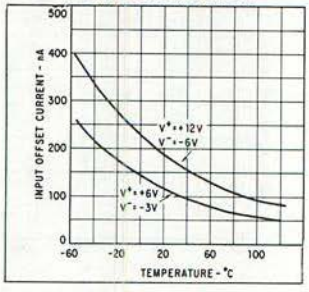
VOLTAGE GAIN AS A FUNCTION OF AMBIENT TEMPERATURE



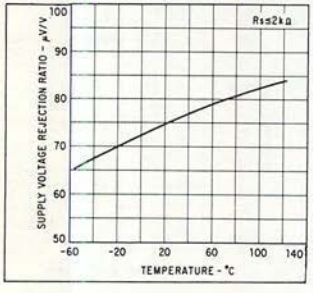
INPUT BIAS CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



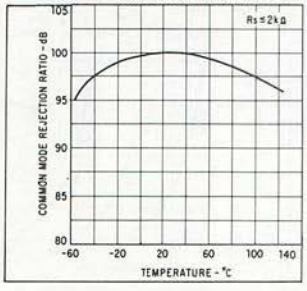
INPUT OFFSET CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



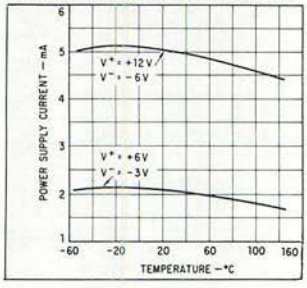
SUPPLY VOLTAGE REJECTION RATIO AS A FUNCTION OF AMBIENT TEMPERATURE



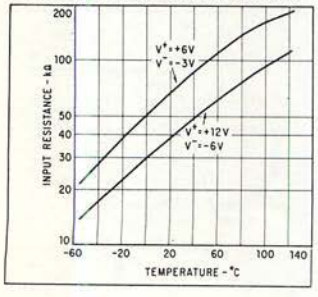
COMMON MODE REJECTION RATIO AS A FUNCTION OF AMBIENT TEMPERATURE



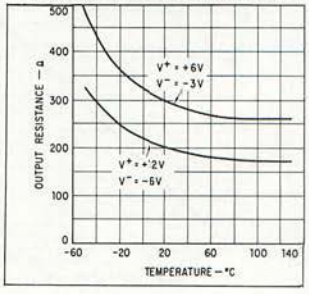
POWER SUPPLY CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



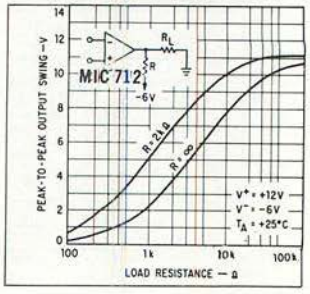
INPUT RESISTANCE AS A FUNCTION OF AMBIENT TEMPERATURE



OUTPUT RESISTANCE AS A FUNCTION OF AMBIENT TEMPERATURE

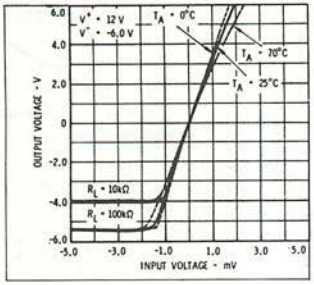


OUTPUT VOLTAGE SWING AS A FUNCTION OF LOAD RESISTANCE

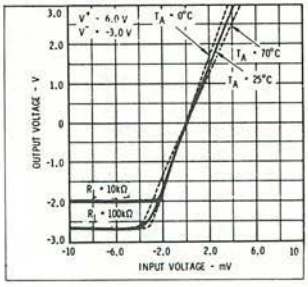


TYPICAL PERFORMANCE CURVES MIC 712-5

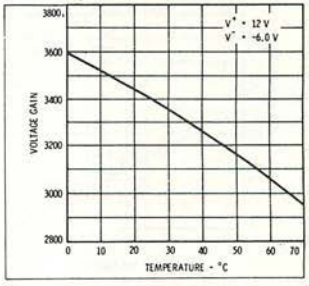
VOLTAGE TRANSFER CHARACTERISTIC



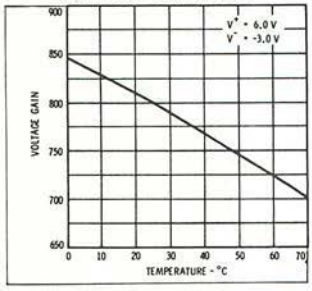
VOLTAGE TRANSFER CHARACTERISTIC



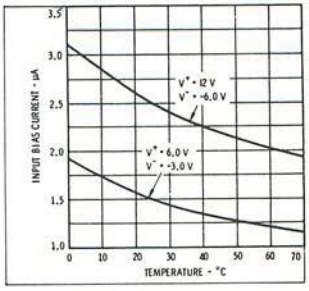
VOLTAGE GAIN AS A FUNCTION OF AMBIENT TEMPERATURE



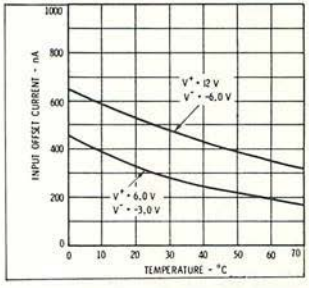
VOLTAGE GAIN AS A FUNCTION OF AMBIENT TEMPERATURE



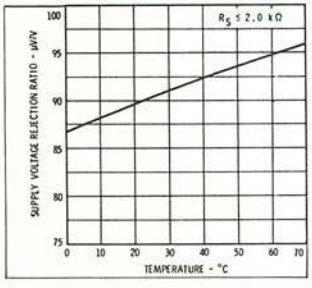
INPUT BIAS CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



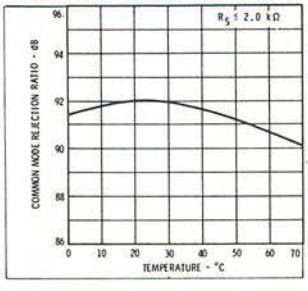
INPUT OFFSET CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



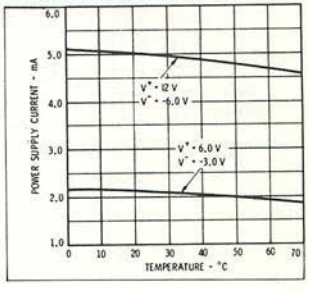
SUPPLY VOLTAGE REJECTION RATIO AS A FUNCTION OF AMBIENT TEMPERATURE



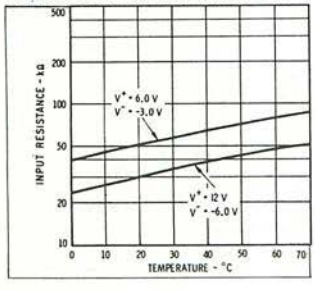
COMMON MODE REJECTION RATIO AS A FUNCTION OF AMBIENT TEMPERATURE



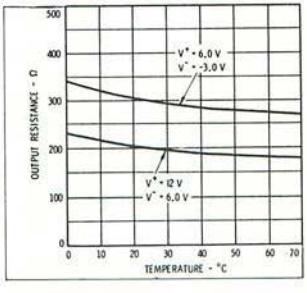
POWER SUPPLY CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



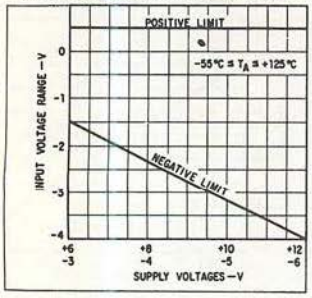
INPUT RESISTANCE AS A FUNCTION OF AMBIENT TEMPERATURE



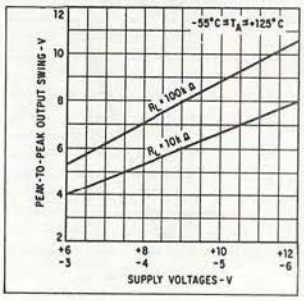
OUTPUT RESISTANCE AS A FUNCTION OF AMBIENT TEMPERATURE



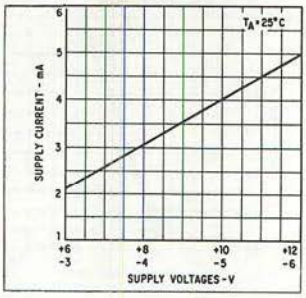
INPUT VOLTAGE RANGE AS A FUNCTION OF SUPPLY VOLTAGES



OUTPUT VOLTAGE SWING AS A FUNCTION OF SUPPLY VOLTAGES

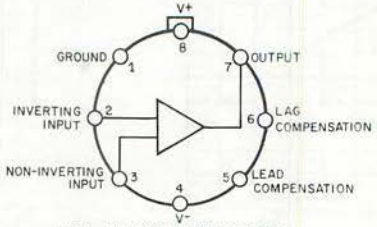


SUPPLY CURRENT AS A FUNCTION OF SUPPLY VOLTAGES



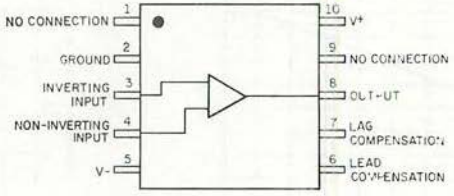
CONNECTION DIAGRAMS

TO-5 (Top View)

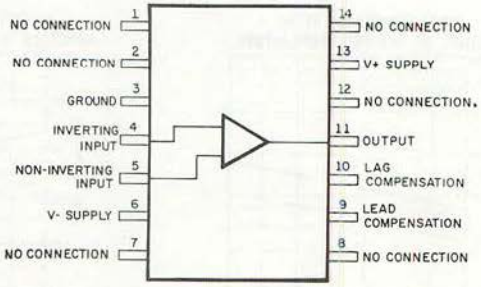


NOTE: PIN 4 CONNECTED TO CASE

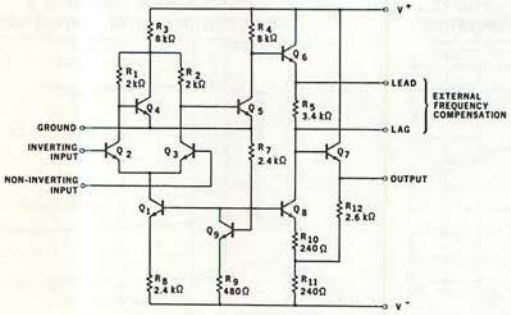
FLAT PACK (Top View)



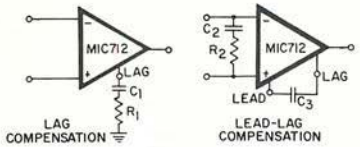
DUAL IN-LINE



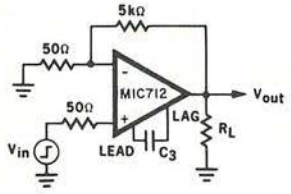
SCHEMATIC DIAGRAM



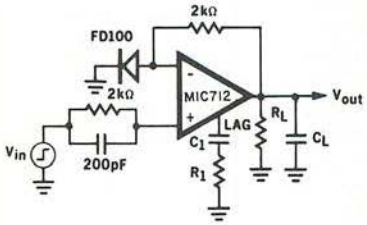
FREQUENCY COMPENSATION CIRCUITS



TRANSIENT RESPONSE TEST CIRCUITS



X100 AMPLIFIER (LEAD COMPENSATION)



UNITY-GAIN AMPLIFIER (LAG COMPENSATION)

SPECIAL ORDERING CODE

Temperature Range:
1 = −55° +125°C
5 = 0° to +70C

Package:
B = .250" X .250" Flat Pack
C = 8-lead TO-5
D = 14-Lead Dual-In-Line

Example:
MIC712-1C means operating temperature range of −55° to +125°C, supplied in a TO-5 package.

DEFINITION OF TERMS

INPUT OFFSET VOLTAGE — That voltage which must be applied between the input terminals to obtain zero output voltage. The input offset voltage may also be defined for the case where two equal resistances are inserted in series with the input leads.

INPUT QFFSET CURRENT — The difference in the currents into the two input terminals with the output at zero volts.

INPUT RESISTANCE — The resistance looking into either input terminal with the other grounded.

INPUT BIAS CURRENT — The average of the two input currents.

INPUT VOLTAGE RANGE — The range of voltage which, if exceeded on either input terminal, could cause the amplifier to cease functioning properly.

INPUT COMMON MODE REJECTION RATIO — The ratio of the input voltage range to the maximum change in input offset voltage over this range.

SUPPLY VOLTAGE REJECTION RATIO — The ratio of the change in input offset voltage to the change in supply voltage producing it.

LARGE-SIGNAL VOLTAGE GAIN — The ratio of the maximum output voltage swing with load to the change in input voltage required to drive the output from zero to this voltage.

OUTPUT VOLTAGE SWING — The peak output swing, referred to zero, that can be obtained without clipping.

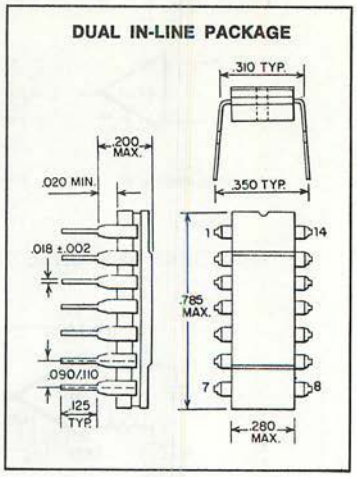
OUTPUT RESISTANCE — The resistance seen looking into the output terminal with the output at null. This parameter is defined only under small signal conditions at frequencies above a few hundred cycles to eliminate the influence of drift and thermal feedback.

POWER CONSUMPTION — The DC power required to operate the amplifier with the output at zero and with no load current.

TRANSIENT RESPONSE — The closed-loop step-function response of the amplifier under small-signal conditions.

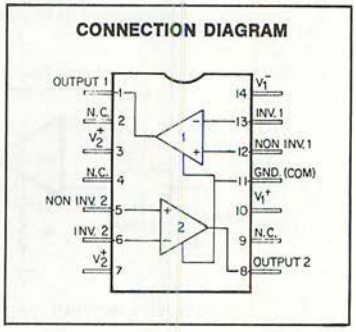
PEAK OUTPUT CURRENT — The maximum current that may flow in the output load without causing damage to the unit.

DUAL HIGH SPEED DIFFERENTIAL COMPARATOR



- **Better Temperature Tracking**
- **Low Offset Voltage**
- **Low Offset Current**
- **High Voltage Gain**
- **Fast Response Time**

The ITT MIC720 differential voltage dual comparator, offering high accuracy and fast response times, consists of two separate MIC710 high speed differential comparators. The entire circuit is contained on one silicon chip and is manufactured using the ITT Planar Epitaxial process. The output of the MIC720 is compatible with all integrated logic forms. The MIC720 can also be used as a variable threshold Schmidt trigger, a pulse height discriminator, a memory sense amplifier, a high noise immunity line receiver, or in high speed A-D conversion and multivibrator functions.



ABSOLUTE MAXIMUM RATINGS

CHARACTERISTICS	UNITS
Positive Supply Voltage	+14.0 V
Negative Supply Voltage	−7.0 V
Peak Output Current	10 mA
Differential Input Voltage	±5.0 V
Input Voltage	±7.0 V
Internal Power Dissipation	300 mW
(MIC720-1 Note 1, MIC720-5 Note 2)	200 mW
Operating Temperature Range MIC720-1	−55° to +125°C
MIC720-5	0° to +70°C
Storage Temperature Range	−65° to +150°C
Lead Temperature (Soldering, 60 sec.)	300°C

ELECTRICAL CHARACTERISTICS for MIC 720-1 (T = +25°C, V = 12.0V, V = −6.0V unless otherwise specified)

PARAMETER (see definitions)	MIN.	TYP.	MAX.	UNITS	CONDITIONS (Note 4)
Input Offset Voltage		0.6	2.0	mV	Rs ≦ 200Ω
Input Offset Current		0.75	3.0	uA	
Input Bias Current		13	20	uA	
Voltage Gain	1250	1700			
Output Resistance		200		Ω	
Output Sink Current	2.0	2.5		mA	$\Delta V_{in} \geqq 5mV$, $V_{out} = 0$
Response Time (Note 3)		40		ns	
The following specifications apply for −55°C ≦ T$_A$ ≦ +125°C:					
Input Offset Voltage			3.0	mV	Rs ≦ 200Ω
Average Temperature Coefficient		3.5	10	uV/°C	Rs = 50Ω, TA = 25°C to TA = +125°C
of Input Offset Voltage		2.7	10	uV/°C	Rs50Ω, TA = 25°C to TA = −55°C
Input Offset Current		0.25	3.0	uA	TA = +125°C
		1.8	7.0	uA	T$_A$ = −55°C
Average Temperature Coefficient		5.0	25	nA/°C	T$_A$ = 25°C to T$_A$ = +125°C
of Input Offset Current		15	75	nA/°C	T$_A$ = 25°C to T$_A$ = −55°C
Input Bias Current		27	45	uA	T$_A$ = −55°C
Input Voltage Range	±5.0			V	V = −7.0V
Common Mode Rejection Ratio	80	100		dB	Rs ≦ 200Ω
Differential Input Voltage Range	±5.0			V	
Voltage Gain	1000				
Positive Output Level	2.5	3.2	4.0	V	$V_{in} \geqq 5mV$, $0 \leqq I_{out} \leqq 5.0mA$
Negative Output Level	−1.0	−0.5	0	V	$\Delta V_{in} \geqq 5mV$
Output Sink Current	0.5	1.7		mA	T$_A$ = +125°C, $\Delta V_{in} \geqq 5mV$, $V_{out} = 0$
	1.0	2.3		mA	T$_A$ = −55°C, $\Delta V_{in} \geqq 5mV$, $V_{out} = 0$
Positive Supply Current		5.2	9.0	mA	$V_{out} \leqq 0$
Negative Supply Current		4.6	7.0	mA	
Power Consumption		90	150	mW	

NOTES:

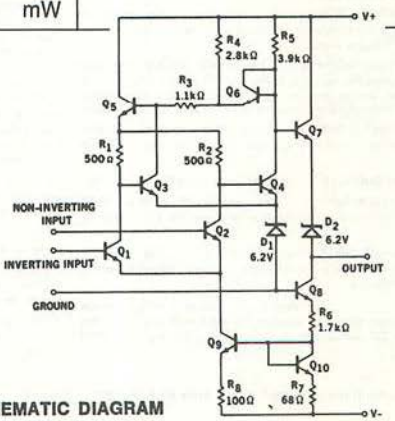
(1) For DIP pack derate at 4.4mW/°C for case temperatures above +115°C; derate linearly at 3.3mW/°C for ambient temperatures above +100°C.

(2) Ratings apply for ambient temperatures to +70°C.

(3) The response time specified (see definitions) is for a 100-mV input step with 5-mV overdrive.

(4) The input offset voltage and input offset current (see definitions) are specified for a logic threshold voltage of 1.8V at −55°C, 1.4V at +25°C and 1.0V at +125°C.

(5) The input offset voltage and input offset current (see definitions) are specified for a logic threshold voltage of 1.5V at 0°C, 1.4V at +25°C and 1.2V at +70°C.



½ CIRCUIT — SCHEMATIC DIAGRAM

ELECTRICAL CHARACTERISTICS for MIC 720-5 (TA = 25°C, V = 12.0V, V = −6.0V unless otherwise specified)

PARAMETER (see definitions)	MIN.	TYP.	MAX.	UNITS	CONDITIONS (Note 5)
Input Offset Voltage		1.6	5.0	mV	$R_S \leqslant 200\Omega$
Input Offset Current		1.8	5.0	uA	
Input Bias Current		16	25	uA	
Voltage Gain	1000	1500			
Output Resistance		200		Ω	
Output Sink Current	1.6	2.5		mA	$\Delta V_{in} \geqslant 5mV$, $V_{out} = 0$
Response Time (Note 3)		40		ns	
The following specifications apply for $0°C \leqslant TA \leqslant +70°C$:					
Input Offset Voltage			6.5	mV	$R_S \leqslant 200\Omega$
Average Temperature Coefficient of Input Offset Voltage		5.0	20	uV/°C	$R_S = 50\Omega$, TA = 0°C to TA = +70°C
Input Offset Current			7.5	uA	
Average Temperature Coefficient of Input Offset Current		15	50	nA/°C	TA = 25°C to TA = +70°C
		24	100	nA/°C	TA = 25°C to TA = 0°C
Input Bias Current		25	40	uA	TA = 0°C
Input Voltage Range	±5.0			V	V = −7.0V
Common Mode Rejection Ratio	70	98		dB	$R_S \leqslant 200$
Differential Input Voltage Range	±5.0			V	
Voltage Gain	800				
Positive Output Level	2.5	3.2	4.0	V	$\Delta V_{in} \geqslant 5mV$, $0 \leqslant I_{out} \leqslant 5.0mA$
Negative Output Level	−1.0	−0.5	0	V	$\Delta V_{in} \geqslant 5mV$
Output Sink Current	0.5			mA	$\Delta V_{in} \geqslant 5mV$, $V_{out} = 0$
Positive Supply Current		5.2	9.0	mA	$V_{out} \leqslant 0$
Negative Supply Current		4.6	7.0	mA	
Power Consumption		90	150	mW	

DEFINITION OF TERMS:

LOGIC THRESHOLD VOLTAGE — The approximate voltage at the output of the comparator at which the loading logic circuitry changes its digital state.

INPUT OFFSET VOLTAGE* — The voltage between the input terminals when the output is at the logic threshold voltage. The input offset voltage may also be defined for the case where two equal resistances are inserted in series with the input leads.

INPUT OFFSET CURRENT* — The difference in the currents into the two input terminals with the output at the logic threshold voltage.

INPUT BIAS CURRENT* — The average of the two input currents.

INPUT VOLTAGE RANGE* — The range of voltage on the input terminals for which the comparator will operate within specifications.

DIFFERENTIAL INPUT VOLTAGE RANGE* — The range of voltage between the input terminals for which operation within specifications is assured.

VOLTAGE GAIN* — The ratio of the change in output voltage to the change in voltage between the input terminals producing it with the DC output level in the vicinity of the logic threshold voltage.

RESPONSE TIME* — The interval between the application of an input step function and the time when the output crosses the logic threshold voltage. The input step drives the comparator from some initial, saturated input voltage to an input level just barely in excess of that recuired to bring the output from saturation to the logic threshold voltage. This excess is referred to as the voltage overdrive.

STROBE RELEASE TIME* — The time required for the output to rise to the logic threshold voltage after the strobe terminal has been driven from the zero to the one logic level. Appropriate input conditions are assumed.

POSITIVE OUTPUT LEVEL* — The DC output voltage in the positive direction with the input voltage equal to or greater than a minimum specified amount.

NEGATIVE OUTPUT LEVEL* — The DC output voltage in the negative direction with the input voltage equal to or greater than a minimum specified amount.

OUTPUT SINK CURRENT — The maximum negative current that can be delivered by the comparator.

PEAK OUTPUT CURRENT — The maximum current that may flow into the output load without causing damage to the comparator.

OUTPUT RESISTANCE* — The resistance seen looking into the output terminal with the DC output level at the logic threshold voltage.

STROBED OUTPUT LEVEL* — The DC output voltage, independent of input voltage, with the voltage on the strobe terminal equal to or less than a minimum specified amount.

STROBE CURRENT — The maximum current drawn by the strobe terminal when it is at the zero logic level.

POWER CONSUMPTION — The DC power into the amplifier with no output load. The DC power will vary with signal level, but is specified as a maximum for the entire range of input-signal conditions.

*These definitions apply for either side with the other disabled with the strobe.

SPECIAL ORDERING CODE

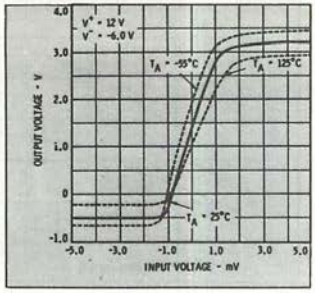
Temperature Range:
1 = −55° +125°C
5 = 0° to +70°C

Case Style:
D = Ceramic Dual In-Line, 16 leads, add "D" following last digit.

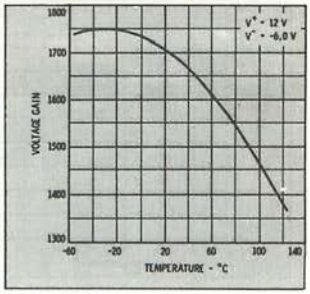
Example:
MIC720-1D is −55°C to +125°C temperature range in Ceramic Dual In-Line package.

TYPICAL CHARACTERISTICS MIC 720-1 (T = +25°C, V = 12.0V, V = −6.0V unless otherwise specified)

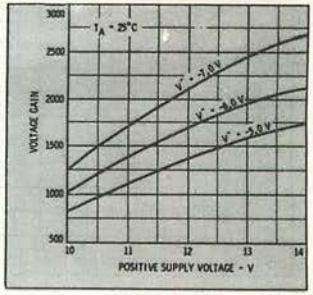
VOLTAGE TRANSFER CHARACTERISTIC



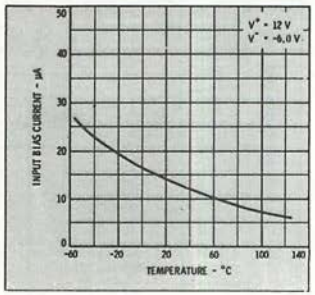
VOLTAGE GAIN AS A FUNCTION OF AMBIENT TEMPERATURE



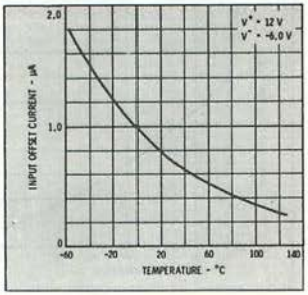
VOLTAGE GAIN AS A FUNCTION OF SUPPLY VOLTAGES



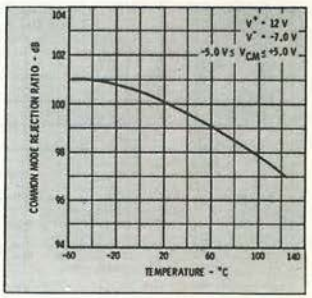
INPUT BIAS CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



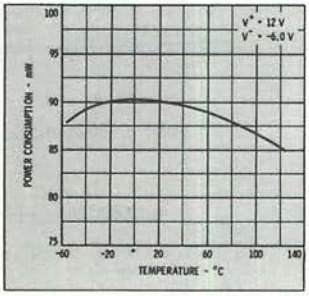
INPUT OFFSET CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



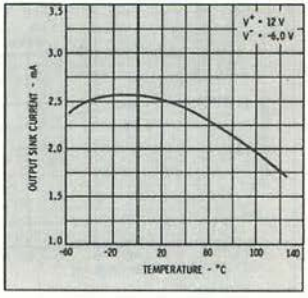
COMMON MODE REJECTION RATIO AS A FUNCTION OF AMBIENT TEMPERATURE



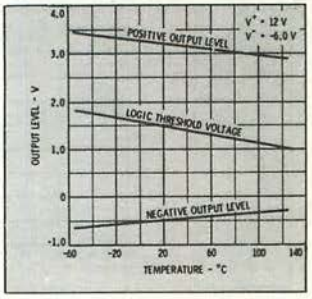
POWER CONSUMPTION AS A FUNCTION OF AMBIENT TEMPERATURE



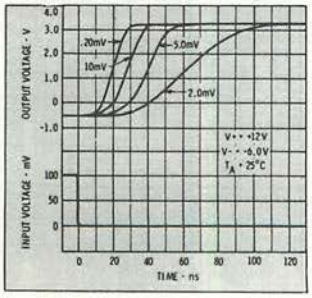
OUTPUT SINK CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



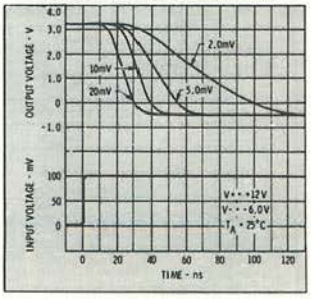
OUTPUT VOLTAGE LEVELS AS A FUNCTION OF AMBIENT TEMPERATURE



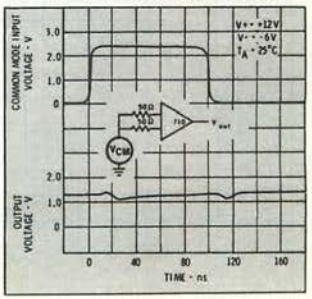
RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES



RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES

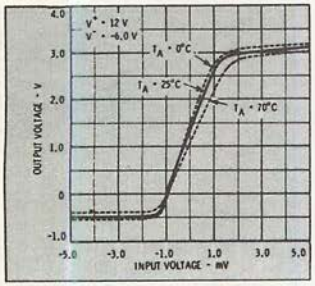


COMMON MODE PULSE RESPONSE

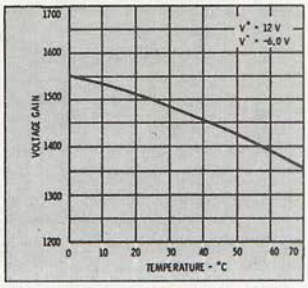


TYPICAL CHARACTERISTICS MIC 720-5 (TA = 25°C, V = 12.0V, V = −6.0V unless otherwise specified)

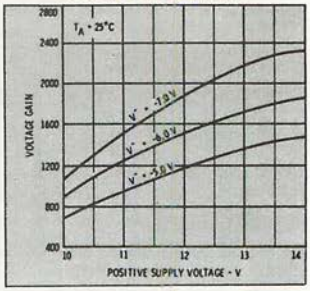
VOLTAGE TRANSFER CHARACTERISTIC



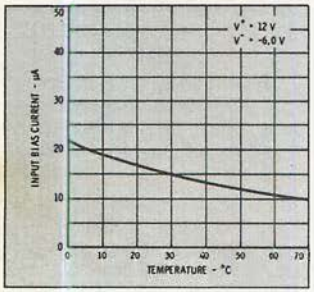
VOLTAGE GAIN AS A FUNCTION OF AMBIENT TEMPERATURE



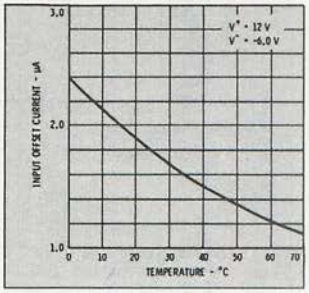
VOLTAGE GAIN AS A FUNCTION OF SUPPLY VOLTAGES



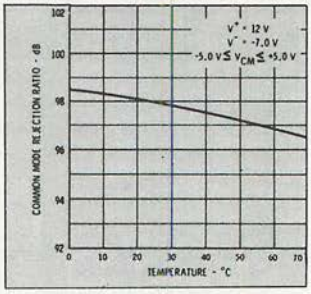
INPUT BIAS CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



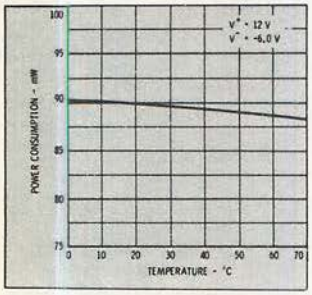
INPUT OFFSET CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



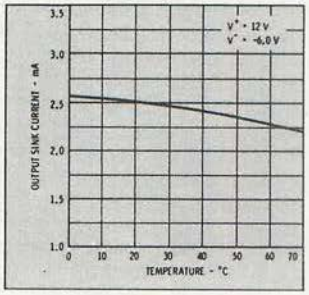
COMMON MODE REJECTION RATIO AS A FUNCTION OF AMBIENT TEMPERATURE



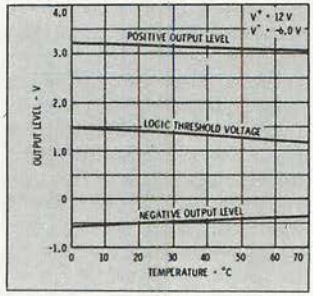
POWER CONSUMPTION AS A FUNCTION OF AMBIENT TEMPERATURE



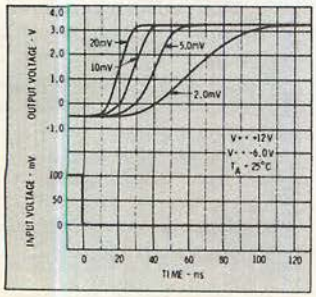
OUTPUT SINK CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



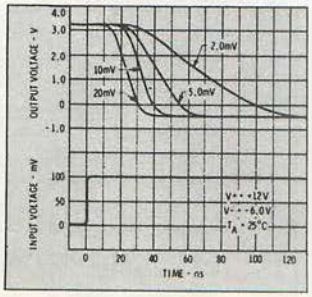
OUTPUT VOLTAGE LEVELS AS A FUNCTION OF AMBIENT TEMPERATURE



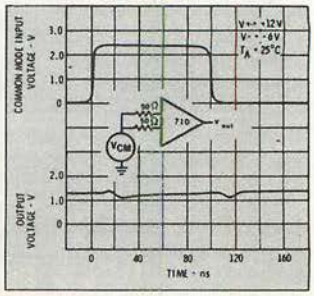
RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES



RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES



COMMON MODE PULSE RESPONSE

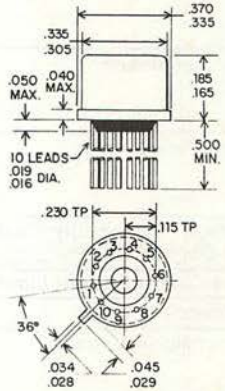


PRECISION VOLTAGE REGULATOR

- **Positive or Negative Supply Operation**
- **Series, Shunt, Switching or Floating Operation**
- **.01% Line and Load Regulation**
- **Output Voltage Adjustable From 2 to 37 Volts**
- **Output Current to 150 mA Without External Pass Transistor**

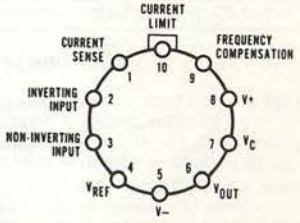
The MIC723 is a monolithic voltage regulator constructed on a single silicon chip using the epitaxial process. The device consists of a temperature compensated reference amplifier, error amplifier, power series pass transistor and current limit circuitry. Additional NPN or PNP pass elements may be used when output currents exceeding 150 mA are required. Provisions are made for adjustable current limiting and remote shutdown. In addition to the above, the device features low standby current drain, low temperature drift and high ripple rejection. The MIC723 is intended for use with positive or negative supplies as a series, shunt, switching or floating regulator. Applications include laboratory power supplies, isolation regulators for low level data amplifiers, logic card regulators, small instrument power supplies, airborne systems and other power supplies for digital and linear circuits.

DIMENSIONS



NOTES: LEADS ARE GOLD-PLATED KOVAR
PACKAGE WEIGHT IS 1.32 GRAMS

CONNECTION DIAGRAMS
TOP VIEWS



Note: On metal can, pin 5 is connected to case

ABSOLUTE MAXIMUM RATINGS

CHARACTERISTICS	MIC723-1	MIC723-5	UNITS
Pulse Voltage from V^+ to V^- (50 msec)	50		V
Voltage from V^+ to V^-		40	V
Continuous Voltage from V^+ to V^-	40		V
Maximum Output Current		150	mA
Input-Output Voltage Differential	40	40	V
Current from V_Z	25	25	mA
Current from V_{REF}	15	15	mA
Internal Power Dissipation — Metal Can (Note 1)	800	800	mW
Internal Power Dissipation — DIP (Note 1)	900	900	mW
Operating Temperature Range	−55 to +125	0 to +70	°C
Storage Temperature Range	−65 to +150	−65 to +150	°C
Lead Temperature (Soldering, 60 sec.)	300	300	°C

ELECTRICAL CHARACTERISTICS for MIC723-1 (Note 2)

PARAMETER (see definitions)	MIN.	TYP.	MAX.	UNITS	CONDITIONS
Line Regulation		.01	0.1	% V_{OUT}	V_{IN} = 12 V to V_{IN} = 15 V
		.02	0.2	% V_{OUT}	V_{IN} = 12 V to V_{IN} = 40 V
			0.3	% V_{OUT}	−55°C ≤ T_A ≤ +125°C, V_{IN} = 12 V to V_{IN} = 15 V
Load Regulation		.03	0.15	% V_{OUT}	I_L = 1 mA to I_L = 50 mA
			0.6	% V_{OUT}	−55°C ≤ T_A ≤ +125°C, I_L = 1 mA to I_L = 50 mA
Ripple Rejection		74		dB	f = 50 Hz to 10 kHz, C_{REF} = 0
		86		dB	f = 50 Hz to 10 kHz, C_{REF} = 5 μF
Average Temperature Coefficient of Output Voltage		.002	.015	%/°C	−55°C ≤ T_A ≤ +125°C
Short Circuit Current Limit		65		mA	R_{SC} = 10 Ω, V_{OUT} = 0
Reference Voltage	6.95	7.15	7.35	V	
Output Noise Voltage		20		μV_{rms}	BW = 100 Hz to 10 kHz, C_{REF} = 0
		2.5		μV_{rms}	BW = 100 Hz to 10 kHz, C_{REF} = 5 μF
Long Term Stability		0.1		%/1000 hrs	
Standby Current Drain		2.3	3.5	mA	I_L = 0, V_{IN} = 30 V
Input Voltage Range	9.5		40	V	
Output Voltage Range	2.0		37	V	
Input-Output Voltage Differential	3.0		38	V	

DEFINITION OF TERMS

LINE REGULATION — The percentage change in output voltage for a specified change in input voltage.

LOAD REGULATION — The percentage change in output voltage for a specified change in load current.

RIPPLE REJECTION — The ratio of the peak to peak input ripple voltage to the peak to peak output ripple voltage.

AVERAGE TEMPERATURE COEFFICIENT OF OUTPUT VOLTAGE — The percentage change in output voltage for a specified change in ambient temperature.

SHORT CIRCUIT CURRENT LIMIT — The output current of the regulator with the output shorted to the negative supply.

REFERENCE VOLTAGE — The output of the reference amplifier measured with respect to the negative supply.

OUTPUT NOISE VOLTAGE — The rms output noise voltage with constant load and no input ripple.

STANDBY CURRENT DRAIN — The supply current drawn by the regulator with no output load and no reference voltage load.

INPUT VOLTAGE RANGE — The range of supply voltage over which the regulator will operate.

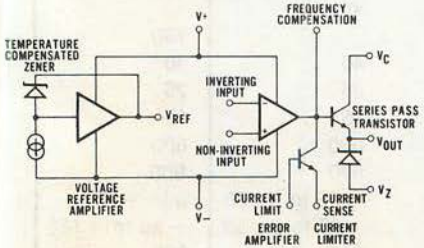
OUTPUT VOLTAGE RANGE — The range of output voltage over which the regulator will operate.

INPUT-OUTPUT VOLTAGE DIFFERENTIAL — The range of voltage difference between the supply voltage and the regulated output voltage over which the regulator will operate.

SENSE VOLTAGE — The voltage between current sense and current limit terminals necessary to cause current limiting.

TRANSIENT RESPONSE — The closed-loop step function response of the regulator under small-signal conditions.

EQUIVALENT CIRCUIT



NOTES:

(1) Derate metal can package at 6.8 mW/°C and dual-in-line package at 9 mW/°C for operation at ambient temperatures above 25°C.

(2) Unless otherwise specified, T_A = 25°C, V_{IN} = V^+ = V_C = 12 V, V^- = 0, V_{out} = 5 V, I_L = 1 mA, R_{SC} = 0, C_1 = 100 pF, C_{REF} = 0 and divider impedance as seen by error amplifier ≤ 10 KΩ connected as shown in Fig. 1.

(3) L_1 is 40 turns of #20 enameled copper wire wound on Ferroxcube P36/22-3B7 pot core or equivalent with 0.009" air gap.

(4) Figures in parentheses may be used if R_1/R_2 divider is placed on opposite of error amp.

(5) Replace R_1/R_2 in figures with divider shown in figure 13.

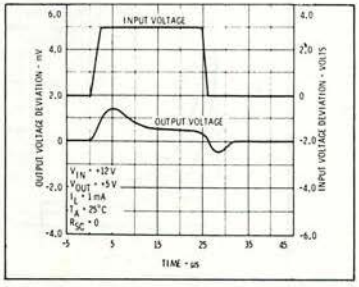
(6) V^+ must be connected to a +3 V or greater supply.

ELECTRICAL CHARACTERISTICS for MIC723-5 (Note 2)

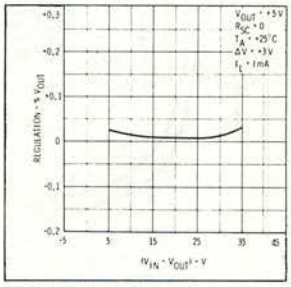
PARAMETER (see definitions)	MIN.	TYP.	MAX.	UNITS	CONDITIONS
Line Regulation		.01	0.1	% V_{OUT}	V_{IN} = 12 V to V_{IN} = 15 V
		0.1	0.5	% V_{OUT}	V_{IN} = 12 V to V_{IN} = 40 V
			0.3	% V_{OUT}	0°C ≤ T_A ≤ 70°C, V_{IN} = 12 V to V_{IN} = 15 V
Load Regulation		.03	0.2	% V_{OUT}	I_L = 1 mA to I_L = 50 mA
			0.6	% V_{OUT}	0°C ≤ T_A ≤ 70°C, I_L = 1 mA to I_L = 50 mA
Ripple Rejection		74		dB	f = 50 Hz to 10 kHz, C_{REF} = 0
		86		dB	f = 50 Hz to 10 kHz, C_{REF} = 5 μF
Average Temperature Coefficient of Output Voltage		.003	.015	%/°C	0°C ≤ T_A ≤ 70°C
Short Circuit Current Limit		65		mA	R_{SC} = 10 Ω, V_{OUT} = 0
Reference Voltage	6.80	7.15	7.50	V	
Output Noise Voltage		20		μV_{rms}	BW = 100 Hz to 10 kHz, C_{REF} = 0
		2.5		μV_{rms}	BW = 100 Hz to 10 kHz, C_{REF} = 5 μF
Long Term Stability		0.1		%/1000 hrs	
Standby Current Drain		2.3	4.0	mA	I_L = 0, V_{IN} = 30 V
Input Voltage Range	9.5		40	V	
Output Voltage Range	2.0		37	V	
Input-Output Voltage Differential	3.0		38	V	

TYPICAL PERFORMANCE CURVES MIC723-1, 723-5

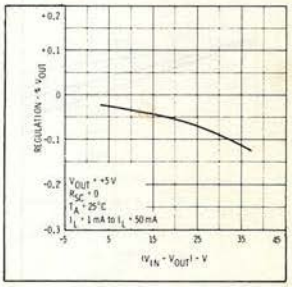
LINE TRANSIENT RESPONSE



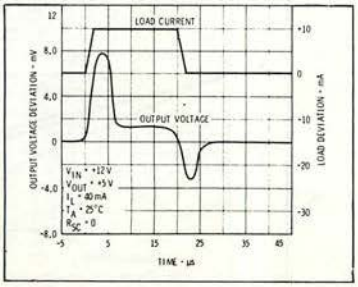
LINE REGULATION AS A FUNCTION OF INPUT-OUTPUT VOLTAGE DIFFERENTIAL



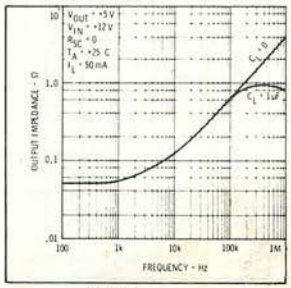
LOAD REGULATION AS A FUNCTION OF INPUT-OUTPUT VOLTAGE DIFFERENTIAL



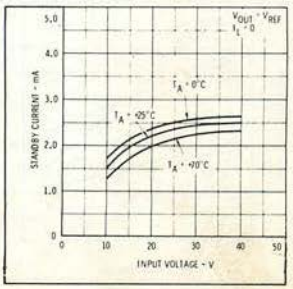
LOAD TRANSIENT RESPONSE



OUTPUT IMPEDANCE AS A FUNCTION OF FREQUENCY

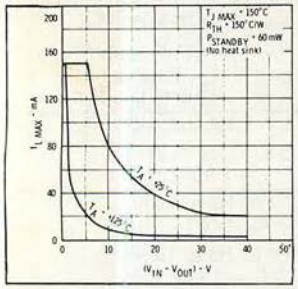


STANDBY CURRENT DRAIN AS A FUNCTION OF INPUT VOLTAGE

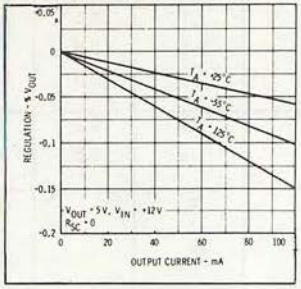


TYPICAL PERFORMANCE CURVES MIC723-1

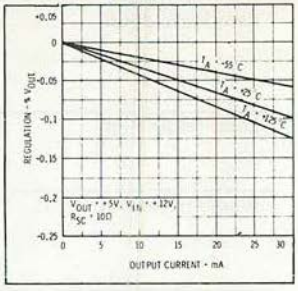
MAXIMUM LOAD CURRENT AS A FUNCTION OF INPUT-OUTPUT VOLTAGE DIFFERENTIAL



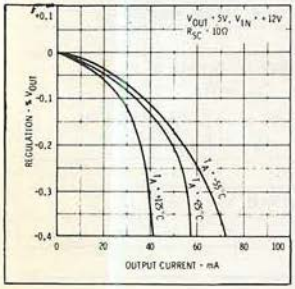
LOAD REGULATION CHARACTERISTICS WITHOUT CURRENT LIMITING



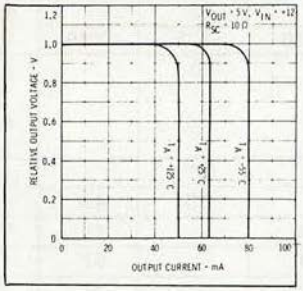
LOAD REGULATION CHARACTERISTICS WITH CURRENT LIMITING



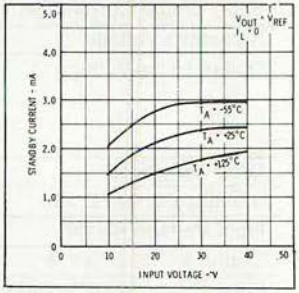
LOAD REGULATION CHARACTERISTICS WITH CURRENT LIMITING



CURRENT LIMITING CHARACTERISTICS

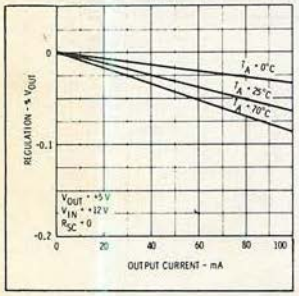


AS A STANDBY CURRENT DRAIN FUNCTION OF INPUT VOLTAGE

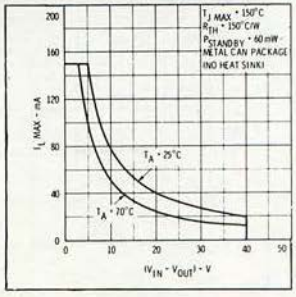


TYPICAL PERFORMANCE CURVES MIC723-5

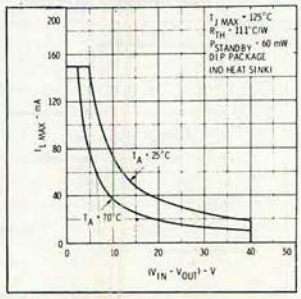
LOAD REGULATION CHARACTERISTICS WITHOUT CURRENT LIMITING



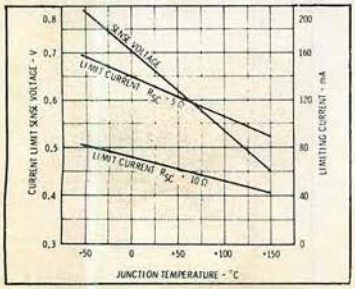
MAXIMUM LOAD CURRENT AS A FUNCTION OF INPUT-OUTPUT VOLTAGE DIFFERENTIAL



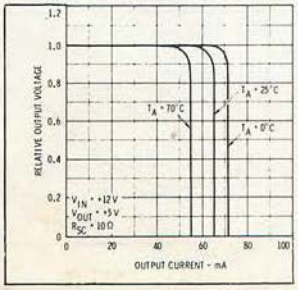
MAXIMUM LOAD CURRENT AS A FUNCTION OF INPUT-OUTPUT VOLTAGE DIFFERENTIAL



CURRENT LIMITING CHARACTERISTICS AS A FUNCTION OF JUNCTION TEMPERATURE



CURRENT LIMITING CHARACTERISTICS



LOAD REGULATION CHARACTERISTICS WITH CURRENT LIMITING

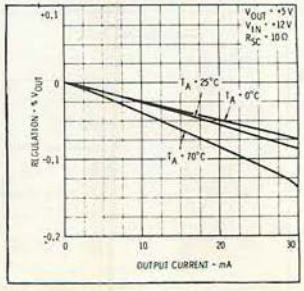


TABLE I — RESISTOR VALUES (kΩ) FOR STANDARD OUTPUT VOLTAGES

Positive Output Voltage	Applicable Figures	Fixed Output ±5%		Output Adjustable ±10% (Note 5)			Negative Output Voltage	Applicable Figures	Fixed Output ±5%		5% Output Adjustable ±10%		
	(Note 4)	R_1	R_2	R_1	P_1	R_2			R_1	R_2	R_1	P_1	R_2
+3.0	1, 5, 6, 9, 12 (4)	4.12	3.01	1.8	0.5	1.2	+100	7	3.57	102	2.2	10	91
+3.6	1, 5, 6, 9, 12 (4)	3.57	3.65	1.5	0.5	1.5	+250	7	3.57	255	2.2	10	240
+5.0	1, 5, 6, 9, 12 (4)	2.15	4.99	.75	0.5	2.2	−6 (note 6)	3, (10)	3.57	2.43	1.2	0.5	.75
+6.0	1, 5, 6, 9, 12 (4)	1.15	6.04	0.5	0.5	2.7	−9	3, 10	3.48	5.36	1.2	0.5	2.0
+9.0	2, 4, (5, 6, 12, 9)	1.87	7.15	.75	1.0	2.7	−12	3, 10	3.57	8.45	1.2	0.5	3.3
+12	2, 4, (5, 6, 9, 12)	4.87	7.15	2.0	1.0	3.0	−15	3, 10	3.65	11.5	1.2	0.5	4.3
+15	2, 4, (5, 6, 9, 12)	7.87	7.15	3.3	1.0	3.0	−28	3, 10	3.57	24.3	1.2	0.5	10
+28	2, 4, (5, 6, 9, 12)	21.0	7.15	5.6	1.0	2.0	−45	8	3.57	41.2	2.2	10	33
+45	7	3.57	48.7	2.2	10	39	−100	8	3.57	97.6	2.2	10	91
+75	7	3.57	78.7	2.2	10	68	−250	8	3.57	249	2.2	10	240

TABLE II — FORMULAE FOR INTERMEDIATE OUTPUT VOLTAGES

Outputs from +2 to +7 volts
[Figures 1, 5, 6, 9, 12, (4)]

$$V_{OUT} = [V_{REF} \times \frac{R_2}{R_1 + R_2}]$$

Outputs from +4 to +250 volts
[Figure 7]

$$V_{OUT} = [\frac{V_{REF}}{2} \times \frac{R_2 - R_1}{R_1}]\ ;\ R_3 = R_4$$

Current Limiting

$$I_{LIMIT} = \frac{V_{SENSE}}{R_{SC}}$$

Outputs from +7 to +37 volts
[Figures 2, 4, (5, 6, 9, 12)]

$$V_{OUT} = [V_{REF} \times \frac{R_1 + R_2}{R_2}]$$

Outputs from −6 to −250 volts
[Figures 3, 8, 10]

$$V_{OUT} = [\frac{V_{REF}}{2} \times \frac{R_1 + R_2}{R_1}]\ ;\ R_3 = R_4$$

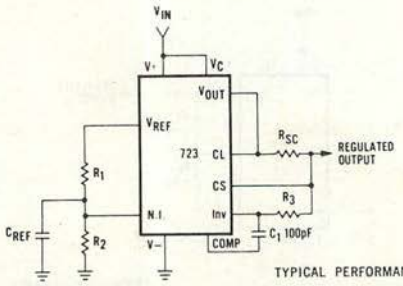
Foldback Current Limiting

$$I_{KNEE} = [\frac{V_{OUT}\ R_3}{R_{SC}\ R_4} + \frac{V_{SENSE}\ (R_3 + R_4)}{R_{SC}\ R_4}]$$

$$I_{SHORT\ CKT} = [\frac{V_{SENSE}}{R_{SC}} \times \frac{R_3 + R_4}{R_4}]$$

Figure 1

BASIC LOW VOLTAGE REGULATOR
(V_{out} = 2 to 7 Volts)



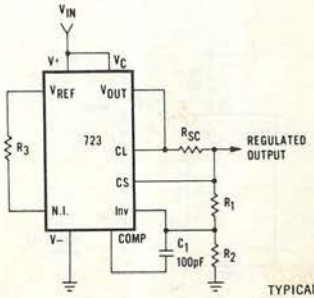
TYPICAL PERFORMANCE

Regulated Output Voltage	5 V
Line Regulation (ΔV_{IN} = 3 V)	0.5 mV
Load Regulation (ΔI_L=50 mA)	1.5 mV

Note: $R_3 = \frac{R_1\ R_2}{R_1 + R_2}$ for minimum temperature drift.

Figure 2

BASIC HIGH VOLTAGE REGULATOR
(V_{out} = 7 to 37 Volts)



TYPICAL PERFORMANCE

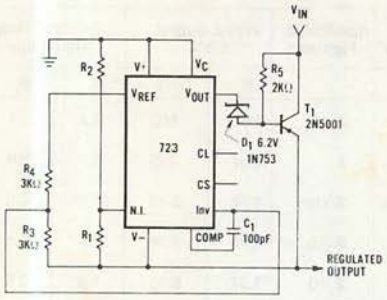
Regulated Output Voltage	15 V
Line Regulation (ΔV_{IN} = 3 V)	1.5 mV
Load Regulation (ΔI_L=50 mA)	4.5 mV

Note: $R_3 = \frac{R_1\ R_2}{R_1 + R_2}$ for minimum temperature drift.

R_3 may be eliminated for minimum component count.

Figure 3

NEGATIVE VOLTAGE REGULATOR

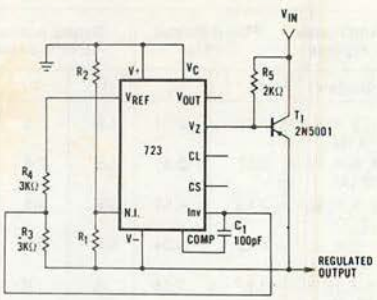


TYPICAL PERFORMANCE

Regulated Output Voltage	−15 V
Line Regulation (ΔV_{IN} = 3 V)	1 mV
Load Regulation (ΔI_L = 100 mA)	2 mV

Figure 3A*

NEGATIVE VOLTAGE REGULATOR



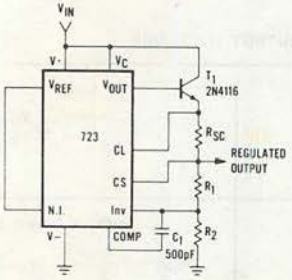
TYPICAL PERFORMANCE

Regulated Output Voltage	−15 V
Line Regulation (ΔV_{IN} = 3 V)	1 mV
Load Regulation (ΔI_L = 100 mA)	2 mV

Note 3

Figure 4

POSITIVE VOLTAGE REGULATOR
(External NPN Pass Transistor)

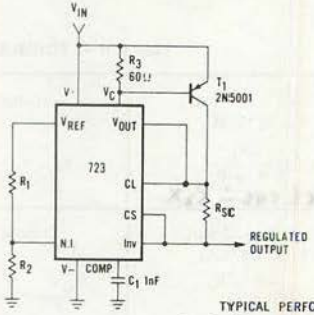


TYPICAL PERFORMANCE

Regulated Output Voltage	+15 V
Line Regulation (ΔV_{IN} = 3 V)	1.5 mV
Load Regulation (ΔI_L = 1 A)	15 mV

Figure 5

POSITIVE VOLTAGE REGULATOR
(External PNP Pass Transistor)

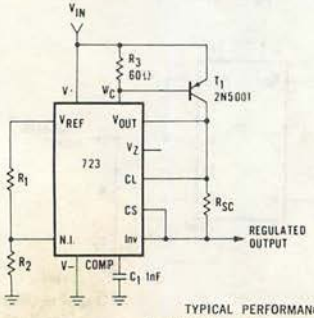


TYPICAL PERFORMANCE

Regulated Output Voltage	+5 V
Line Regulation (ΔV_{IN} = 3 V)	0.5 mV
Load Regulation (ΔI_L = 1 A)	5 mV

Figure 5A*

POSITIVE VOLTAGE REGULATOR
(External PNP Pass Transistor)

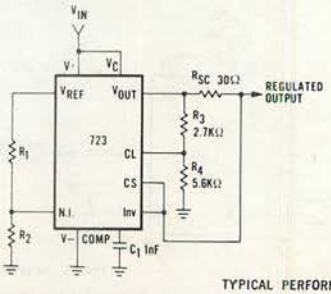


TYPICAL PERFORMANCE

Regulated Output Voltage	+5 V
Line Regulation (ΔV_{IN} = 3 V)	0.5 mV
Load Regulation (ΔI_L = 1 A)	5 mV

Figure 6

FOLDBACK CURRENT LIMITING

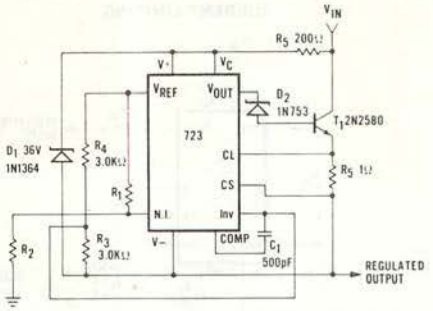


TYPICAL PERFORMANCE

Regulated Output Voltage	+5 V
Line Regulation (ΔV_{IN} = 3 V)	0.5 mV
Load Regulation (ΔI_L = 10 mA)	1 mV
Current Limit Knee	20 mA

* Figure numbers followed by "A" indicate low temperature range

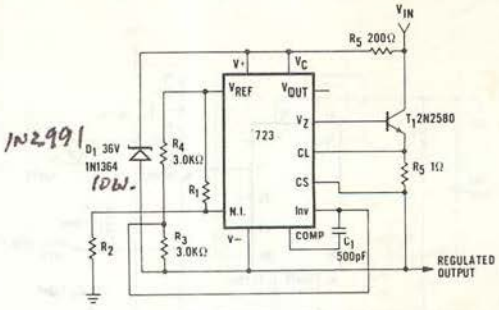
Figure 7
POSITIVE FLOATING REGULATOR



TYPICAL PERFORMANCE

Regulated Output Voltage	+50 V
Line Regulation (ΔV_{IN} = 20 V)	15 mV
Load Regulation (ΔI_L = 50 mA)	20 mV

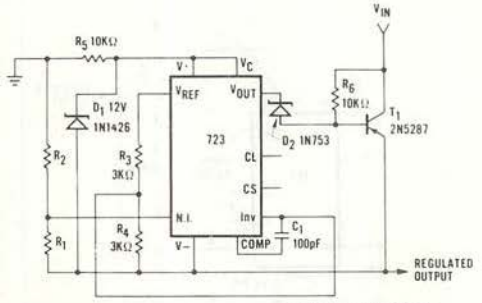
Figure 7A*
POSITIVE FLOATING REGULATOR



TYPICAL PERFORMANCE

Regulated Output Voltage	+50 V
Line Regulation (ΔV_{IN} = 20 V)	15 mV
Load Regulation (ΔI_L = 50 mA)	20 mV

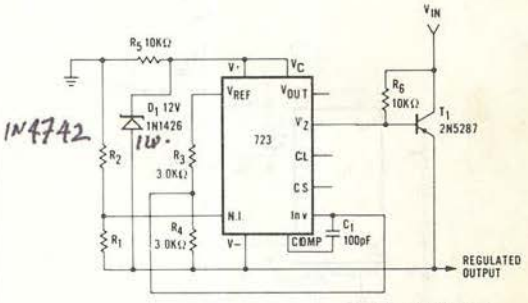
Figure 8
NEGATIVE FLOATING REGULATOR



TYPICAL PERFORMANCE

Regulated Output Voltage	−100 V
Line Regulation (ΔV_{IN} = 20 V)	30 mV
Load Regulation (ΔI_L=100 mA)	20 mV

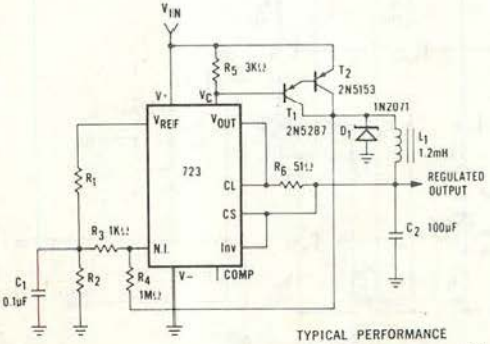
Figure 8A*
NEGATIVE FLOATING REGULATOR



TYPICAL PERFORMANCE

Regulated Output Voltage	−100 V
Line Regulation (ΔV_{IN} = 20 V)	30 mV
Load Regulation (ΔI_L=100 mA)	20 mV

Figure 9
POSITIVE SWITCHING REGULATOR

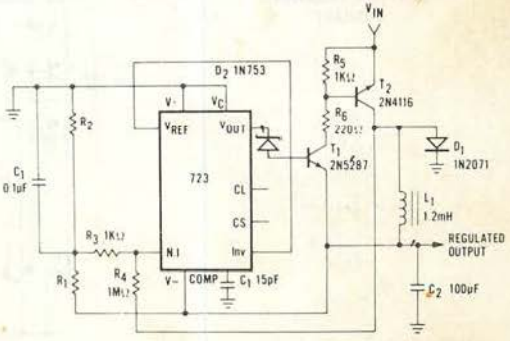


TYPICAL PERFORMANCE

Regulated Output Voltage	+5 V
Line Regulation (ΔV_{IN} = 30 V)	10 mV
Load Regulation (ΔI_L = 2 A)	80 mV

Note 3

Figure 10
NEGATIVE SWITCHING REGULATOR



TYPICAL PERFORMANCE

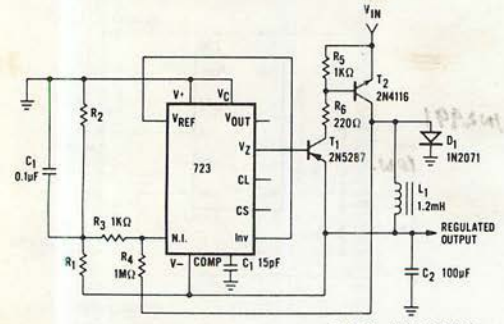
Regulated Output Voltage	−15 V
Line Regulation (ΔV_{IN} = 20 V)	8 mV
Load Regulation (ΔI_L = 2 A)	6 mV

Note 3

* Figure numbers followed by "A" indicate low temperature range

Figure 10A*

NEGATIVE SWITCHING REGULATOR



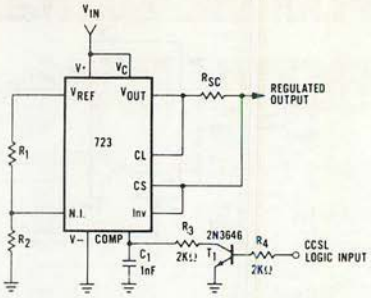
TYPICAL PERFORMANCE

Regulated Output Voltage	−15 V
Line Regulation (ΔV_{IN} = 20 V)	8 mV
Load Regulation (ΔI_L = 2 A)	6 mV

Note 3
Note 7

Figure 11

REMOTE SHUTDOWN REGULATOR WITH CURRENT LIMITING



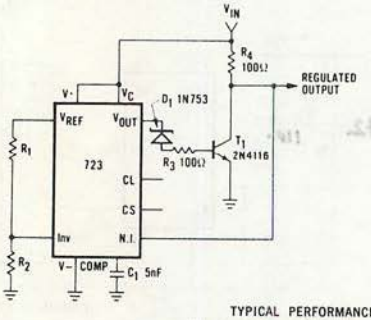
Note: Current limit transistor may be used for shutdown if current limiting is not required.

TYPICAL PERFORMANCE

Regulated Output Voltage	+5 V
Line Regulation (ΔV_{IN} = 3 V)	0.5 mV
Load Regulation (ΔI_L = 50 mA)	1.5 mV

Figure 12

SHUNT REGULATOR

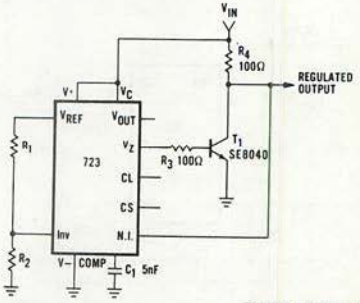


TYPICAL PERFORMANCE

Regulated Output Voltage	+5 V
Line Regulation (ΔV_{IN} = 10 V)	0.5 mV
Load Regulation (ΔI_L = 100 mA)	1.5 mV

Figure 12 *

SHUNT REGULATOR



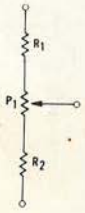
Note 3

TYPICAL PERFORMANCE

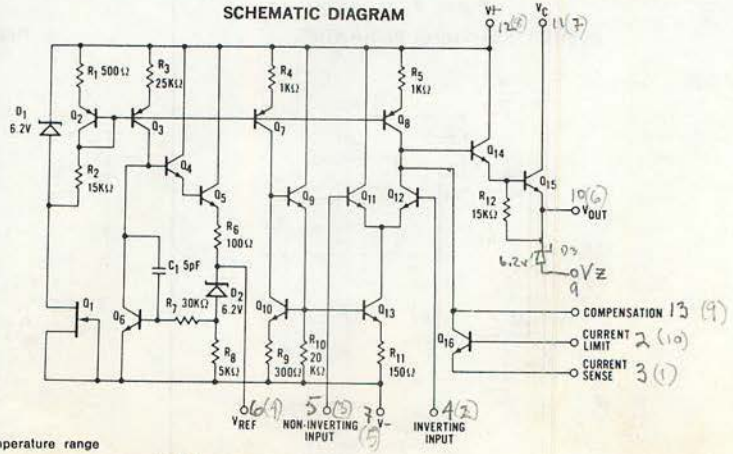
Regulated Output Voltage	+5 V
Line Regulation (ΔV_{IN} = 10 V)	0.5 mV
Load Regulation (ΔI_L = 100 mA)	1.5 mV

Figure 13

OUTPUT VOLTAGE ADJUST



SCHEMATIC DIAGRAM



* Figure numbers followed by "A" indicate low temperature range

TEMPERATURE-CONTROLLED DIFFERENTIAL PAIR

- **Excellent Transistor Matching**
- **Close Thermal Coupling**
- **Fast Thermal Response**
- **Tight Temperature Control**

MIC726 is a monolithic transistor pair in a high thermal-resistance package, held at a constant temperature by active temperature regulator circuitry. The transistor pair displays the excellent matching, close thermal coupling and fast thermal response inherent in monolithic construction. The high gain and low standby dissipation of the regulator circuit permits tight temperature control over a wide range of ambient temperatures. It is intended for use as an input stage in very-low drift dc amplifiers, replacing complex chopper-stabilized amplifiers; it is also useful as the nonlinear element in logarithmic amplifiers and multipliers where the highly predictable exponential relation between emitter-base voltage and collector current is employed. The device is constructed on a single silicon chip using the ITT Planar process.

ABSOLUTE MAXIMUM RATINGS

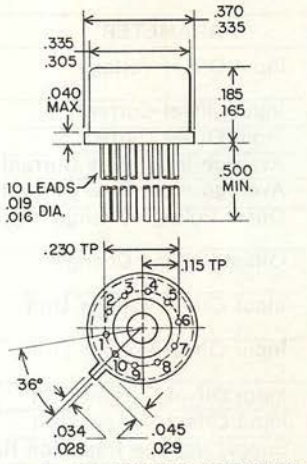
CHARACTERISTICS	UNITS
Operating Temperature Range	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering 60 seconds)	300°C
Supply Voltage	±18 V

MAXIMUM RATINGS FOR EACH TRANSISTOR

CHARACTERISTICS	UNITS
Maximum collector-to-substrate voltage	40 V
BV_{CBO}	40 V
LV_{CEO} [Note 1]	30 V
BV_{EBO}	5 V
Collector Current	5 mA

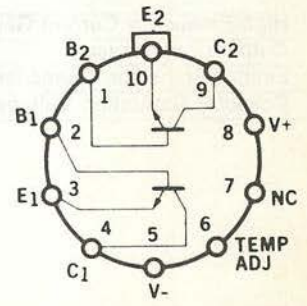
Note 1: Measured at 1 mA collector current.

PHYSICAL DIMENSIONS



NOTES: LEADS ARE GOLD-PLATED KOVAR
PACKAGE WEIGHT IS 1.32 GRAMS

CONNECTION DIAGRAM



SPECIAL ORDERING CODE

Temperature Range:
1 = −55°C to 125°C
5 = 0°C to 70°C

Package:
C = 10-lead TO-5
D = 14-lead DIP

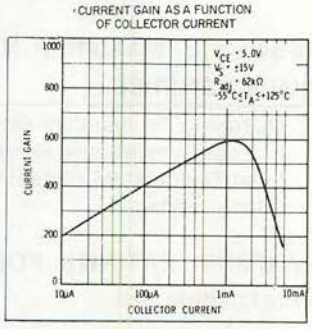
Example:
MIC726-1C means operating temperature range of −55°C to +125°C, supplied in a TO-5 package.

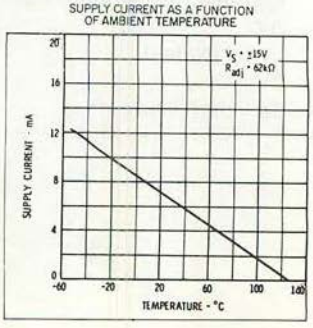
ELECTRICAL CHARACTERISTICS for MIC 726-1

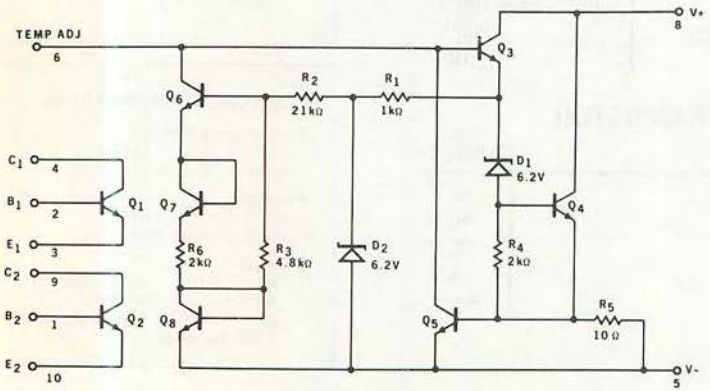
($-55°C \leq T_A \leq +125°C$, $V_S = \pm 15$ V, $R_{adj} = 62k\Omega$ unless otherwise specified)

PARAMETER	MIN.	TYP.	MAX.	UNITS	CONDITIONS
Input Offset Voltage		1.0	2.5	mV	$10\ \mu A \leq I_C \leq 100\mu A$, $V_{CE} = 5$ V, $R_S \leq 50\Omega$
Input Offset Current		10	50	nA	$I_C = 10\ \mu A$, $V_{CE} = 5$ V
Input Offset Current		50	200	nA	$I_C = 100\ \mu A$, $V_{CE} = 5$ V
Average Input Bias Current		50	150	nA	$I_C = 10\ \mu A$, $V_{CE} = 5$ V
Average Input Bias Current		250	500	nA	$I_C = 100\ \mu A$, $V_{CE} = 5$ V
Offset Voltage Change		0.3	6.0	mV	$I_C = 10\ \mu A$, $5\text{ V} \leq V_{CE} \leq 25$ V, $R_S \leq 100$ kΩ
Offset Voltage Change		0.3	6.0	mV	$I_C = 100\ \mu A$, $5\text{ V} \leq V_{CE} \leq 25$ V, $R_S \leq 10$ kΩ
Input Offset Voltage Drift		0.2	1.0	μV/°C	$10\ \mu A \leq I_C \leq 100\ \mu A$, $V_{CE} = 5$ V, $R_S \leq 50\Omega$, $+25°C \leq T_A \leq +125°C$
Input Offset Voltage Drift		0.2	1.0	μV/°C	$10\ \mu A \leq I_C \leq 100\ \mu A$, $V_{CE} = 5$ V, $R_S \leq 50\Omega$, $-55°C \leq T_A \leq +25°C$
Input Offset Current Drift		10		pA/°C	$I_C = 10\ \mu A$, $V_{CE} = 5$ V
Input Offset Current Drift		30		pA/°C	$I_C = 100\ \mu A$, $V_{CE} = 5$ V
Supply Voltage Rejection Ratio		25		μV/V	$10\ \mu A \leq I_C \leq 100\ \mu A$, $R_S \leq 50\Omega$,
Low-Frequency Noise		4.0		μV pp	$I_C = 10\ \mu A$, $V_{CE} = 5$ V, $R_S \leq 50\Omega$, BW = .001 Hz to 0.1 Hz
Broadband Noise		10		μV pp	$I_C = 10\ \mu A$, $V_{CE} = 5$ V, $R_S \leq 50\Omega$, BW = 0.1 Hz to 10 kHz
Long-Term Drift		5.0		μV/week	$10\ \mu A \leq I_C \leq 100\ \mu A$, $V_{CE} = 5$ V, $R_S \leq 50\Omega$, $T_A = 25°C$
High-Frequency Current Gain	1.5	3.5			f=20 MHz, $I_C = 100\ \mu A$, $V_{CE}=5$ V
Output Capacitance		1.0		pF	$I_E = 0$, $V_{CB} = 5$ V
Emitter Transition Capacitance		1.0		pF	$I_E = 100\ \mu A$
Collector Saturation Voltage		0.5	1.0	V	$I_B = 100\ \mu A$, $I_C = 1$ mA

TYPICAL CHARACTERISTICS FOR MIC726-1





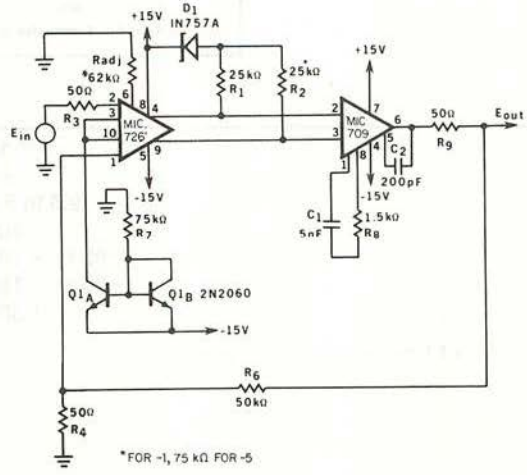


SCHEMATIC DIAGRAM-1-5

ELECTRICAL CHARACTERISTICS for MIC726-5

($0°C \leq T_A \leq +85°C$, $V_S = \pm 15$ V, $R_{adj} = 75$ kΩ unless otherwise specified)

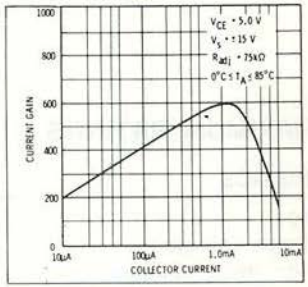
PARAMETER	MIN.	TYP.	MAX.	UNITS	CONDITIONS
Input Offset Voltage		1.0	3.0	mV	$10\ \mu A \leq I_C \leq 100\mu A$ $V_{CE} = 5$ V, $R_S \leq 50\Omega$
Input Offset Current		10	100	nA	$I_C = 10\ \mu A$, $V_{CE} = 5$ V
Input Offset Current		50	400	nA	$I_C = 100\ \mu A$, $V_{CE} = 5$ V
Average Input Bias Current		50	300	nA	$I_C = 10\ \mu A$, $V_{CE} = 5$ V
Average Input Bias Current		250	1000	nA	$I_C = 100\ \mu A$, $V_{CE} = 5$ V
Offset Voltage Change		0.3	6.0	mV	$I_C = 10\ \mu A$, $5\text{ V} \leq V_{CE} \leq 25$ V, $R_S \leq 100$ kΩ
Offset Voltage Change		0.3	6.0	mV	$I_C = 100\ \mu A$, $5\text{ V} \leq V_{CE} \leq 25$ V, $R_S \leq 10$ kΩ
Input Offset Voltage Drift		0.2	2.0	μV/°C	$I_C = 100\ \mu A$, $V_{CE} = 5$ V, $R_S \leq 50\Omega$
Input Offset Current Drift		10		pA/°C	$I_C = 10\ \mu A$, $V_{CE} = 5$ V
Input Offset Current Drift		30		pA/°C	$I_C = 100\ \mu A$, $V_{CE} = 5$ V
Supply Voltage Rejection Ratio		25		μV/V	$I_C = 100\ \mu A$, $R_S = 50\Omega$
Low-Frequency Noise		4.0		μV pp	$I_C = 10\ \mu A$, $V_{CE} = 5$ V, $R_S \leq 50\Omega$, BW = 0.001 Hz to 0.1 Hz
Broadband Noise		10		μV pp	$I_C = 10\ \mu A$, $V_{CE} = 5$ V, $R_S \leq 50\Omega$, BW = 0.1 Hz to 10 kHz
Long-Term Drift		5.0		μV/week	$I_C = 100\ \mu A$, $V_{CE} = 5$ V, $R_S \leq 50\Omega$, $T_A = 25°C$
High-Frequency Current Gain	1.5	3.5			f = 20 MHz, $I_C = 100\ \mu A$, $V_{CE} = 5$ V
Output Capacitance		1.0		pF	$I_E = 0$, $V_{CB} = 5$ V
Emitter Transition Capacitance		1.0		pF	$I_E = 100\ \mu A$
Collector Saturation Voltage		0.5	1.0	V	$I_B = 100\ \mu A$, $I_C = 1$ mA



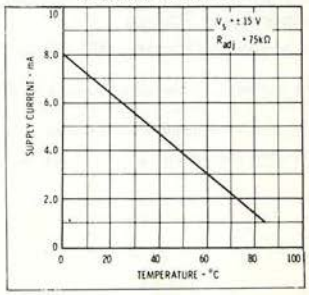
TYPICAL X1000 CIRCUIT

TYPICAL CHARACTERISTICS FOR MIC726-5

CURRENT GAIN AS A FUNCTION OF COLLECTOR CURRENT



SUPPLY CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE

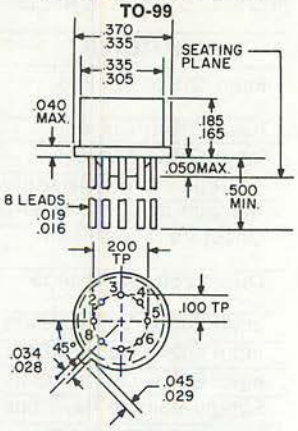


DIFFERENTIAL AMPLIFIER

- **Low Input Offset Voltage**
- **High and Low Impedance Differential Outputs**
- **1.0 MHz Bandwidth**

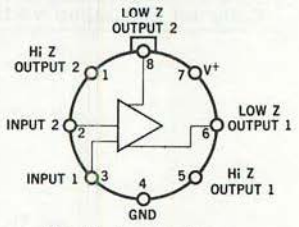
The MIC730 is a differential amplifier constructed on a single silicon-chip using the ITT Planar epitaxial process. This device has a wide range of applications since it has both a differential input and output; any combination of single-ended or differential configurations can be employed at its input and output. The emitter follower output stage gives this device a low output impedance making it useful as a preamplifier.

PHYSICAL DIMENSIONS
TO-99



NOTE: DIMENSIONS AS PER LATEST JS-10 COMMITTEE.
ALL DIMENSIONS IN INCHES.
LEADS ARE GOLD-PLATED KOVAR.
PACKAGE WEIGHT IS 1.22 GRAMS.

CONNECTION DIAGRAM



Note: Pin 4 connected to case

ABSOLUTE MAXIMUM RATINGS

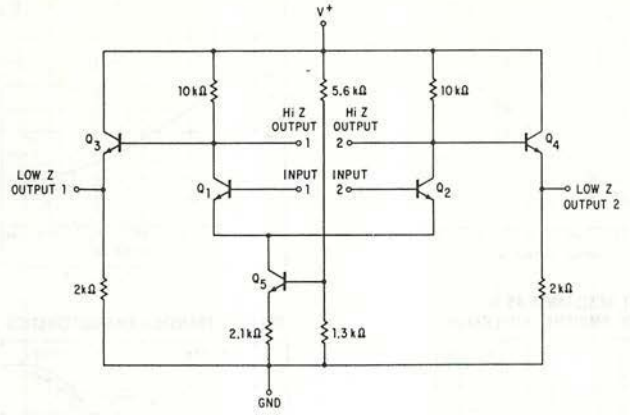
CHARACTERISTICS		UNITS
Supply Voltage	15	V
Differential Input Voltage	±5	V
Common Mode Input Voltage	2.5 to 5.5	V
Internal Power Dissipation (Note 1 and 2)	300	mW
Operating Temperature Range (Note 3)	−55 to +125	°C
Storage Temperature Range	−65 to +150	°C
Lead Temperature (Soldering, 60 seconds)	+300	°C

NOTES: (1) Rating applies for case temperature to +125°C; derate linearly at 5.6 mW/°C for ambient temperature above +105°C.

(2) Rating applies for ambient temperatures to +70°C.

(3) Also limited temperature range from 0°C to +70°C.

SCHEMATIC DIAGRAM



SPECIAL ORDERING CODE

Temperature Range:
1 = −55°C to +125°C
5 = 0°C to +70°C

Package:
C = TO-99

Example:
MJC730-1C means operating temperature range of −55°C to +125°C, supplied in a TO-99 package.

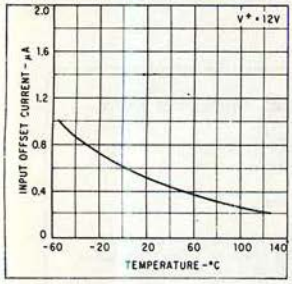
For Package Options:
Contact local ITT Franchised Distributor or Field Sales Office.

ELECTRICAL CHARACTERISTICS ($T_A = 25°C$, $V+ = 12.0$ V, and $V_{CM} = 3.5$ V unless otherwise specified)

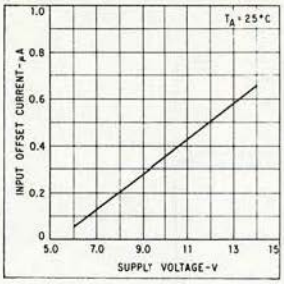
PARAMETER (See Definitions)	−55°C to +125°C			CONDITIONS	0°C to +70°C			UNITS	CONDITIONS
	MIN.	TYP.	MAX.		MIN.	TYP.	MAX.		
Input Offset Voltage		1.0	2.5	$R_S \leq 50\Omega$		2.0	5.0	mV	$R_S \leq 50\Omega$
Input Offset Current		0.5	1.5			0.7	3.0	μA	
Input Bias Current		3.5	7.5			4.5	16.0	μA	
Input Resistance	5.0	20			2.5	15		kΩ	
Differential Voltage Gain	100	145	160	$R_L \geq 100$ kΩ	100	135	160		$R_L \geq 100$ kΩ
Differential Distortion		80	300	$R_L \geq 100$ kΩ		85	300	mVpp	$R_L \geq 100$ kΩ
Bandwidth	1.0	1.5			1.0	1.5		MHz	
Single-Ended Output Resistance		70	500			70	500	Ω	
Output Voltage Swing	5.0	8.0		$R_L \geq 100$ kΩ	5.0	8.0		Vpp	$R_L \geq 100$ kΩ
Supply Current		9.5	13	$R_L \geq 100$ kΩ		9.5	13	mA	$R_L \geq 100$ kΩ
Power Consumption		114	156	$R_L \geq 100$ kΩ		114	156	mW	$R_L \geq 100$ kΩ
The following specifications apply for $-55°C \leq T_A \leq 125°C$:					The following specifications apply for $0°C \leq T_A \leq +70°C$:				
Input Offset Voltage			3.5	$R_S \leq 50\Omega$			7.5	mV	$R_S \leq 50\Omega$
Input Offset Current		0.2	1.5	$T_A = +125°C$		0.5	3.0	μA	$T_A = +70°C$
		1.0	3.0	$T_A = -55°C$		0.8	5.0	μA	$T_A = 0°C$
Input Bias Current		6.5	15	$T_A = -55°C$		5.0	20	μA	$T_A = 0°C$
Input Resistance	0.9				1.8			kΩ	
Input Voltage Range	3.5		5.2		+3.5		+5.2		
Common Mode Rejection Ratio	70	85		$R_S \leq 50\Omega$ f ≤ 1.0 kHz, +3.5 V ≤ V_{CM} ≤ +5.2 V	60	80		dB	$R_S \leq 50\Omega$ f ≤ 1.0 kHz, +3.5 V ≤ V_{CM} ≤ +5.2 V
Differential Voltage Gain	90		175	$R_L \geq 100$ kΩ	80		190		$R_L \geq 100$ kΩ
Common Mode Output Voltage	5.5	7.0	7.75		5.0	7.0	8.0	V	
Output Resistance			600				600	Ω	
Output Voltage Swing	4.5	6.8			4.5	7.5		Vpp	
Supply Current		10	15	$T_A = -55°C$		10	15	mA	$T_A = 0°C$
		8.0	11	$T_A = 125°C$		8.8	13	mA	$T_A = +70°C$
Power Consumption		120	180	$T_A = -55°C$		120	180	mW	$T_A = 0°C$
		96	121	$T_A = 125°C$		100	158	mW	$T_A = +70°C$

TYPICAL PERFORMANCE CURVES FOR −55°C TO +125°C

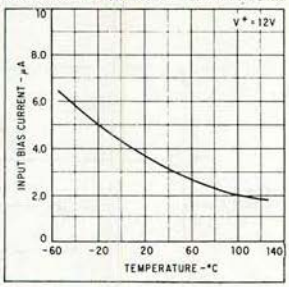
INPUT OFFSET CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



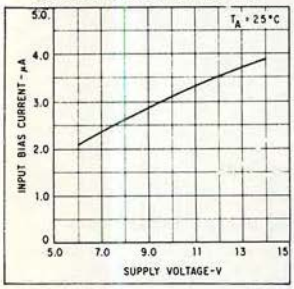
INPUT OFFSET CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



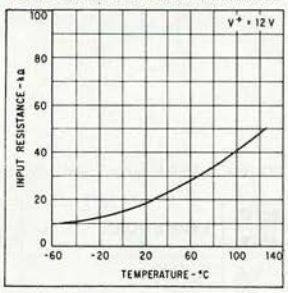
INPUT BIAS CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



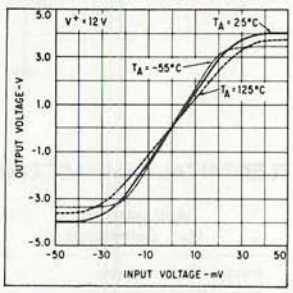
INPUT BIAS CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



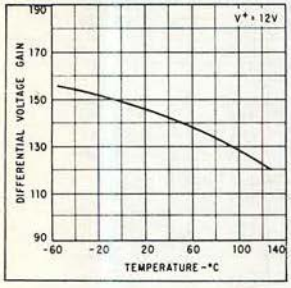
INPUT RESISTANCE AS A FUNCTION OF AMBIENT TEMPERATURE



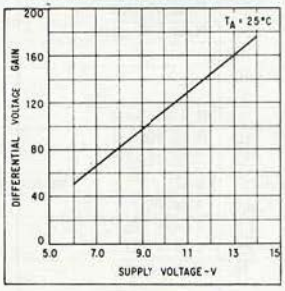
VOLTAGE TRANSFER CHARACTERISTICS



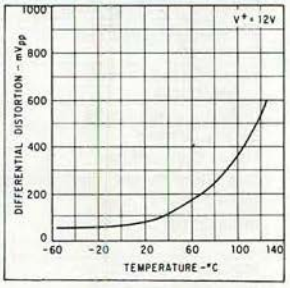
DIFFERENTIAL VOLTAGE GAIN AS A FUNCTION OF AMBIENT TEMPERATURE



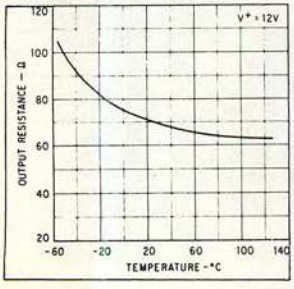
DIFFERENTIAL VOLTAGE GAIN AS A FUNCTION OF SUPPLY VOLTAGE



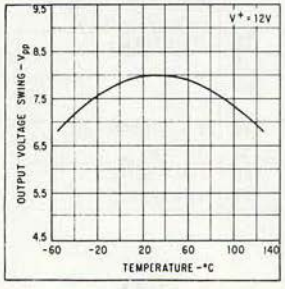
DIFFERENTIAL DISTORTION AS A FUNCTION OF AMBIENT TEMPERATURE



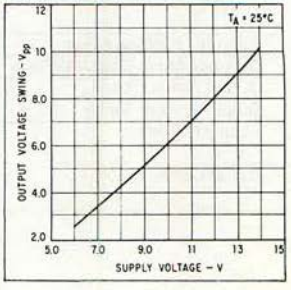
OUTPUT RESISTANCE AS A FUNCTION OF AMBIENT TEMPERATURE



OUTPUT VOLTAGE SWING AS A FUNCTION OF AMBIENT TEMPERATURE

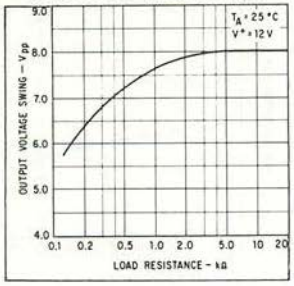


OUTPUT VOLTAGE SWING AS A FUNCTION OF SUPPLY VOLTAGE

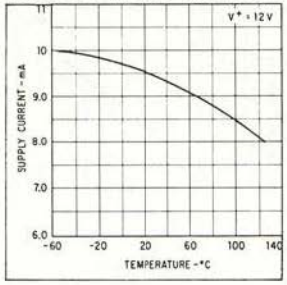


TYPICAL PERFORMANCE CURVES FOR −55°C TO +125°C

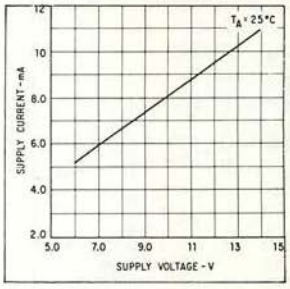
OUTPUT VOLTAGE SWING AS A FUNCTION OF LOAD RESISTANCE



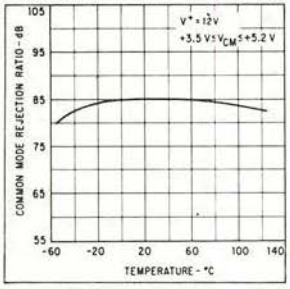
SUPPLY CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



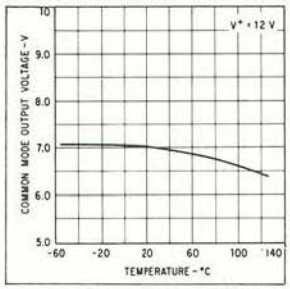
SUPPLY CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



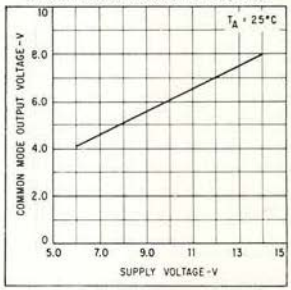
COMMON MODE REJECTION RATIO AS A FUNCTION OF AMBIENT TEMPERATURE



COMMON MODE OUTPUT VOLTAGE AS A FUNCTION OF AMBIENT TEMPERATURE

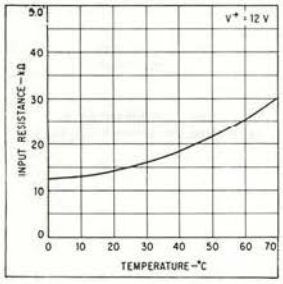


COMMON MODE OUTPUT VOLTAGE AS A FUNCTION OF SUPPLY VOLTAGE

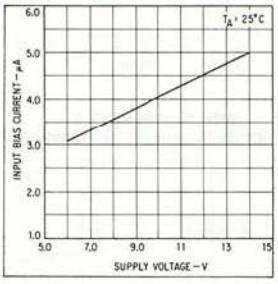


TYPICAL PERFORMANCE CURVES FOR 0°C TO +70°C

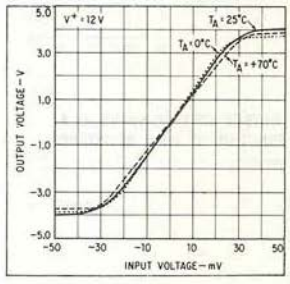
INPUT RESISTANCE AS A FUNCTION OF AMBIENT TEMPERATURE



INPUT BIAS CURRENT AS A FUNCTION OF SUPPLY VOLTAGE

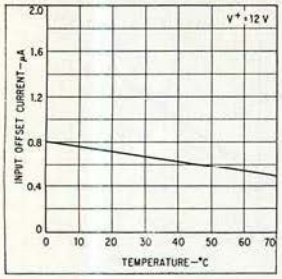


VOLTAGE TRANSFER CHARACTERISTICS

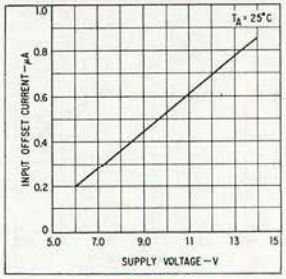


TYPICAL PERFORMANCE CURVES FOR 0°C TO +70°C

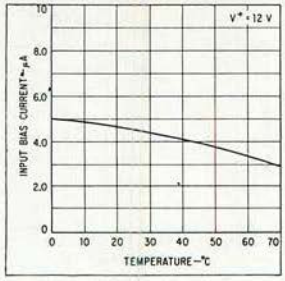
INPUT OFFSET CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



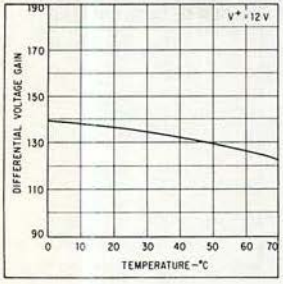
INPUT OFFSET CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



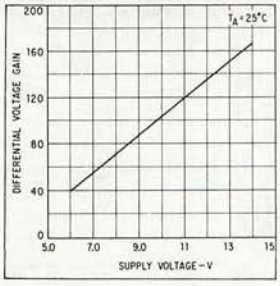
INPUT BIAS CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



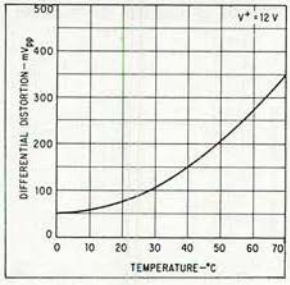
DIFFERENTIAL DISTORTION AS A FUNCTION OF AMBIENT TEMPERATURE



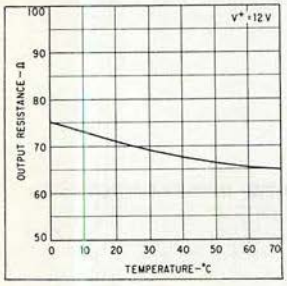
DIFFERENTIAL VOLTAGE GAIN AS A FUNCTION OF SUPPLY VOLTAGE



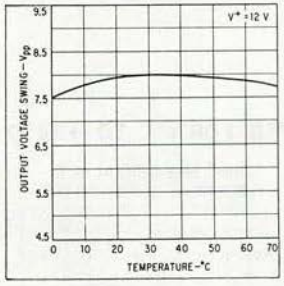
DIFFERENTIAL VOLTAGE GAIN AS A FUNCTION OF AMBIENT TEMPERATURE



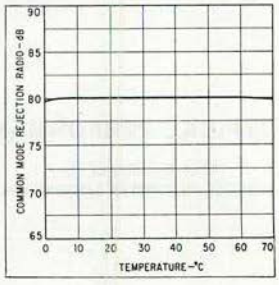
OUTPUT RESISTANCE AS A FUNCTION OF AMBIENT TEMPERATURE



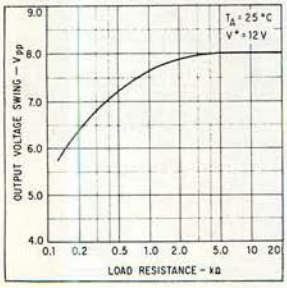
OUTPUT VOLTAGE SWING AS A FUNCTION OF AMBIENT TEMPERATURE



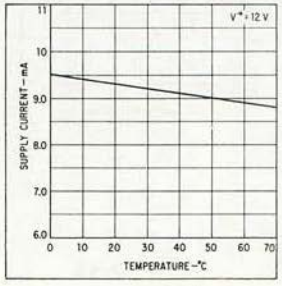
COMMON MODE REJECTION RATIO AS A FUNCTION OF AMBIENT TEMPERATURE



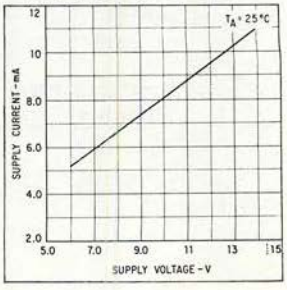
OUTPUT VOLTAGE SWING AS A FUNCTION OF LOAD RESISTANCE



SUPPLY CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE

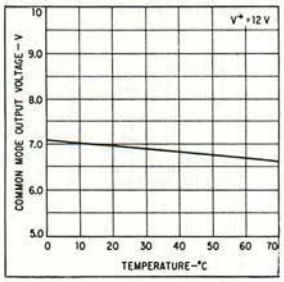


SUPPLY CURRENT AS A FUNCTION OF SUPPLY VOLTAGE

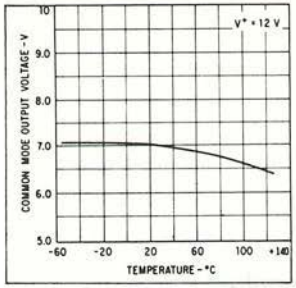


TYPICAL PERFORMANCE CURVES FOR 0°C TO +70°C

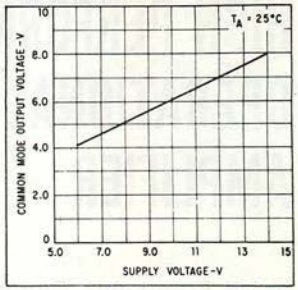
COMMON MODE OUTPUT VOLTAGE AS A FUNCTION OF AMBIENT TEMPERATURE



COMMON MODE OUTPUT VOLTAGE AS A FUNCTION OF AMBIENT TEMPERATURE



COMMON MODE OUTPUT VOLTAGE AS A FUNCTION OF SUPPLY VOLTAGE



DEFINITION OF TERMS

INPUT OFFSET VOLTAGE — That voltage which must be applied between the input terminals to obtain zero differential output voltage.

INPUT OFFSET CURRENT — The difference in the currents into the two input terminals with the output at zero differential volts.

INPUT BIAS CURRENT — The average of the two input currents.

INPUT BIAS RESISTANCE — The resistance looking into either input terminal with the other grounded.

INPUT VOLTAGE RANGE — The range of voltage which, if exceeded on either input terminal, could cause the amplifier to cease functioning properly.

COMMON MODE REJECTION RATIO — The ratio of the input voltage range to the maximum change in input offset voltage over this range.

DIFFERENTIAL VOLTAGE GAIN — The ratio of the change in the differential output voltage to the change in voltage between the input terminals producing it.

DIFFERENTIAL DISTORTION — The A.C. unbalance in the output common mode voltage produced by unsymmetrical output voltage swings.

BANDWIDTH — The frequency at which the differential voltage gain is 3 dB below its low frequency value.

OUTPUT RESISTANCE — The resistance seen looking into either output terminal with the output at differential null.

COMMON MODE OUTPUT VOLTAGE — The average voltage at the two output terminals referred to ground.

OUTPUT VOLTAGE SWING — The peak-to-peak output swing that can be obtained without clipping.

SUPPLY CURRENT — The current required from the power supply to operate the device with no load.

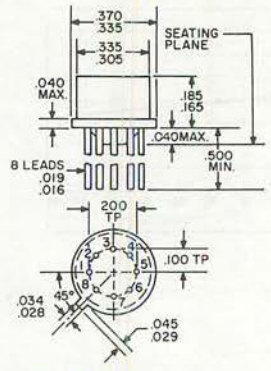
POWER CONSUMPTION — The DC power required to operate the amplifier with no load current.

HIGH PERFORMANCE OPERATIONAL AMPLIFIER

- **No Frequency Compensation Required**
- **Short-Circuit Protection**
- **Offset Voltage Null Capability**
- **Large Common-Mode and Differential Voltage Ranges**
- **Low Power Consumption**
- **No Latch Up**

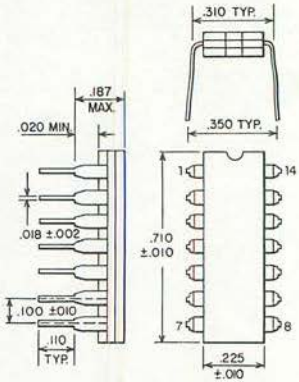
The MICA741 is a high performance monolithic operational amplifier constructed on a single silicon chip, using the ITT Planar epitaxial process. It is intended for a wide range of analog applications. High common mode voltage range and absence of "latch-up" tendencies make the MICA741 ideal for use as a voltage follower. The high gain and wide range of operating voltages provide superior performance in integrator, summing amplifier, and general feedback applications. The MICA741 is short-circuit protected, has the same pin configuration as the popular MICA709 operational amplifier, but requires no external components for frequency compensation. The internal 6dB/ octave roll-off insures stability in closed loop applications.

DIMENSIONS



NOTE: DIMENSIONS AS PER LATEST JS-10 COMMITTEE.
ALL DIMENSIONS IN INCHES.
LEADS ARE GOLD-PLATED KOVAR.
PACKAGE WEIGHT IS 1.22 GRAMS.

DUAL IN-LINE



ABSOLUTE MAXIMUM RATINGS

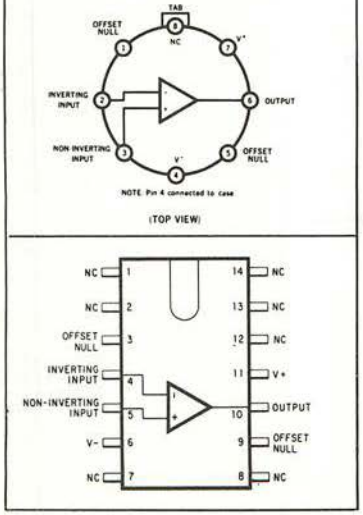
CHARACTERISTICS	MIC741-1	MIC741-5	UNITS
Supply Voltage	±22	±18	V
Internal Power Dissipation	500 (Note 1)	500	mW
Differential Input Voltage	±30	±30	V
Input Voltage (Note 2)	±15	±15	V
Storage Temperature Range	−65 to +150	−65 to +150	°C
Operating Temperature Range	−55 to +125	0 to +70	°C
Lead Temperature (Soldering, 60 sec)	300	300	°C
Output Short-Circuit Duration	Indefinite (Note 3)	Indefinite (Note)	

NOTES:
(1) Rating applies for case temperatures to 125°C; derate linearly at 6.5 mW/°C for ambient temperatures above +75°C.
(2) For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.
(3) Short circuit may be to ground or either supply. Rating applies to +125°C case temperature or +75°C ambient temperature.
( ) Short circuit may be to ground or either supply.

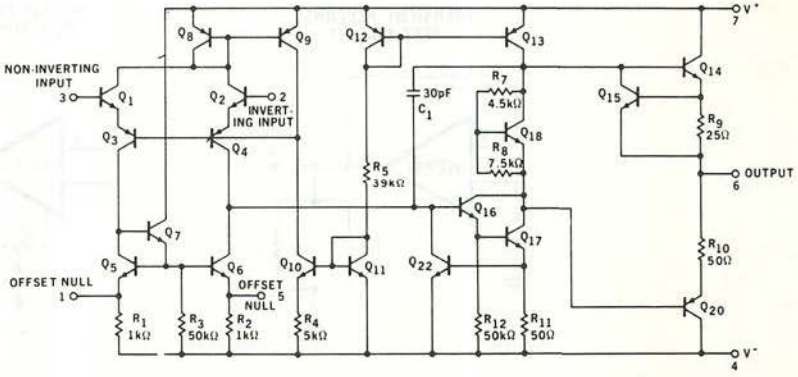
ELECTRICAL CHARACTERISTICS for MIC 741-1 ($V_S = \pm 15V$, $T_A = 25°C$ unless otherwise specified)

PARAMETER	MIN.	TYP.	MAX.	UNITS	CONDITIONS
Input Offset Voltage		1.0	5.0	mV	R_S 10kΩ
Input Offset Current		30	200	nA	
Input Bias Current		200	500	nA	
Input Resistance	0.3	1.0		MΩ	
Large-Signal Voltage Gain	50,000	200,000			$R_L \geq 2k\Omega$, $V_{out} = \pm 10V$
Output Voltage Swing	± 12 ± 10	± 14 ± 13		V V	$R_L \geq 10k\Omega$ $R_L \geq 2k\Omega$
Input Voltage Range	± 12	± 13		V	
Common Mode Rejection Ratio	70	90		dB	$R_S \leq 10k\Omega$
Supply Voltage Rejection Ratio		30	150	μV/V	$R_S \leq 10k\Omega$
Power Consumption		50	85	mW	
Transient Response (unity gain)					$V_{in} = 20mV$, $R_L = 2k\Omega$, $C_L \leq 100pF$
Risetime		0.3	1.0	μs	
Overshoot		5.0	10	%	
Slew Rate (unity gain) (Pulsed)		0.5		V/μs	
The following specifications apply for $-55°C \leq T_A \leq +125°C$:					
Input Offset Voltage			6.0	mV	$R_S \leq 10k\Omega$
Input Offset Current			500	nA	
Input Bias Current			1.5	μA	
Large Signal Voltage Gain	25,000				$R_L \geq 2k\Omega$, $V_{out} = \pm 10V$
Output Voltage Swing	± 10			V	$R_L \geq 2k\Omega$

CONNECTION DIAGRAMS



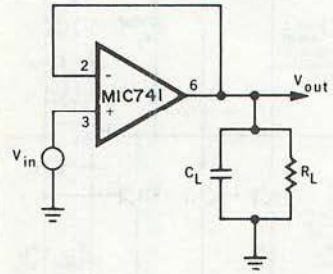
SCHEMATIC DIAGRAM



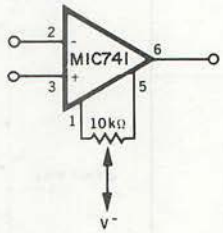
ELECTRICAL CHARACTERISTICS for MIC 741-5 ($V_S = \pm 15V$, $T_A = 25°C$ unless otherwise specified)

PARAMETER	MIN.	TYP.	MAX.	UNITS	CONDITIONS
Input Offset Voltage		2.0	6.0	mV	$R_S \leq 10k\Omega$
Input Offset Current		30	200	nA	
Input Bias Current		200	500	nA	
Input Resistance	0.3	1.0		MΩ	
Large-Signal Voltage Gain	20,000	100,000			$R_L \geq 2k\Omega$, $V_{out} = \pm 10V$
Output Voltage Swing	± 12 ± 10	± 14 ± 13		V V	$R_L \geq 10k\Omega$ $R_L \geq 2k\Omega$
Input Voltage Range	± 12	± 13		V	
Common Mode Rejection Ratio	70	90		dB	$R_S \leq 10k\Omega$
Supply Voltage Rejection Ratio		30	150	$\mu V/V$	$R_S \leq 10k\Omega$
Power Consumption		50	85	mW	
Transient Response (unity gain)					$V_{in} = 20mV$, $R_L = 2k\Omega$, $C_L \leq 100pF$
Risetime		0.3		μs	
Overshoot		5.0		%	
Slew Rate (unity gain)		0.5		$V/\mu s$	$R_L \geq 2k\Omega$
The following specifications apply for $0°C \leq T_A \leq +70°C$:					
Input Offset Voltage			7.5	mV	$R_S \leq 10k\Omega$
Input Offset Current			300	nA	
Input Bias Current			800	nA	
Large-Signal Voltage Gain	15,000				$R_L \geq 2k\Omega$, $V_{out} = \pm 10V$
Output Voltage Swing	± 10			V	$R_L \geq 2k\Omega$

TRANSIENT RESPONSE TEST CIRCUIT

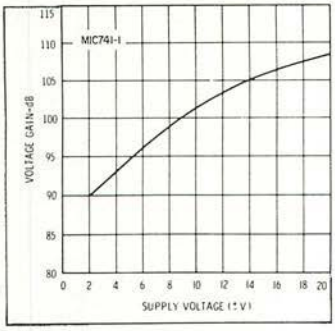


VOLTAGE OFFSET NULL CIRCUIT

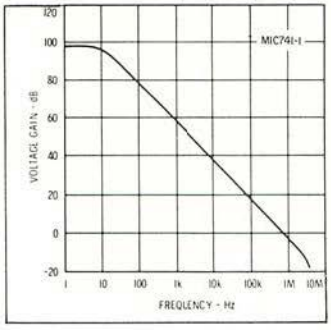


TYPICAL PERFORMANCE CURVES

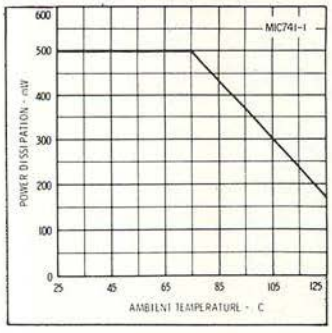
OPEN LOOP
VOLTAGE GAIN



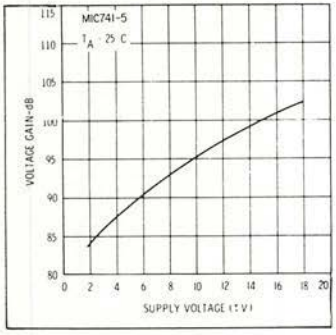
OPEN LOOP
FREQUENCY RESPONSE



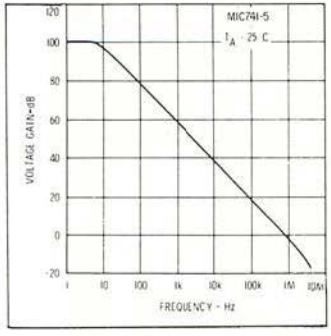
ABSOLUTE MAXIMUM
POWER DISSIPATION



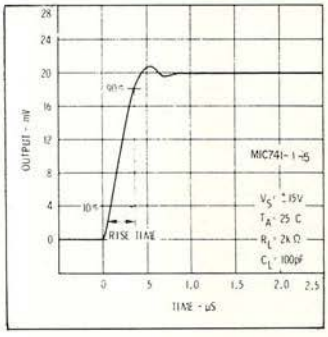
OPEN LOOP
VOLTAGE GAIN



OPEN LOOP
FREQUENCY RESPONSE



TRANSIENT RESPONSE



Monolithic integrated circuit in bipolar technique, designed primarily for use in electronic organs. The device incorporates seven flip-flops with externally accessible inputs and outputs.

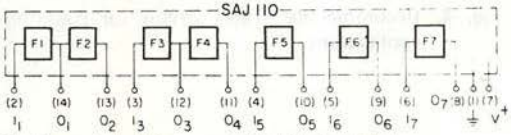
Each flip-flop changes state on application of a positive-going input pulse. The individual flip-flops can be interconnected to form a divider chain. Two flip-flop pairs are already internally series-connected as shown in Fig. 2.

An emitter-follower is interposed between each flip-flop and the associated output terminal to ensure that the output voltage is largely independent of load. Because no internal emitter resistors are provided, the emitter-follower delivers undirectional output currents.

When used in electronic organs the frequency divider SAJ110 may be driven by sine-wave as well as square-wave signals. The shape of the square-wave output signal can be modified by connection of RC filters.

If, by means of an appropriate circuit, all inputs and outputs are brought to a potential below 1.5 volts for a short time, all outputs remain in the low state.

Block Diagram

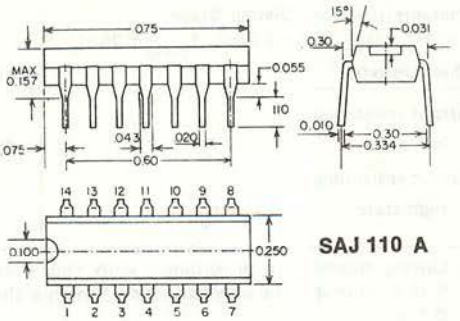


The figures in brackets correspond to the pin numbers.

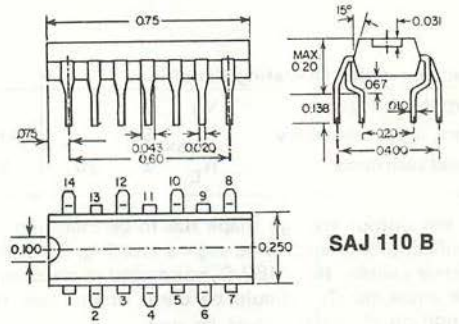
All voltages are referred to terminal 1.

ABSOLUTE MAXIMUM RATINGS

Characteristic			Unit
Supply voltage	V_7	11	V
Input voltage see Fig. 6			
Output current per stage	I_o	5*)	mA
External voltage at output terminals	V_{ext}	±5	V
Ambient temperature range	T_{amb}	−10 . . . +60	°C
Storage temperature range	T_s	−30 . . . +125	°C



SAJ 110 A



SAJ 110 B

Normally, the SAJ110 is delivered in the dual in-line plastic package TO-116 (Fig. 1a, add suffix "A" to type No.). Upon special request it is also available in the quad in-line package (Fig. 1b, add suffix "B" to type No.).

Characteristics per Divider Stage
at $V_7 = 9$ V, $R_L = 2.2$ kΩ, $T_{amb} = 25°C$

Characteristic			Unit
Supply current (low state at output)	I	< 3	mA
Input voltage high state (see Fig. 6)	V_i	6 . . . 9	V
Input voltage low state	V_i	< 1	V
Output voltage low state	V_o	< 0.1	V
Output voltage high state	V_o	> 7.0	V
Rise time of output voltage	t_r	< 0.2	us
Fall time of output voltage	t_f	< 0.2	us
Input resistance (see Fig. 7)	r_i	6 . . . 9	kΩ

Characteristics per Divider Stage
at V_7 = 9 V, R_L = 2.2 kΩ, T_{amb} = 25°C

Characteristic			Unit
Output resistance low state	r_o	> 1	MΩ
Output resistance high state	r_o	200	Ω

*) During resetting in accordance with Figs. 4 and 6 this value may be exceeded for a time less than 0.1 ms.

Recommended Operating Conditions			
Supply voltage	V_7	9	V
Max. input frequency	f_{imax}	50	kHz
Load resistance	R_L	2 . . . 20	kΩ

If the output voltage shape has to be modified for applications in electronic organs (see Fig. 3), a protective resistor R_S = 180 Ω, connected in series with the capacitor C_L, should be used. In this case the condition $R_L >> R_S$ must be met.

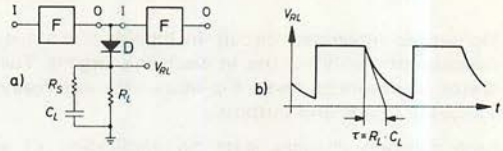


Fig. 3: Modification of the square-wave output voltage using RC networks.
a) Circuit diagram, D = Decoupling diode, e. g. BA 170
b) Shape of output voltage V_{RL}

On application in counter circuits resetting may be required. This can be accomplished by bringing all outputs to a potential less than 3 Volts with the inputs kept on 0 Volt as shown in Fig. 8, or more conveniently by bringing all imputs and outputs to a potential less than 1.5 Volts. The active edge of the reset pulse has to be fast enough to complete the resetting within less than 0.1 ms, otherwise the device may be overloaded. Fig. 4 shows a recommended circuit for resetting.

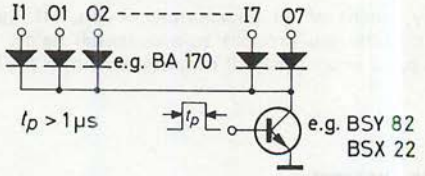


Fig. 4: Recommended reset circuit for counting applications.

Fig. 5:
Output voltage versus supply voltage.

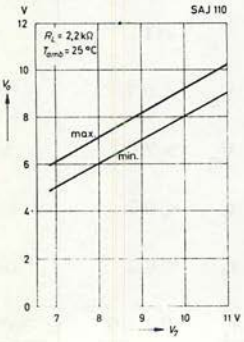


Fig. 6: Max. admissible and min. required value of input pulses (high state) versus supply voltage.

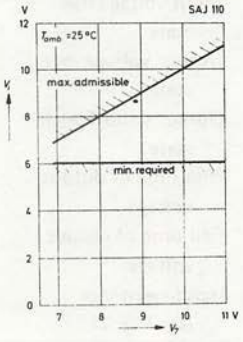


Fig. 7:
Input characteristic

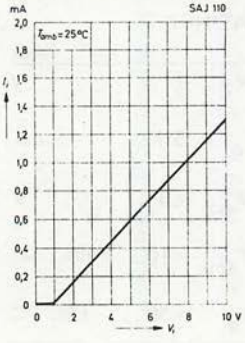
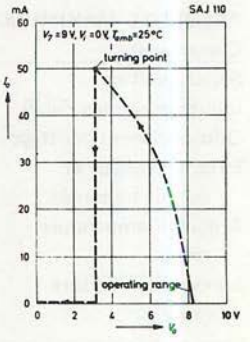


Fig. 8:
Output characteristic



SEVEN STAGE FREQUENCY DIVIDER POWER OSCILLATOR

The monolithic integrated circuit SAJ170 is intended for application in quartz-controlled clocks (wall and table models). The device consists of seven series-connected flip-flop stages, triggered by the positive-going edge of the respective input pulse. The SAJ170 may be driven either by sine-wave or by square-wave signals according to Fig. 3a and 3b.

For divisions by the usual factor 2^{14} (e. g. from 16,384 Hz to 1 Hz) it is necessary to use two SAJ170 connected directly in series.

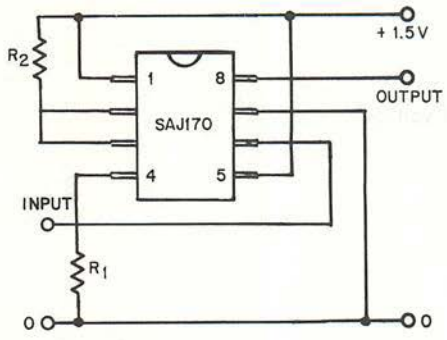


Fig. 1: Operating circuit of SAJ170.

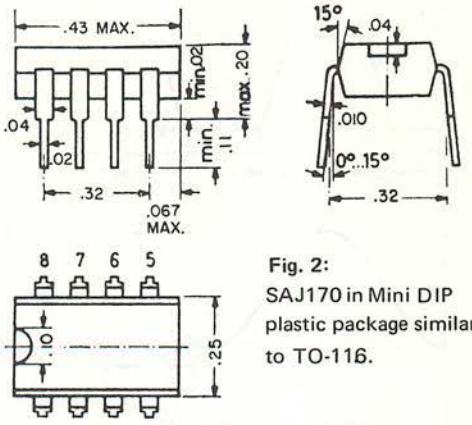


Fig. 2: SAJ170 in Mini DIP plastic package similar to TO-116.

All voltages are referred to terminal 7.

ABSOLUTE MAXIMUM RATINGS

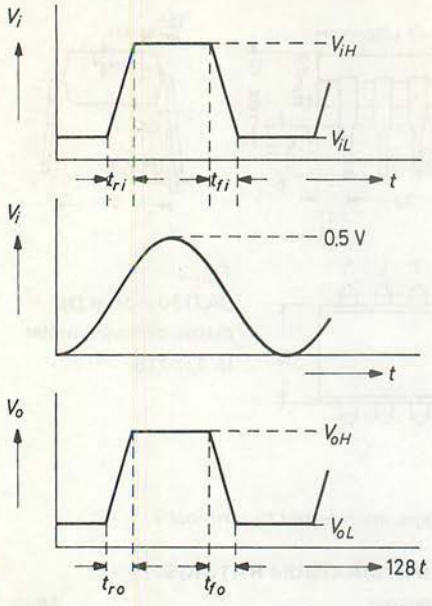
Characteristics	Units
Supply voltage	2 V
Ambient temperature range	-10 . . . +60 °C
Storage temperature range	-30 . . . +125 °C

ELECTRICAL CHARACTERISTICS @ $V_1 = V_5 = 1.5$ V, R1 = 680 kΩ, R2 = 270 kΩ, $T_{amb} = 25°C$

Characteristics			Units
Current consumption	$I_{1+2+3+5}$	17	uA
Divider ratio	f_i/f_o	128	
Output voltage high state	V_{oH}	0.55	V
Output voltage low state	V_{oL}	0.05	V
Rise time of output voltage	t_{ro}	10	us
Fall time of output voltage	t_{fo}	5	us

RECOMMENDED OPERATING CONDITIONS @ $T_{amb} = 25°C$

Characteristics			Units
Supply voltage	V_1, V_5	V1.2	V
Current consumption adjustable by R1	$I_{1+2+3+5}$	10 . . . 25	uA
Resistor for adjusting current consumption	R1	according to Fig. 4	
Input frequency	f_i	V50	kHz
Capacitive load at output	C_8	V30	pF
Input voltage high state	V_{iH}	0.4 . . . 0.6	V
Input voltage low state	V_{iL}	V0.1	V
Rise time of input voltage	t_{ri}	V20	us
Fall time of input voltage	t_{fi}	V10	us



a) Input voltage if driven by square-wave signal

b) Input voltage if driven by sinusoidal signal (only for $f_i > 8$ kHz)

c) Output voltage

Fig. 3: Input and output voltages of SAJ 170

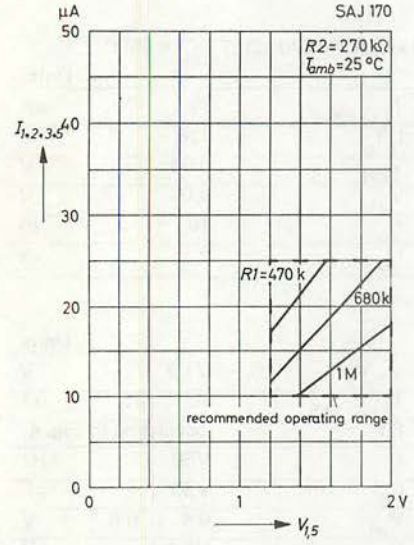


Fig. 4: Current consumption versus supply voltage

The monolithic integrated circuit SAK110 is designed for use in rev-counters of cars.

By use of suitable external circuitry the rev-counter can be adapted to engines with two to eight cylinders. It is designed for a nominal 12 V DC supply.

The heart of the SAK110 is a monostable flip-flop which converts the input signal (which can be derived, for example, directly from the contactbreaker) into square pulses with constant voltage and duration. Using an 8 mA moving-coil instrument it is possible to design a simple frequency meter.

The circuit is so designed that with the use of a suitable instrument the readings will be practically independent of temperature. The push-pull output allows for the use of instruments with high inductance moving coil even at high frequencies. A diode which is parallel to input terminal 2 and 3 prevents triggering by negative pulses.

The SAK110 can be triggered only by pulses exceeding 8 V supplied from a voltage-divider directly connected to contact-baker. Thus good noise immunity is obtained.

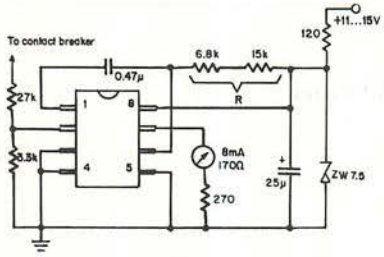


Fig. 1: Circuit diagram of a rev-counter with full scale deflection at 6000 RPM (two control pulses per turn of crank-shaft). Nominal voltage of car battery 12 V.

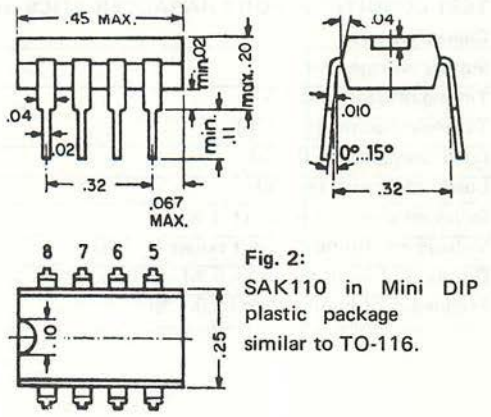


Fig. 2: SAK110 in Mini DIP plastic package similar to TO-116.

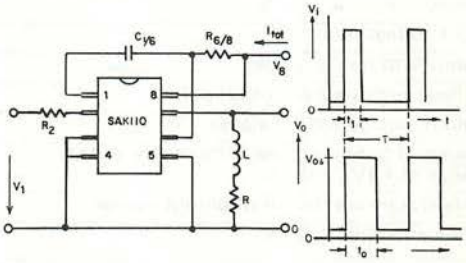


Fig. 3: Test Circuit.

All voltages are referred to terminals 3, 4 and 5.

ABSOLUTE MAXIMUM RATINGS

Characteristics	Units
Supply voltage	9 V
Currents	−20 mA
average value	2 mA
at pulse duration V0.5 ms	20 mA
at pulse duration V0.5 ms	75 mA
at pulse duration V0.5 ms	−75 mA
Ambient temperature range	-25 . . . +65 °C

RECOMMENDED OPERATING CONDITIONS

Characteristics			Units
Supply voltage	V_8	7.5 . . . 8	V
Frequency of input pulses	f_i	<10	kHz
Pulse duty factor of output voltage	t_o/T	<0.85	
Timing resistor	$R_{6/8}$	3 . . . 20	kΩ

TEST CONDITIONS FOR CHARACTERISTICS see test circuit Fig. 3

Characteristics			Units
Supply voltage (± 1 %)	V_8	8	V
Timing resistor (± 0.1 %)	$R_{6/8}$	10	kΩ
Timing capacitor (± 0.1 %)	$C_{1/6}$	0.47	µF
Load resistance (± 0.5 %)	R_L	440	Ω
Load inductance (± 5 %)	L	80	mH
Series resistance at input (± 1 %)	R_2	10	kΩ
Voltage amplitude of input pulses (± 2 %)	V_{is}	10	V
Duration of input pulses (± 5 %)	t_i	0.5	ms
Frequency of input pulses (± 0.1 %)	f_i	250	Hz

CHARACTERISTICS AT T_{amb} = 25°C. See preceding test conditions

Supply current at $V_i = 0$	I_{tot}	12 . . . 22	mA
Input voltage drop	$V_{2/3}$	6.5 . . . 8	V
Duration of output pulses	t_o	2.7 . . . 3.1	ms
Voltage amplitude of output pulses	V_{os}	5 . . . 5.8	V
Output voltage average vlaue	V_o	3.3 . . . 4.5	V
Change of output voltage for a supply voltage change of ± IV_8 = 0.3 V	$\pm\frac{\Delta V_o}{V_o}$	<2	%
Temperature coefficient of output voltage	a_{V_o}	$< 2 \cdot 10^{-3}$	1/°C
Residual output voltage	$V_{o\ res}$	<30	mV

At input frequencies in the range of f_i = 25 . . . 250 hZ:

Dependence of output voltage on the frequency $V_{o\ lin} = \frac{V_{o\ max} - V_{o\ res}}{f_{i\ max}} \cdot f_i + V_{o\ res}$

Deflection linearity error $\left|\frac{V_o - V_{o\ lin}}{V_{o\ max}}\right| < 0.3\ \%$

Definitions:

V_o = actual value of output voltage (average value)

$V_{o\ lin}$ = nominal value of output voltage

$V_{o\ max}$ = final value of output voltage at $f_i = f_{i\ max}$ = 250 Hz (full scale deflection)

The duration of the input pulses must always be shorter than the duration of the output pulses.

POWER OSCILLATOR

Monolithic integrated circuit in bipolar technique. Particularly suited as electronic pulse generator for direction blinker and emergency blinker in cars with 12V DC supply. Also suited for other applications, e.g. for interval wind-screen wipers.

The TAA 775 G is an oscillator, the frequency of which is determined by an external RC network and which supplies rectangular output pulses. The output terminal 10 is connected to the collector of the output transistor operating in common emitter configuration. An integrated diode between the collector of the output transistor and the supply voltage terminal 1 allows for operation with inductive loads.

As can be seen from the terminal diagram Fig. 1, the TAA 775 G has two oscillator input terminals 5 and 6, for the connection of the frequency-determining RC network. By applying a suitable control voltage to the control input (terminal 7) the following operating modes are possible (see Fig. 5):

a) Operation at nominal frequency f_o

b) Operation at increased frequency f'_o

c) Oscillator not oscillating

When a control voltage for operating mode a) or b) is applied, oscillation starts in the on-state. Since the control voltage is effective only during the off-state, blocking of the oscillator in the on-state is possible only at the end of the normal on-state.

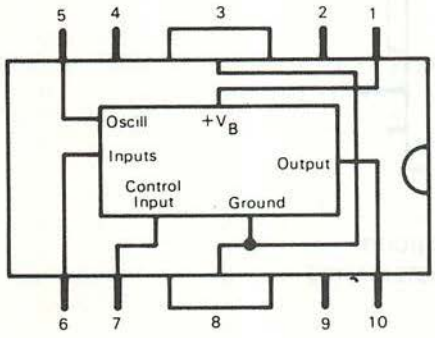
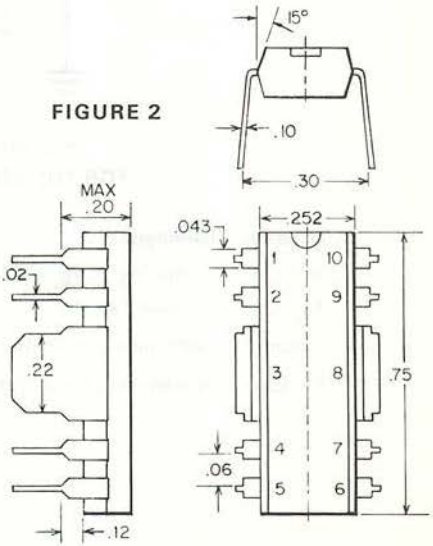


FIGURE 1 – TERMINAL DIAGRAM OF TAA 775 G

The TAA 775 G is supplied in a modified dual in-line plastic package. Instead of the three central connection pins a connection fin of suitable width serving as ground terminal is lead out on both sides (see Fig. 2).

FIGURE 2



ABSOLUTE MAXIMUM RATINGS

Characteristics	Unit
Supply Voltage	15 Volts
Control Voltage	$<V_1$
External Voltage on Terminal 10	$<V_1$
Output Current	150 mA
Ambient Temperature Range	−25...+85°C

STATIC CHARACTERISTICS @ V_1 = 12 Volts: $V_3 = V_8$ = 0 Volt T_{amb} = 25°C (see Fig. 3)

Characteristics	Unit
Average Current Consumption	8 mA
Leakage Current of the Oscillator Input at V_5 = 0 Volt	<1 μA
Required Oscillator Input Current for Turning on the Oscillator Output	>10 μA
Output Saturation Voltage in the On-State at I_{10} = 110 mA	<1 Volt
Output Leakage Current in the Off-State at $V_{10} = V_1$ and V_5 = 0 Volt or $V_7 = V_1$	<1 μA

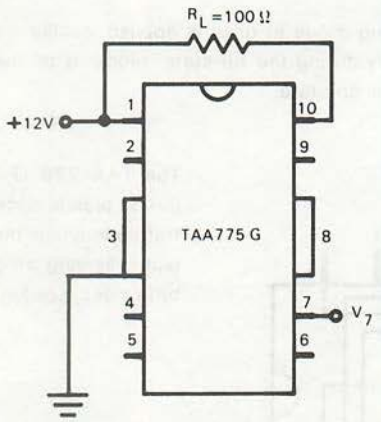


FIGURE 3 – TEST CIRCUIT FOR THE STATIC CHARACTERISTICS

Dynamic Characteristics

at V_1 = 12 Volts, $V_3 = V_8$ = 0 Volt,

T_{amb} = 25°C (see Fig. 4)

Frequency-determining resistor – $R_{5/6}$	1...120	kΩ
Frequency-determining capacitor – C_5	optional, but the leakage current of the capacitor must be taken into consideration.	

Oscillator frequency (see Fig. 5)

at V_7 = 0...0.35 Volt $\quad f_o = \frac{800}{R_{5/6} \cdot C_5}$ Hz $\quad R_{5/6}$ in kΩ, C_5 in uF

at V_7 = 0.45...5 Volts $\quad f'_o = 2.2\, f_o$

at V_7 = 8 Volts...V_1 $\quad f''_o = 0$; output transistor blocked

on/off ratio (see Fig. 5)

at V_7 = 0...0.35 Volt $\quad t_{on}/t_{off} = 0.8$

at V_7 = 0.45...5 Volts $\quad t'_{on}/t'_{off} = 1.1$

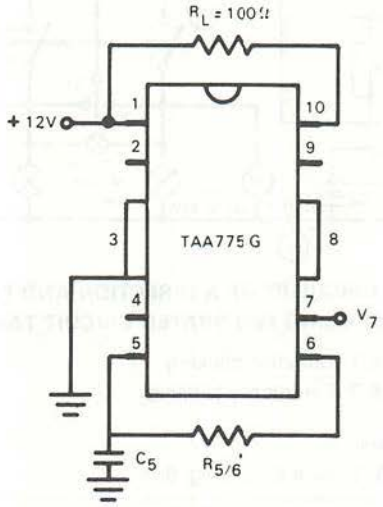
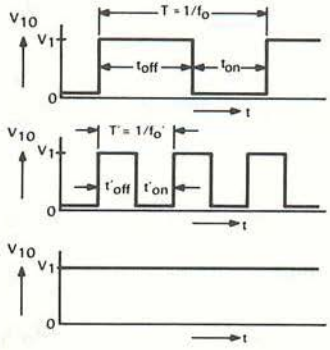


FIGURE 4 – TEST CIRCUIT FOR THE DYNAMIC CHARACTERISTICS



V_7 = 0...0.35 Volt

V_7 = 0.45...5 Volts

V_7 = 8 Volts...V_1

FIGURE 5 – OPERATION OF THE CONTROL INPUT 7 (STEADY STATE)

Application as directional and emergency blinker (see Fig. 6)

In conjunction with a frequency-determining RC network (e.g. $R_{5/6}$ = 5.6 kΩ, C_5 = 100 µF/6 Volts) and a relay (coil resistance min. 100Ω) the TAA 775 G replaces a conventional hot wire interval switch and a current monitoring relay. The previous arrangement of the terminals on the blinker realy package (plus and minus pole of the battery and connection to steering-wheel changeover switch) can be retained. In the case of direction blinking, the bulbs are monitored: the breakdown of a bulb causes a greatly increased blink frequency. The capacitor C_6 prevents battery voltage transients affecting the operation of the TAA 775 G.

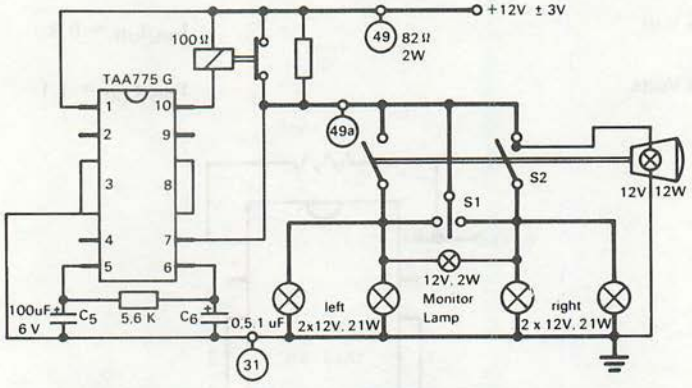


FIGURE 6 – CIRCUITRY OF A DIRECTION AND EMERGENCY BLINKER USING INTEGRATED CIRCUIT TAA 775 G

S 1: Direction blinking
S 2: Emergency blinking

Characteristics of Blinker Circuit

At V_1 = 12 Volts, T_{amb} = 25°C, as in Circuit Fig. 6

Operation starts with a bright interval			
Duration of the first bright interval	t	<1	Sec
Nom. frequency in normal operating with two 21 Watt bulbs	f_o	85	Min^{-1}
Nom. frequency in emergency operation with four 21 Watt bulbs	f_o	85	Min^{-1}
Ratio of on-time to total period at nom. frequency	ν	45	%
Dependence of operating frequency on the supply voltage in the range of 9 to 15 Volts	$\pm\Delta f_o/f_o$	<2	%
Control of the lamps:			
Defect in one of the two direction indicating lamps causes an increase of the blink frequency by the factor	$\Delta f_o'/f_o$	2.2	–
Ratio of on-time to total period in the case of increased frequency	ν'	52	%

Other applications

The frequency and the on/off ratio of the output voltage can be varied within a wide range by variation of the time-determining RC network. For the charging resistor R_a and the discharging resistor R_e the following conditions must be met:

$$1\ k\Omega < R_a < 120\ k\Omega$$

$$1\ k\Omega < R_e < 120\ k\Omega$$

The TAA 775 G can be used for frequencies up to 20 kHz. The approximate equations given below are, however, only valid for frequencies up to 4 kHz. Fig. 7 gives the output voltage wave form with load resistor connected.

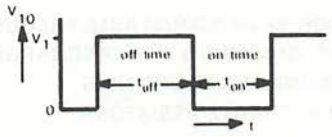


FIGURE 7 – BEHAVIOR OF THE OUTPUT VOLTAGE AS A FUNCTION OF TIME

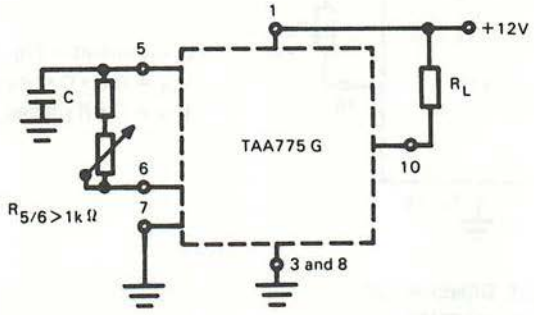


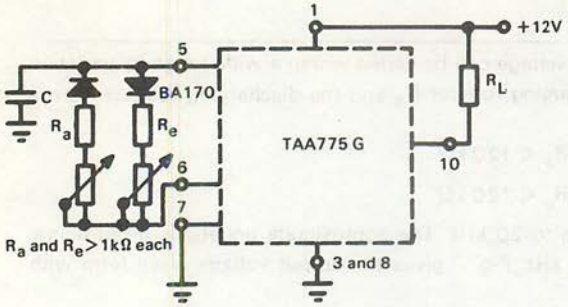
FIGURE 8 – AS PULSE GENERATOR WITH ADJUSTABLE FREQUENCY AND CONSTANT ON/OFF RATIO. CHARGING AND DISCHARGING OF THE TIME-DETERMINING CAPACITOR THROUGH THE SAME RESISTOR

For the circuit in Fig. 8 these equations are valid:

$$T = 1/f_o = \frac{R \cdot C}{800}\ \text{sec} \quad \begin{matrix} R \text{ in } k\Omega \\ C \text{ in } \mu F \end{matrix}$$

$$t_{on} = 0.45\ T$$

$$t_{off} = 0.55\ T$$

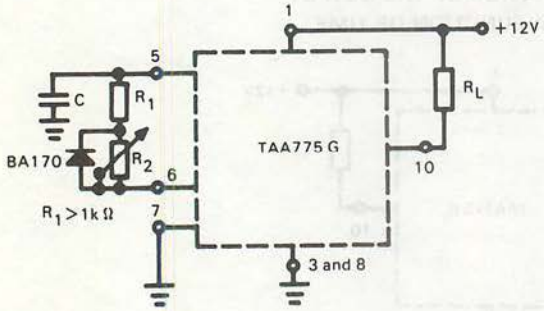


For the circuit in Fig. 9 these equations are valid:

$t_{on} = 0.7 \cdot C \cdot R_e$ msec R in kΩ

$t_{off} = C \cdot R_a$ msec C in μF

FIGURE 9 – AS PULSE GENERATOR WITH ADJUSTABLE FREQUENCY AND ADJUSTABLE ON/OFF RATIO. CHARGING AND DISCHARGING OF THE TIME-DETERMINING CAPACITOR IS EFFECTED THROUGH SEPARATE RESISTORS.

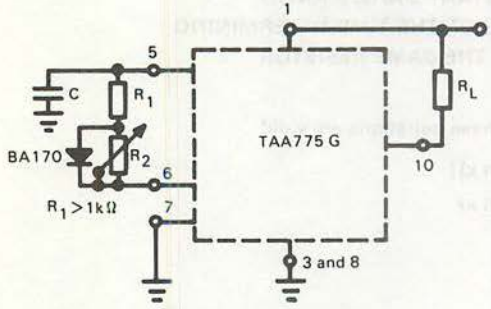


For the circuit in Fig. 10 these equations are valid:

$t_{on} = 0.6 \cdot C \cdot (R_1 + R_2)$ msec R in kΩ

$t_{off} = C \cdot R_1$ msec C in μF

FIGURE 10 – AS PULSE GENERATOR WITH ADJUSTABLE ON-TIME



For the circuit in Fig. 11 these equations are valid:

$t_{on} = 0.7 \cdot C \cdot R_1$ msec R in kΩ

$t_{off} = 0.75 \cdot C \cdot (R_1 + R_2)$ msec C in μF

FIGURE 11 – AS PULSE GENERATOR WITH ADJUSTABLE OFF-TIME

WIND-SHIELD WIPER

The interval wind-shield wiper circuit is shown in circuit Fig. 12. The pause duration between two consecutive wiping operations can be continously adjusted.

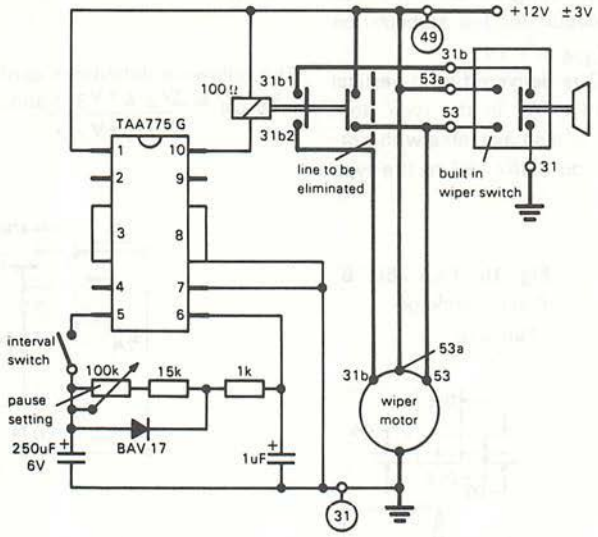


FIGURE 12 – CIRCUIT OF AN INTERVAL WIND-SHIELD WIPER USING TAA 775 G.

Characteristics of the circuit in Fig. 12

At V_1 = 12 Volts, T_{amb} = 25°C

On-time (constant)	0.2 sec
Off-time (adjustable)	4 to 20 sec

1.1V Stabilizing Circuit

Monolithic integrated circuit, e.g. for the stabilization of the operating point in transistor circuits and for the voltage-stabilized drive of clocks. The circuit comprises the operating transistor T1 (see fig. 2) and a control circuit for the stabilization of the output voltage $V_{3/4}$ to 1.1V.

Normally the TAA 780 is delivered with vertical leads (Fig. 1a, add suffix "A" to the type No.). Upon special request it is also available with horizontal leads (Fig. 1b, add suffix "B" to the type No.).

Fig. 1a: TAA 780 "A"
Plastic package
"Pancake"

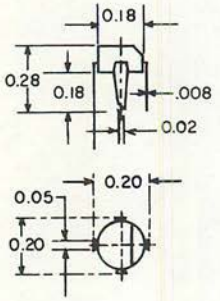
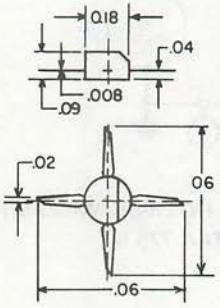


Fig. 1b: TAA 780 "B"
Plastic package
"Pancake"



All characteristics and maximum ratings indicated below refer to the test circuit (Fig. 2) shown below. The figure 0 in the index of some characteristics means that in this case all other terminals are open.

The following definitions apply:

$$S_{V3/4} = \frac{\Delta V_{2/4} \cdot V_{3/4}}{\Delta V_{3/4} \cdot V_{2/4}} \text{ and } \alpha_{V3/4} = \frac{\Delta V_{3/4}}{V_{3/4} \cdot \Delta T_{amb}}$$

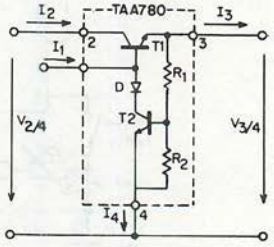


Fig. 2: Circuit Diagram and Test Circuit

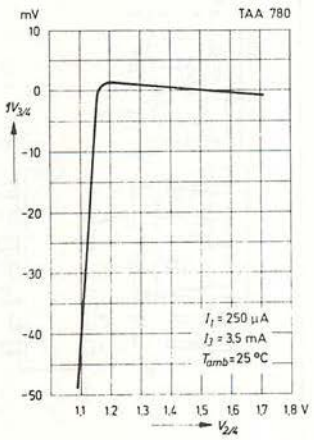
T1 ..... Operating transistor
T2 ..... Regulation transistor
D ..... Blocking diode
R1, R2 ..... Voltage divider

ABSOLUTE MAXIMUM RATINGS

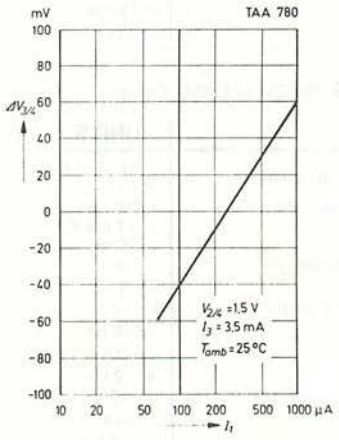
Characteristics	Unit
Collector-Base Voltage	3 Volts
Collector-Emitter Voltage @$R_{1/3}$ = 5 k ohms (ext. connected)	2 Volts
Emitter-Base Voltage	2 Volts
Substrate-Base Voltage	2 Volts
Collector Current	15 mA
Stabilizing Current	1 mA
Ambient Temperature Range	−20 to +40°C
Storage Temperature Range	−20 to 125°C

ELECTRICAL CHARACTERISTICS @ $T_{amb} = 25°C$	UNITS
DC Current Gain of Transistor T1	
@ $V_{2/3} = 1.5V, I_2 = 0.3$ mA, $I_4 = 0$	250(> 120)
Collector-Saturation Voltage of Transistor T1	
@ $I_2 = 3.5$ mA, $I_1 = 35\,\mu$A, $I_4 = 0$	0.1 (> 0.12) Volt
Base-Saturation Voltage of Transistor T1	
@ $I_2 = 3.5$ mA, $I_1 = 35\,\mu$A, $I_4 = 0$	0.7 Volt
Total Resistance of Voltage Divider	15 (> 10) k ohms
Stabilized Voltage	
@ $V_{2/4} = 1.5V, I_1 = 250\,\mu$A, $I_3 = 3.5$ mA	1.1±0.06 Volt
Voltage Stabilization Coefficient	
@ $V_{2.4} = 1.3$ to 1.7V, $I_1 = 250\,\mu$A, $I_3 = 3.5$ mA	−200
Temperature Coefficient of the Stabilized Voltage	
@ $V_{2/4} = 1.5V, I_1 = 250\,\mu$A, $I_3 = 3.5$ mA	$-2.8 \cdot 10^{-3}/°C$
Small Signal Current Gain of Transistor T1	
@ $V_{2/3} = 1.5V, I_2 = 0.3$ mA, $I_4 = 0$	250

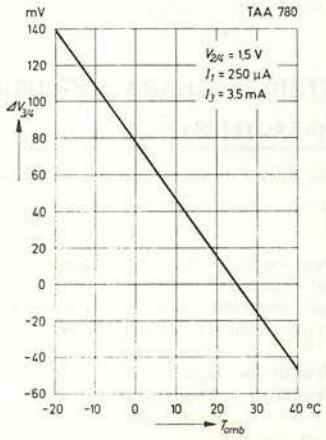
Variation of output voltage $V_{3/4}$ versus input voltage $V_{2/4}$, referred to $V_{2/4} = 1.5$ V, $V_{3/4} = 1.1$ V



Variation of output voltage $V_{3/4}$ versus current I_1 referred to $I_1 = 250\,\mu$A, $V_{3/4} = 1.1$ V



Variation of output voltage $V_{3/4}$ versus ambient temperature referred to $T_{amb} = 25°C$, $V_{3/4} = 1.1$ V



MULTI-FUNCTION IC FOR TV RECIEVERS

- **Sync Separator**
- **A F C**
- **Horizontal Oscillator**
- **A P C**
- **Noise Suppression**

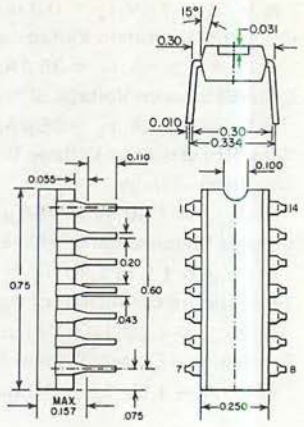
MAXIMUM RATINGS @ 25°C Case Temperature

CHARACTERISTICS		UNITS
Ambient temperature	T_a	0 . . . 60°C
Junction temperature	T_j	< 125°C
Currents: power supply	I_{13}	< 10 mA
signal inputs	I_8	< 1 mA
signal inputs	I_9	< 1 mA
signal inputs	I_5	< 5 mA
signal outputs	I_1	< 10 mA
signal outputs	I_7	< 10 mA
Voltages: supply voltage	V_2	< 10 mA
composite video signal	V_P	0 to < +6 V

ELECTRICAL CHARACTERISTICS @ 25°C Case Temp.

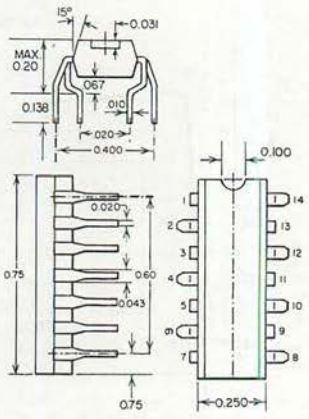
CHARACTERISTICS		UNITS
Input current of the synch separator stage, connection (9)		$+20\ \mu A < I_9 > +1$ mA
Input current of the noise suppressor, connection (8)		$-100\ \mu A < I_8 > -1$ mA $R_{2\text{-}8} \approx 27$ kΩ
Output current of the synch separator, connection (7)		I_7 6 mA
Load resistance		$R_{2\text{-}7}$ 1 kΩ
Amplitude of the line synch and frame pulse at output 7		V_7 +6 V
Nominal frequency of the oscillator		15750 Hz
Output of the oscillator:	Pulse current	I_1 3 mA
	Load resistor	$R_{1\text{-}14}$ 2 kΩ
	Amplitude	V_1 +2 V
	Pulse width	t_1 14 μs
Pull-in range		> ± 1 kHz
Hold-in range		> ± 2 kHz
Slope of the AFC-circuit		> 1 kHz/0.5 μs
Phase shift between oscillator output pulse and synch pulse (defined as the time between the leading edges of these pulses with the oscillator aligned to the nominal frequency).		$t_0 = 1.2\ \mu$s

PHYSICAL DIMENSIONS



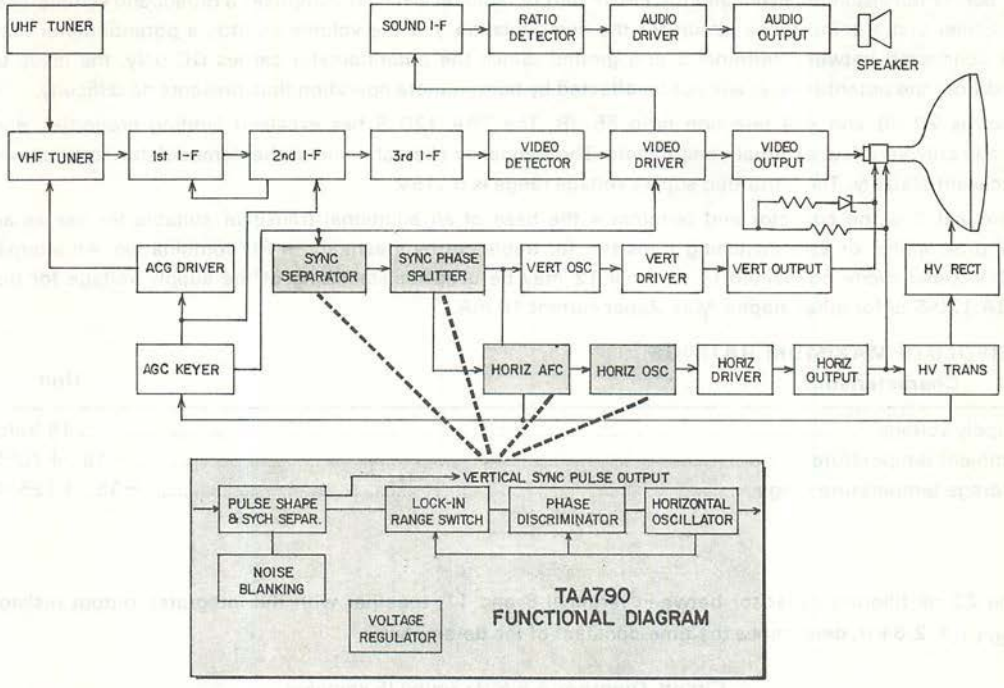
DUAL IN-LINE

PHYSICAL DIMENSIONS

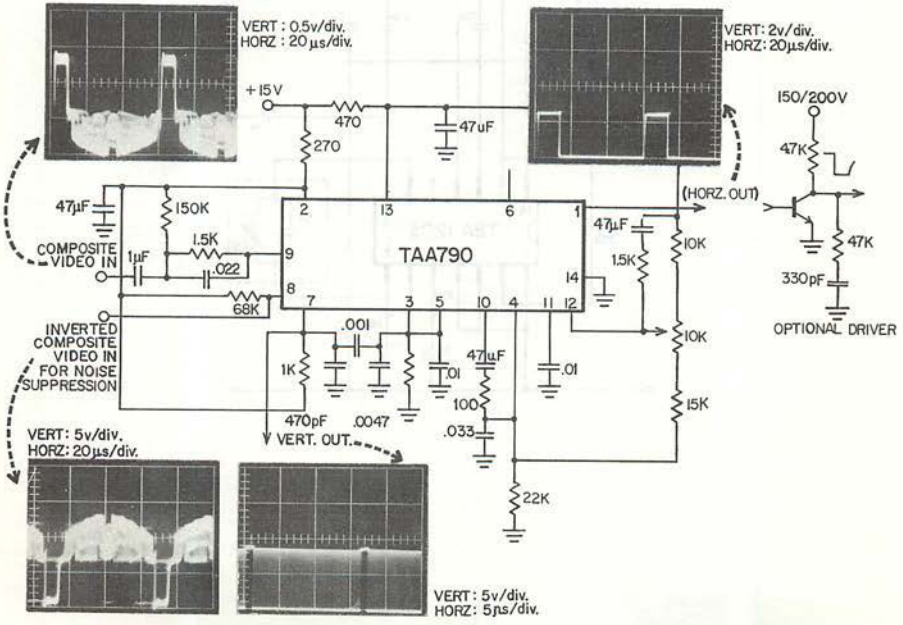


QUAD IN-LINE

BLOCK DIAGRAM OF A TELEVISION RECIEVER



NECESSARY EXTERNAL COMPONENTS



TBA120S

INTEGRATED FM/IF AMPLIFIER AND DEMODULATOR

Package: TO-116
Quad in-line

The monolithic integrated FM/IF amplifier TBA 120 S is designed specifically for use in the sound IF part of television receivers and the FM/IF part of radio receivers. It comprises a broadband symmetrical amplifier and a coincidence circuit for the demodulation. For the volume control, a potentiometer may be connected between terminal 5 and ground. Since the potentiometer carries DC only, the leads to and from the potentiometer will not be affected by hum; remote operation thus presents no difficulty.

Gain is 70 dB and AM rejection ratio 65 dB. The TBA 120 S has excellent limiting properties, and needs only very few external components. The frequency characteristic of the demodulator curve shows excellent stability. The permitted supply voltage range is 5...15V.

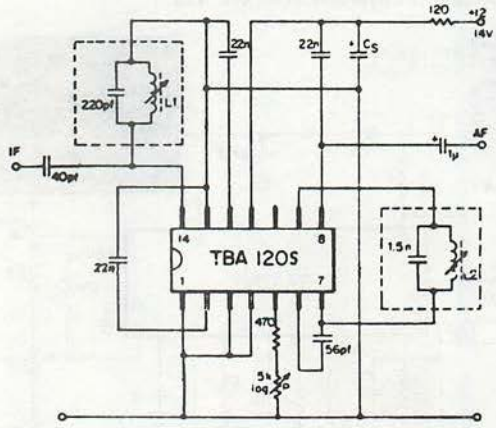
Terminal 3 is the collector and terminal 4 the base of an additional transistor suitable for use as an AF preamplifier or as a switching transistor for treble cut by means of an RC combination. An internal 12 V Zener diode connected to terminal 12 may be used for stabilizing of the supply voltage for the TBA 120 S or for other stages. Max. Zener current 10 mA.

ABSOLUTE MAXIMUM RATINGS

Characteristics	Unit
Supply voltage	15 Volts
Ambient temperature range	−15...+70°C
Storage temperature range	−35...+125°C

The 22 nF filtering capacitor between terminal 8 and 11, together with the integrated output resistor $R_{8/11} = 2.6\ k\Omega$, determines the time-constant of the de-emphasis.

Circuit Diagram 4.5 MHz sound IF amplifier



ELECTRICAL CHARACTERISTICS @ V_{11} = 12 Volts, f_i = 0.5 MHz, P = 5 kΩ, T_{amb} = 25°C

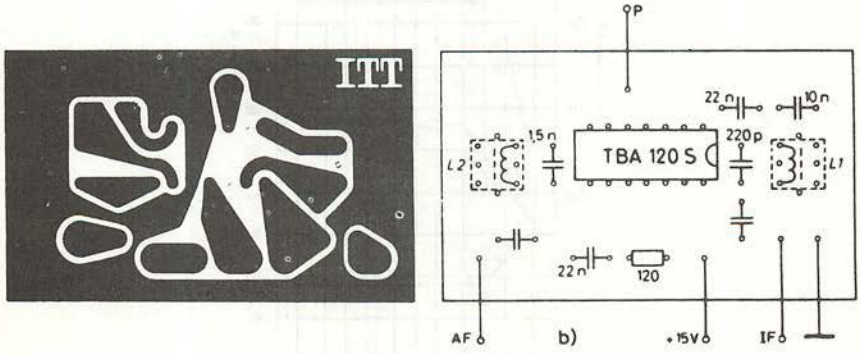
Characteristics	Unit
Recommended range of supply voltage	5...15 Volts
Current consumption	16.5 mA
IF voltage gain	70 dB
Limiting IF output voltage	240 mV
AF output voltage	
@ Δf_i = ± 50 kHz, V_i = 10 mV, f_{AF} = 1 kHz, Q = 45	1.7 Volts
@ Δf_i = ± 25 kHz, V_i = 10 mV, f_{AF} = 1 kHz, Q = 45	0.85 Volt
Distortion	
@ Δf_i = ± 25 kHz, V_i = 10 mV, f_{AF} = 1 kHz, Q = 45	1.8%
Input voltage for start of limitation	
@ Δf_i = ± 50 kHz, f_{AF} = 1 kHz, Q = 45	30 (<60) μV
Input impedance	
@ f_i = 4.5 MHz	20 kΩ parallel to 6 pF
@ f_i = 10.7 MHz	10 kΩ parallel to 5 pF
Output resistance	2.6 kΩ
Volume control range	75 dB
DC level of output signal at V_i = 0	7.3 Volts
AM rejection ratio	
@ Δf_i = ± 50 kHz, V_i = 10 mV, f_{AF} = 1 kHz, m = 30%	65 dB
@ Δf_i = ± 50 kHz, V_i = 200 μV, f_{AF} = 1 kHz, m = 30%	55 dB

Coil data for Circuit Diagram

Coil assemblies: 7mm x 7mm Neosid miniature filters

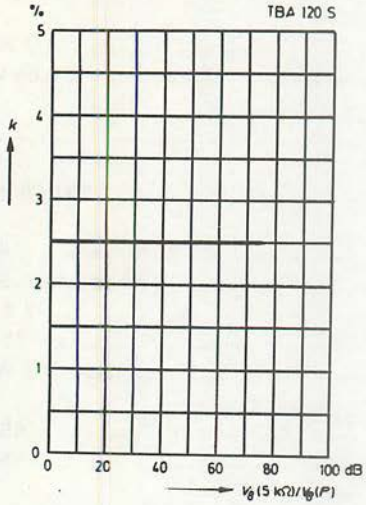
Input coil L1:
12 turns, 0, 1 mm ∅ En. Cu
Material of the core: F 10 B
$Q_0 \approx 80$

Demodulator coil L2:
4 turns, 0, 1 mm ∅ En. Cu
Material of the core: F 2
$Q_0 \approx 45$

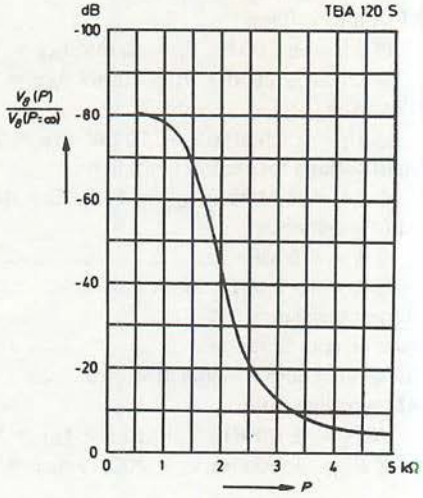


Printed circuit board for circuit diagram, scale 1:1
a) copper foil side b) component side

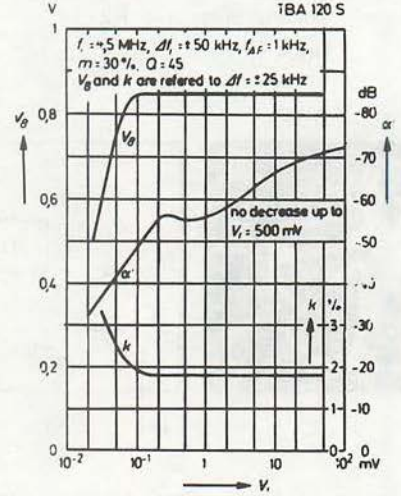
Distortion versus volume control



Volume control versus potentiometer resistance

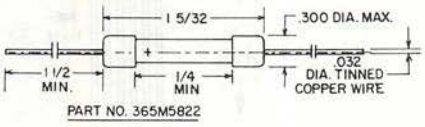


AF output voltage, distortion, and AM rejection ratio versus input voltage

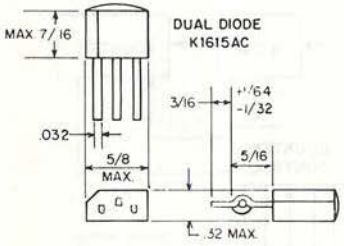


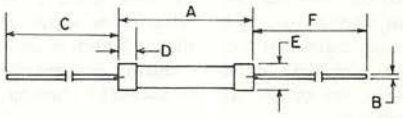
HIGH VOLTAGE SELENIUM RECTIFIERS FOR CONSUMER APPLICATIONS
(Half-Wave unless specified)

PART NO.	PIV—Based on 16 kHz application	OUTPUT— Tests point	FUNCTION
365M5822	800V	4mA	Color TV Boost Rectifier
K1615AC*	20V	2mA	Horizontal Osc.
034	1200V	4mA	Color TV Boost Rectifier
073	17,250V	3mA	Hi Voltage Rectifier
088	24,000V	3mA	Hi Voltage Rectifier
TV6.5	8,500V	3mA	Focus Rectifier
TV9-6K60	11,700V	3mA	Hi Voltage Rectifier
TV11-6K70	14,650V	3mA	Hi Voltage Rectifier
TV13-11K60	17,250V	3mA	Hi Voltage Rectifier
TV18-10K70	24,000V	3mA	Hi Voltage Rectifier
TV18-10K80	24,000V	3mA	Hi Voltage Rectifier
TV20-10K80	26,500V	3mA	Hi Voltage Rectifier



PART NO. 365M5822





Part No.	A	B	C	D	E	F
034	.820 +.086 -.180	.034 ±.004	.50 MIN.	.168 ±.078	.284 MAX.	.50 MIN.
073	3.345 ±.06	.032 ±.004	.50 MIN.	.236 ±.012	.228 ±.008	——
088	2.785 ±.06	.032 ±.004	.50 MIN.	.158 ±.012	.228 ±.008	——
TV6.5	1.98 ±.06	.03	1.50 ±.04	.236	.23 ±.008	1.50 ±.04
TV9-6K60	2.36 ±.06	.03	1.50 ±.04	.236	.23 ±.008	1.50 ±.04
TVII-6K70	2.76 ±.06	.03	1.50 ±.04	.236	.23 ±.008	1.50 ±.04
TVI3-IIK60	3.35 ±.06	.03	1.50 ±1.50	.236	.23 ±.008	1.50 ±.04
TVI8-IOK70	2.758 ±.06	——	——	.236	.23 ±.008	——
TVI8-IOK80	3.15 ±.06	——	——	.236	.23 ±.008	——
TV20-IOK80	3.15 ±.06	——	——	.236	.23 ±.008	——

SAH215
TELEPHONE PUSH-BUTTON DIALLING IC

MONOLITHIC INTEGRATED CIRCUIT IN MOS TECHNOLOGY FOR USE IN TELEPHONE SETS WHEN DIALLING PUSH-BUTTONS.

- **The off-normal relay is released during the interdigital pause**
- **Decoding by means of ROM gives flexible code**
- **Pulse storage with individual or block-wise recalling of numbers**
- **Two different dial pulse ratios available**
- **Two different inter digital pauses available**

The SAH215 - Design and Operation

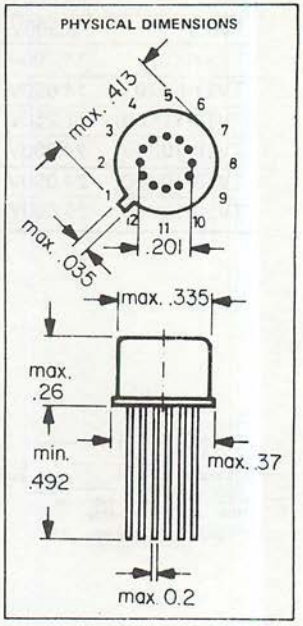
This circuit makes it possible to design push-button dialling telephone sets for connection to conventional telephone networks (quickstep-dialling).

The SAH215 controls a relay the contact of which generates the dialling pulses. It also controls a second relay which performs the function of the o. n. (off-normal) contact, i. e. short-circuits the receiver during the dialling operation. The supply source is a nickel/cadmium accumulator which is charged from the telephone network during conversations. Both relays are driven by the SAH215 through external transistors.

The MOS circuit requires a two-phase clock generator which delivers two non-overlapping clock pulses having an amplitude of approximately - 18 V. Its power consumption can be kept to the extremely low value of less than 4 mW.

Pin Configuration

1 Case, substrate, ground
2 o. n. output
3 d. p. output
4 Reset input
5 Strobe input
6 External register control input
7 Clock t1
8 Clock t2
9 Input A
10 Input B
11 Input C
12 Input D
13 Option t_z (ground-833/ open=433)
14 Option $t_{p/T}$ (ground=0.62/ open=0.66)



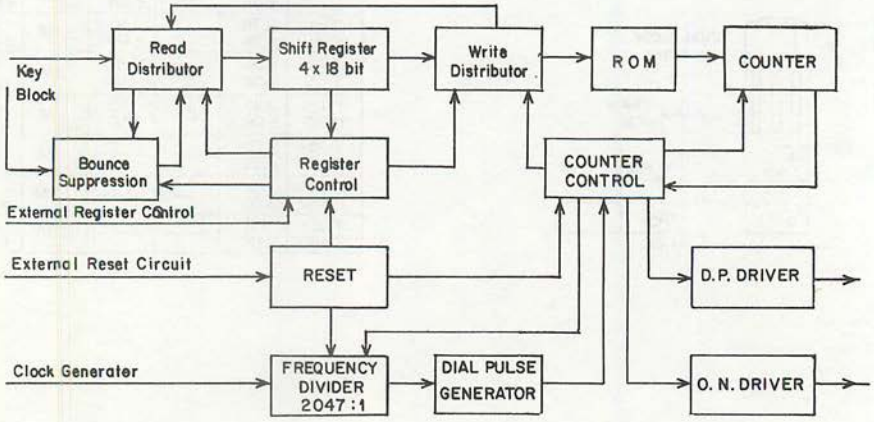


FIG. 1: Block diagram of the SAH215

Fig. 1 shows the block diagram of the SAH215. Four-bit data arriving from the key block are fed in parallel to the shift register via the read distributor. This register consists of four parallel individual registers of 18 bits each and serves for storing a maximum of 18 figures. A bounce-suppression circuit prevents a dialled figure from being written into the register more than once, due to contact bounce in the key block. The register control unit ensures the proper writing and reading sequence.

Through the write distributor the data are taken to a read only memory (ROM) which operates as a decoder and sets a counter in accordance with the entered figure. Through the counter control unit, the dial pulse generator transmits the number of pulses for which the counter was set to the d. p. (dial pulse) driver and drives the d. p. relay, maintaining the proper pulse duty factor. The counter control unit maintains the required interval between the several pulse trains and controls the o. n. relay via the o. n. driver.

The dial pulse generator frequency is derived from the clock frequency by means of a 2047 : 1 frequency divider. For the customary dialling frequency of 10 Hz the required clock frequency is therefore 20.47 kHz.

When applying the supply voltage to the MOS circuit, all stages of the control units have to be reset. This is achieved by a built-in reset unit. The reset time is determined by an external circuit (e. g. an RC-network).

The information in this data sheet relates to "negative logic", i. e. the more negative voltage level (Low) stands for logic "1", and the more positive voltage level (High) for logic "0". The symbol "X" may be an "0" or a "1"

When using a key block in which each key is provided with two ordinary contacts and one positively controlled n. o. (non-overlapping) contact it is possible to control the integrated circuit directly. The same applies to a key block with row and column switches each of which is provided with a common positively controlled n. o. contact. The positively controlled n. o. contacts which close after the other n. o. contacts and open before the other n. o. contacts, control the strobe input 5. Key blocks of different design may be adapted by using a diode matrix. A general requirement for key blocks is that the data signals must be free from bounce prior to the strobe signal as each key is depressed.

Further possibilities of adaptation are introduced by mask variations which enable any desired four-bit code to be set, as long as the tetrades 1111 and 1110 do not occur, because they are needed for register control.

An additional facility

In normal use the terminal 6 is not loaded. This corresponds to a logic "1", if a logic "0" signal is applied to this terminal the register output is blocked and the data made to circulate in the register. In this way, up to 17 figures can be stored. By applying appropriate pulse patterns to terminal 6 individual figures or figure blocks may be recalled. The input of data is not affected by a signal being applied to terminal 6, so that the storage of figures can continue.

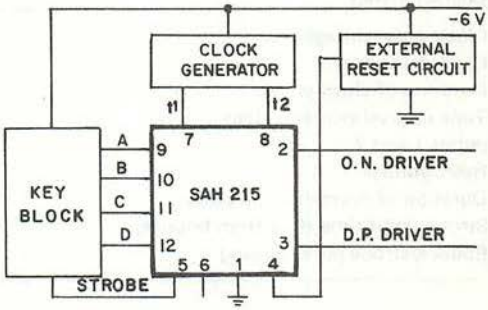


FIG. 2: Block diagram of the general layout

The SAH215 operates with the following code:

Figure	D	C	B	A
1	0	0	0	0
2	0	0	0	1
3	0	0	1	0
4	X	1	0	0
5	0	1	X	1
6	0	1	1	0
7	1	0	0	0
8	1	X	X	1
9	1	0	1	0
0	0	0	1	1

ABSOLUTE MAXIMUM RATINGS

Characteristics			Units
Voltages, clock pulse 1, clock pulse 2	V_7, V_8	-30 . . . +0.3	V
Input voltages Inputs 4, 5, 9, 10, 11 and 12	V_{in}	-30 . . . +0.3	V
Output current	I_2, I_3	-5	mA
Ambient temperature range	T_{amb}	-40 . . . +70	°C

RECOMMENDED OPERATING CONDITIONS

Characteristics			Units
Clock pulse voltages	V_{7M}, V_{8M}	-18	V
Clock frequency	f_t	20 (10 . . . 50)	kHz
Duration of clock pulses	t_t	> 5	us
Time interval between clock pulses 1 and 2	t_a	> 3	us
Reset voltage	$-V_4$	< 3	V
Duration of normalisation pulse	t_4	> 1	ms
Strobe input time (free from bounce)	t_E	> 17	ms
Bounce/strobe pulse spacing	t_B	< 7	ms

Characteristics						Units
at $V_{7M} = V_{8M} = -18$ V, $T_{amb} = 25$ °C						
Input voltages						
Inputs 4, 5, 9, 10, 11 and 12						
Logic "0"	V_{in}			Terminal open		
Logic "1"	V_{in}			-6 (-5 . . . -12)		V
Input 6						
Logic "0"	V_{in}			0 . . . -3		V
Logic "1"	V_{in}			Terminal open		
Input cutoff current at $V_{in} = -12$ V	$-I_R$			< 5		uA
Output frequency	f_{out}			$f_t/2047$		
Power consumption	P_{tot}			< 4		mW
Capacitance of clock inputs	C_7, C_8			< 150		pF
	Type:	1	2	3	4	
Dial break ratio of dial pulses	t_p/T	0.66	0.62	0.66	0.62	
Interdigital pause at $f_t = 20$ kHz	t_z	833	838	433	438	ms

ITT SAJ110 IN FREQUENCY DIVIDER CIRCUITS

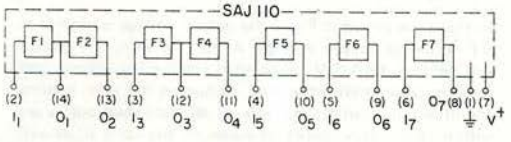
1. Introduction

Integrated digital frequency dividers have for long been widely used in professional digital equipment but have so far found little application in the entertainment sector of the electronic industry. This, no doubt, is due to the fact that the devices presently available do not quite meet the specific requirements of the consumer market, and that they were, until recently, rather expensive. Advances in integration techniques have now made it possible to produce inexpensive linear, as well as digital integrated circuits which should be of special interest to the electronic consumer industry. These devices offer many advantages when compared with circuits employing discrete components and are in many instances already cheaper. It is certain that the availability of these new integrated circuits will lead to rapid new developments in all branches of the electronic industry.

The new monolithic integrated frequency divider circuit SAJ 110, developed by ITT Semiconductors, incorporates seven divider stages which can be used either individually or interconnected to form a divider chain. Because the SAJ 110 requires no additional components and can be used in place of conventional discrete-component flipflop dividers, its use as a frequency divider in electronic organs is particularly advantageous.

2. The Integrated Circuit SAJ 110

Integration of a conventional flipflop circuit would offer virtually no advantage over a discrete component circuit – only a circuit which does not incorporate capacitors or other charge-storing elements is suitable for integration. Because the master slave flipflop (a frequency divider often used in digital equipment) is far too complex for consumer applications, development of a new circuit was necessary. This circuit had to function in a similar manner to a conventional flipflop but had to be designed so that no additional charge-storing elements were required. The result is a device which combines seven single divider stages on a single chip.



SAJ 110 Block diagram – The figures in brackets are the same as the pin numbers of package

In order to make maximum use of the 14 connections available on a TO-116 package the pins are connected as shown in Fig. 1, being arranged so that access to two divider pairs and three single divider stages is possible. The circuits can thus be used either singly or interconnected in various combinations.

Figs. 2a and 2b give dimensioned outline drawings of the SAJ 110 „A" and „B" versions respectively.

2.1. Functional Description of an SAJ110 Divider Stage

Each stage used in the SAJ 110 comprises basically a trigger network, two transistors connected as a flipflop, and an output stage (Fig. 3). The input is first applied to a trigger network which always steers the input pulse to that transistor which is cut off at the time. Fig. 3 shows the input and output waveforms produced by one such stage. Each positive edge of the input waveform causes the flipflop to change state so that frequency division by two results. The flipflop output is fed to a transistor connected as an emitter follower output stage, this being provided to isolate the flipflop from an external load and to supply output pulses of constant amplitude. The output pin is connected to the emitter of this transistor.

2.2. Performance Requirement Summary for the Integrated Frequency Divider SAJ110

The integrated frequency divider had to meet the following customer requirements:

Supply voltage	7 - 11 V
Input (trigger waveforms)	Sinusoid or square wave
Output voltage	Not less than 6 V – high enough to permit reliable triggering of another divider stage under all operating conditions
Permissible load range	2 to 100 kΩ
Ambient operating temperature range	0 to 60°C
Number of stages to be accommodated in one package	7
Packaging	14-pin DIP or QIL plastic package

*Application notes will be found in the last pages of this section.

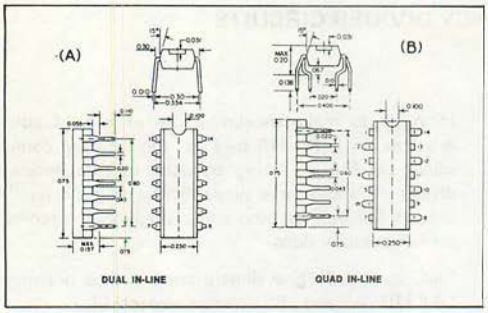


Fig. 2: SAJ 110 Dimensional outline drawings
a) Version "A", TO-116 dual in-line plastic package
b) Version "B", quad in-line plastic package

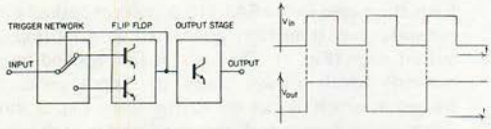


Fig. 3: Block diagram of one divider stage with input and output waveforms

For reason of economy and reliability, it was also considered desirable that the number of integrated elements and the total resistance of all the resistors used in the IC should be kept to a minimum.

2.3. Summary of the Most Important SAJ 110 Data

Maximum ratings

Supply voltage	V_7	11 V
Input voltage	V_{in}	see fig. 4
Output current per stage	I_{out}	5 mA
External output biasing	V_{ext}	$\pm$ 5 V
Ambient temperature range	T_{amb}	− 0 to +60°C
Storage temperature range	T_{stor}	−30 to +125°C

Single stage characteristics
(@ V_7 = 9 V, R_L = 2.2 kΩ, T_A = 25°C)

Current consumption (output in "low" state)	I	< 3 mA
Input voltage ("high" state)	V_{in}	6 . . . 9 V
Input voltage ("low" state)	V_{in}	< 3 V
Output voltage ("low" state)	V_{out}	< 1.0 V
Output voltage ("high" state)	V_{out}	> 7.0 V
Rise time of output pulse	t_r	< 1.0 µs
Input resistance (see fig. 5)	R_{in}	6 to 9 kΩ
Output resistance ("low" state)	r_{out}	≥ 1 MΩ
Output resistance ("high" state)	r_{out}	< 100 Ω

Recommended Operating Conditions

Supply voltage	V_7	9 V $\pm$ 20%
Maximum input frequency	f_{max}	100 kHz
Output load resistor	R_L	2 to 20 kΩ

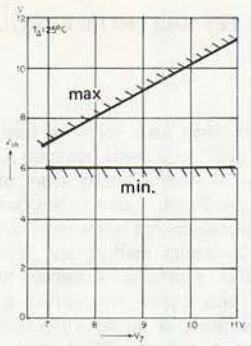


Fig. 4: Maximum permissible input pulse amplitude ("high" state) as a function of supply voltage

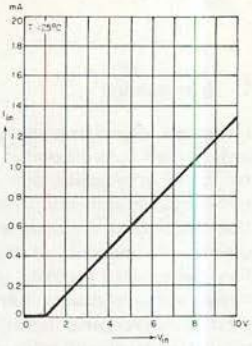


Fig. 5: Input characteristic of a divider stage

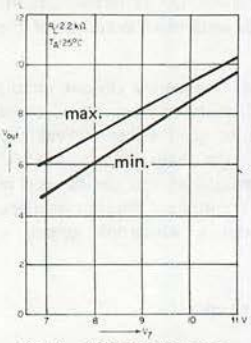


Fig. 6: Output voltage as a function of supply voltage

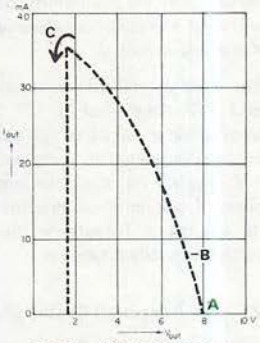


Fig. 7: Output current vs output voltage (pulsed)

The curves shown in Figs. 4 to 7 illustrate the performance of the divider in more detail.

The input parameters of a frequency divider stage at various supply voltages can be deduced from Figs. 4 and 5. The input pulse amplitude should be not less than 6 V, but should, on the other hand, not exceed the supply voltage. The curves in Fig. 4 give the maximum permissible input pulse amplitude range as a function of supply voltage. The input corresponding to "low" level should be less than 1 V. Fig. 5 may be used to determine the static input resistance, which varies between 6 and 9 kΩ.

In the curve shown in Fig. 6 the output voltage is plotted as a function of supply voltage. As can be seen, the output voltage is 1 to 1.5 V lower than the supply voltage and varies somewhat with the load. Assuming the same loading conditions the output voltages of all individual stages are within ±5% − this applies to stages on the same IC as well as to stages on different IC's.

Fig. 7 shows the loading characteristic of a divider stage which gives a "high" output. Note that as the output current of the stage is increased (by reducing the load resistor, for example), point "B" on the curve moves towards "C" (I_{out} = 35 mA and V_{out} = 1.7 V) at which point the stage flips into the "low" state and remains there.

This bistable output effect is discussed further on in connection with the resetting of dividers used in counting circuits.

3. Applications for the SAJ 110

3.1 Use in Electronic Organs

The heart of modern electronic organs is usually a set of LC master oscillators tuned to the frequencies of the highest octave. The frequencies of the lower octaves are then derived from these master oscillators by frequency division. In most conventional organs this frequency division is accomplished by the use of bistable multivibrators (flip-flops). These have the disadvantage of producing a square wave output, which contains practically no even harmonics and offers only limited scope for modifying the character of the notes produced.

However, if the SAJ 110 is used, simple RC networks can be connected across the outputs to generate sawtooth waveforms which contain even harmonics. An additional advantage of the SAJ 110 is its small size, making it particularly suitable for use in portable instruments.

Fig. 8 shows the usual frequency generating circuits employed in electronic organs. Twelve master oscillators produce the frequencies of the highest octave while all the frequencies for the lower octaves are generated by frequency division. The arrangement shown in Fig. 8 requires up to twelve SAJ 110 circuits for one organ. If the organ has less than seven octaves, then there are several spare divider stages which may be utilized in the divider chains associated with other frequencies so that in this case less than 12 integrated circuits are required.

Depression of one of the organ keys, T, causes several outputs to be switched to a common line, S, via high value resistors, R, and this signal, which is a combination of several frequencies, is then further processed. The spectrum of this signal is considerably richer in harmonics than that of an ordinary square wave.

It is an advantage to give a signal to the following filters the mean value of which does little change when the organ keys are pressed. In order to obtain this, the ground of resistor R/10 (Fig. 8) should be connected to a positive potential. Another possibility is to ensure that the divider outputs supply proper AC signals. Fig. 9 shows such an alternative circuit. Use of a suitable bias causes the full alternating divider output component to be developed across the load R_L.

The circuit shown in Fig. 10 fully exploits the high output voltage and low output resistance of the frequency divider SAJ 110. In this circuit RC networks are connected, via protection diodes, to the outputs of individual divider stages so that waveforms which are not very different from that of an ideal sawtooth are presented across the load R_L. The protective resistor R_S connected in series with each capacitor C_L is included to limit the capacitor surge to a value which the output stage can safely handle.

In Fig. 11 the frequency spectrum of the waveform V_{RL} is compared with that of two sawtooth waveforms, and it can be seen that the spectrum attained with the circuit arrangement of Fig. 10 approaches that of an ideal

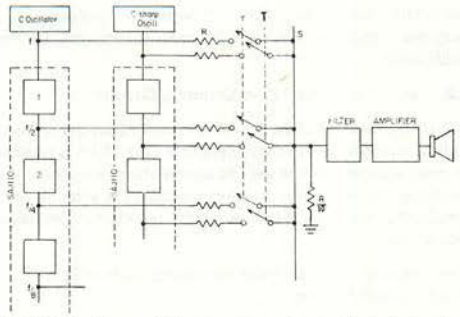


Fig. 8: Block diagram of the tone generating circuits in electronic organs

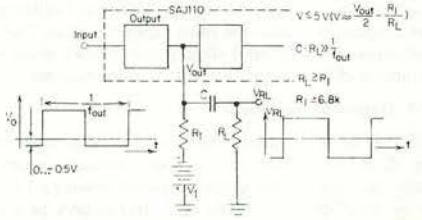


Fig. 9: Conversion of divider unidirectional output into alternating output

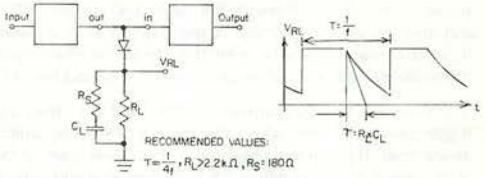


Fig. 10: Modification of the divider frequency spectrum using RC networks

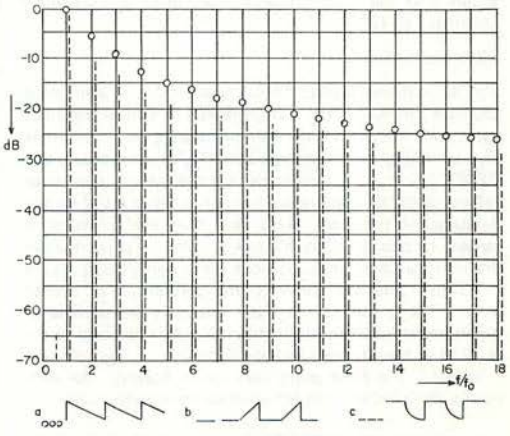


Fig. 11: Frequency spectrum associated with various waveforms

sawtooth. Note that the sub-harmonic component is extremely small – much smaller than is necessary for this application.

3.2. Use of the SAJ 110 in Counting Circuits

Use of the SAJ 110 in a counting circuit raises the problem of how to reset the flipflops. With the SAJ 110 it is possible to reset a single stage as well as several stages connected in a counting chain. However, when designing a suitable reset circuit the following features of the device must be taken into account:

The output of a divider stage can change state only while its input is positive going.

The frequency divider SAJ 110, unlike a master slave flipflop, does not possess a buffer stage between input and output, nor a special reset input.

It is, however, possible to use the inputs and outputs for reset purpose. Because the reset capability of an SAJ 110 stage depends on its input state, it is necessary to use both the input and the output terminals for reset purpose.

3.2.1. Output Characteristic

Referring to the output characteristic of a single stage (Fig. 7) it can be seen that a "high" output can only be flipped to "low" if the output is pulled down to 1.5 V or less by some external means, and this can only be accomplished while the input voltage V_{in} is "low". The output characteristic in Fig. 7 is divided into the sections A-B and B-C, section A-B being the normal operating range. As mentioned previously, in order to initiate a reset it is necessary to force the output through the range B-C to point "C", and this should be effected in the shortest time possible ($t_r < 0.1$ msec) to avoid overheating the device (the output transistor dissipates considerable power during this period).

If the divider input potential is higher than 0 V, then the trigger point C is shifted to the left on the curve, which means that the output potential would then have to be pulled down to a level below 1.5 V. If the input and output of a divider stage or if several inputs and outputs of a divider chain are to be pulled down to a low potential together, then this potential should be less than 1.5 V to ensure that the circuits reset reliably under any condition (refer to Fig. 12).

3.2.2. Reset Circuit

Fig. 12 outlines a reset circuit suitable for a seven stage counting chain. All the output points as well as the input point I are connected, via isolating diodes, to the collector of a switching transistor type 2N2218, or alternatively to a RESET switch. It is important that the transistor collector voltage drops to a saturation level of less than 0.6 V for the duration of the reset pulse, and that the transistor is capable of passing up to 400 mA of collector current under the most unfavorable conditions (i.e. when all outputs are in "high" condition prior to the application of a reset pulse). The pulse source must therefore be capable of supplying at lease approximately 15 mA to the base of the 2N2218 so that the requirement $V_{I_1} = V_{O_1} = \ldots V_{O7} < 1.5$ V is fulfilled. The reset pulse duration is, however, not very critical provided it is not less than approximately 1 μ sec.

As mentioned previously, the output state of all the stages depends on the input state of the first stage immediately after the occurrence of the reset pulse. There are two possible conditions:

V_{I_1} = "low" (Fig. 13)
V_{I_1} = "high" (Fig. 14)

In Fig. 13 I_1 was "low" at the instant when the reset was applied; under this condition all the outputs which were in the "high" state immediately before application of the reset pulse change to "low" and maintain this state after the reset pulse has been removed. The next input pulse to I_1 then causes all the outputs to be triggered to "high", this corresponding to a "PRESET" condition of the counter. Only the second input pulse is counted. These conditions are summarized in the truth table in Fig. 13 and it can be seen that the counter counts (n-1).

Fig. 14, on the other hand, illustrates a condition in which all the outputs are in the "PRESET" state immediately after the occurrence of the reset pulse so that the next pulse is correctly counted as No. 1. The explanation for this is as follows: Although in this case the reset pulse initially pulls all the outputs, as well as the input I_1, to "low", the input I_1 is immediately returned to "high" at the end of the pulse ($t = t_1$), because the positive edge at the end of the pulse is equivalent to the application of a logic "H" to the input. This positive edge triggers first output O_1 and then, in turn, all the other outputs to "high" – this corresponding to the "PRESET" state of the counter.

4. Conclusion

The SAJ 110 is an inexpensive seven-stage frequency divider which, in comparison with equivalent discrete-component circuits, offers many advantages, the most important ones being: small size and low wiring and assembly cost. The device, because of its electrical characteristics, is particularly suitable for use in electronic organs where its performance is superior to that of discrete component flipflops. Being insensitive to the waveform of the input signal, the SAJ 110 will accept a square wave as well as other types of waveforms (e.g. sinusoids); moreover, the low output impedance ensures that the output remains virtually constant irrespective of load, the lowest permissible load being approximately 2 kΩ. At maximum loading the output amplitude is only 1.5 V less than supply voltage.

The generation of output waveforms which are very similar to, and possess virtually the same frequency spectrum as, that of an ideal sawtooth, is possible simply by connection of RC networks across the outputs.

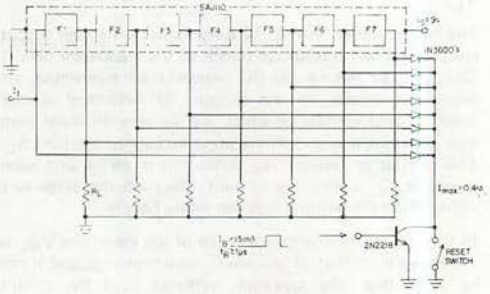


Fig. 12: Reset circuit for a seven stage counter

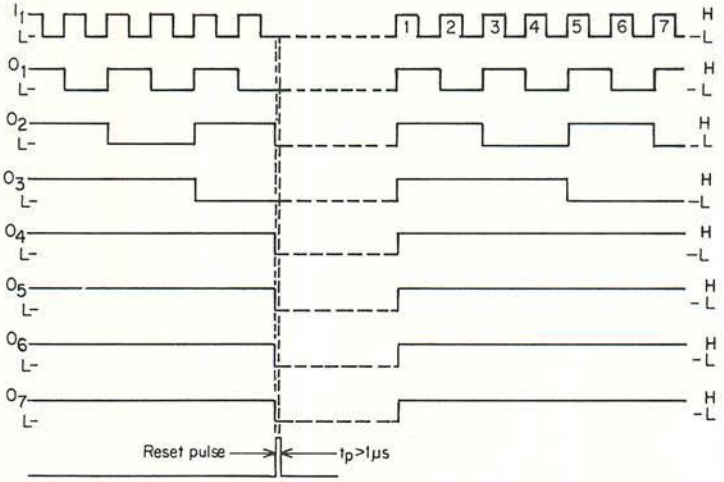


Fig. 13: Reset action at V_{I_1} = "low"

TRUTH TABLE

I_1	O_1	O_2	O_3	O_4	O_5	O_6	O_7
0	L	L	L	L	L	L	L
1	H	H	H	H	H	H	H
2	L	H	H	H	H	H	H
3	H	L	H	H	H	H	H
4	L	L	H	H	H	H	H
5	H	H	L	H	H	H	H
6	L	H	L	H	H	H	H
7	H	L	L	H	H	H	H

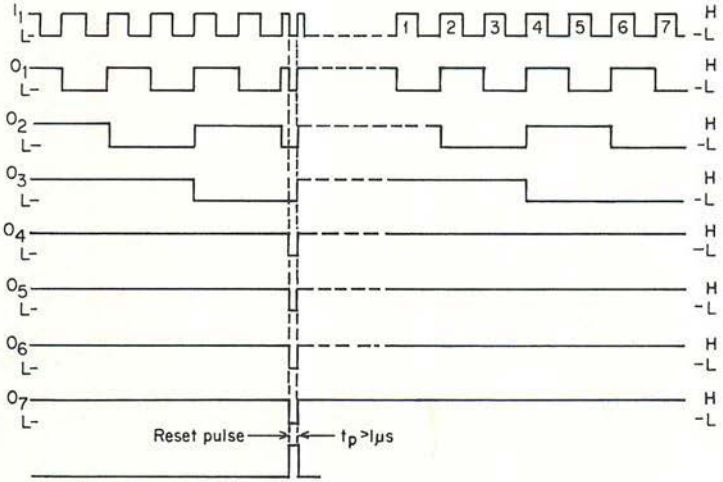


Fig. 14: Reset action at V_{I_1} = "high"

TRUTH TABLE

I_1	O_1	O_2	O_3	O_4	O_5	O_6	O_7
0	H	H	H	H	H	H	H
1	L	H	H	H	H	H	H
2	H	L	H	H	H	H	H
3	L	L	H	H	H	H	H
4	H	H	L	H	H	H	H
5	L	H	L	H	H	H	H
6	H	L	L	H	H	H	H
7	L	L	L	H	H	H	H

ITT'S New Unabridged DTL Design Data Book

ITT DTL 930 SERIES

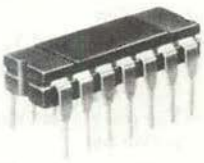
The ITT DTL 930 Series is a family of compatible integrated circuits using diode-transistor logic. The advantages of this family are:

- Choice of dual in-line, ¼" × ¼" flat pack, or TO-5 packages.
- Choice of full (−55° to +125°C) or limited (0 to +75°C) temperature ranges.
- Operation from a single power supply, and over a wide voltage range.
- Low power dissipation
- High worst-case noise immunity
- High fan-out capability
- Fan-out/noise immunity trade-off ability
- Specified operation over full temperature range
- Wide and proven application
- Gate outputs can be "wired OR"

FLAT PACK

SIMILAR TO TO-5

DUAL IN-LINE



Contents

GLOSSARY

GLOSSARY OF TERMS USED WITH DTL 930 SERIES

In General, Subscripts are used as follows:

O = output
I = input
R = reverse, applying to high inputs.
F = forward, applying to low inputs.
L = low, applying to a low signal level or when with V_{CC} to low V_{CC} value.
H = high, applying to a high-signal level or when used with V_{CC} to high V_{CC} value.

Non-operational Terms:

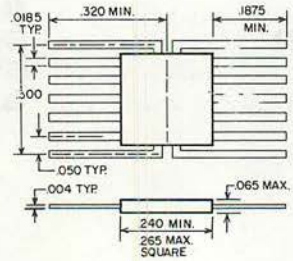
$V_{(MAX)}$ = Maximum rated V_{CC} pin voltage.
$I_{(MAX)}$ = Maximum rated current into V_{CC} pin, with $V_{(MAX)}$ applied.
V_{PD} = V_{CC} pin voltage applied during power dissipation test.
I_{PD} = Current into V_{CC} pin with V_{PD} applied. I_{PDL} means gate or buffer inputs are low or clock pin input is low. I_{PDH} means the inputs are high.
V_R = Input reverse (high) voltage for input diode leakage test.
I_R = Reverse input diode current with V_R applied to input.
I_{RCP} = Reverse clock pin input leakage current with V_R applied to input.
V_{CEX} = Output transistor collector to emitter voltage. With output pull-up resistor connected, $V_{CEX} = V_{CC}$ to avoid drop across output pull-up resistor.

Operational Terms:

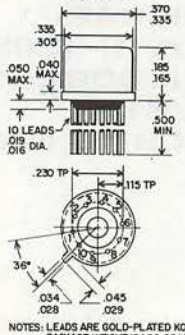
V_{IL} = Input low (threshold) voltage.
V_{OL} = Output low voltage, with rated fanout current I_{OL} into output.
LV_{CE} = Collector emitter latching voltage.
V_B = Breakdown voltage of capacitor input.
I_{CEX} = Output transistor collector to emitter leakage current with V_{CEX} applied to output.
V_{FD} = Forward diode drop in 933 Element.
I_{FD} = Forward diode current in 933 Element.
V_{IH} = Input high (threshold) voltage.
V_{OH} = Output high voltage, with high current (I_{OH}) flowing out of output.
V_F = Forward (low) input voltage, for forward input current (I_F) test. V_F is usually ground.
I_F = Forward input diode current, for unit input load. Also shown will be 2/3 I_F, I_{FCP}, and I_{FS}.
I_{OL} = Output low current.
I_{OH} = Output high current, flowing out of output in V_{OH} test.
I_{SC} = Short circuit output current to ground, with one or more inputs low. I_{SC} minimum confirms output ability to pull up capacitive loads; I_{SC} maximum confirms subtraction of fanout rules when "OR"ing outputs.
V_{CC} = Supply voltage.
V_{CCL} = Low V_{CC} pin voltage. Used for V_{OL} (I_{OL}) and V_{OH} (I_{OH}) tests.
V_{CCH} = High V_{CC} pin voltage. Used for V_F — I_F input forward diode current tests.
$CP_{,X}$ = Clock Pin, pulsed. The subscript if any refers to pulse waveshape. Used in testing binary elements.
V_{CPTH} = Input Clock Pin threshold voltage (low). With Clock Pin at or below V_{CPTH}, the "master" Flip-Flop holds the proper "slave" (output) Flip-Flop output high.
V_X = Input low (threshold) voltage extendable inputs.
I_{RK} = Monitoring current through resistance.

PACKAGES

FLAT PACK
TO-86

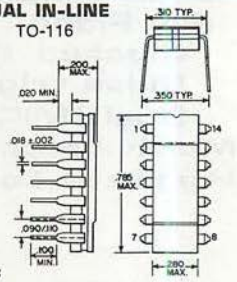


SIMILAR TO TO-5
TO-100



NOTES: LEADS ARE GOLD-PLATED KOVAR
PACKAGE WEIGHT IS 1.32 GRAMS

DUAL IN-LINE
TO-116

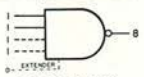


NOTES:

1. Leads are a modified hexagon in cross section. Board-drilling dimensions should equal your practice for a conventional .020 inch diameter lead.
2. Max. envelope for all planned packages of this design family.

INPUT-OUTPUT LOADING FACTORS

The number of elements that may be driven by an output terminal may consist of any combination of elements whose summation of input loading does not exceed the output terminal driving capability. Fanout for 0°C to +75°C range is given in parenthesis.



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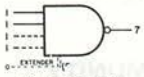
¼ 946.
⅓ 962
⅛ 936



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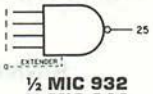

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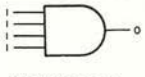

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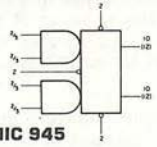

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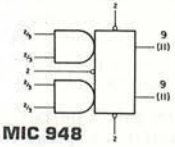
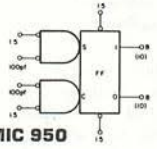
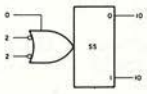


MIC 948



MIC 950



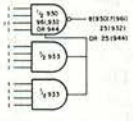
MIC 951

LOADING RULES

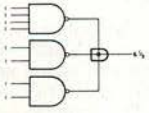
1. Extension of inputs with the MIC 933 does not affect quiescent loading of the supplemented element (MIC 930 or 932). However, capacitance due to wiring to the MIC 933 will affect noise tolerance and propagation delay, and thus establish a fan-in limit for the particular application. Please refer to the typical curves on the MIC 933 Dual Extender Element specifications.
2. For operation with a nominal supply voltage of 4.0 volts from −55°C to +125°C, reduce element fanout as follows: MIC 930=5, MIC 945=7, MIC 932=18. If temperature is maintained above −20°C, no fan-out reduction is necessary.
3. For operation with a nominal supply voltage of 6.0 volts from −55°C to +125°C, reduce element fan-out as follows: MIC 930=6, MIC 945=8, MIC 932=20. If ambient temperature remains below +100°C or if worst case noise threshold is considered to be 250 mV, no fan-out reduction is necessary. Except as noted, these rules apply over the entire military temperature range with a supply voltage of 4.5 to 5.5 volts. These rules also permit a 50°C temperature differential between individual elements. These rules guarantee a worst case signal-line or ground noise threshold of at least 350 mV. Practical noise thresholds exceed 500 mV.
4. All rules for MIC 930 apply to MIC 946, 962, and 936. All rules for MIC 961 apply to MIC 949, 963, and 937. **All rules for MIC 945 apply to MIC 9093 and 9099. All rules for MIC 948 apply to MIC 9094 and 9097.**
5. For increased current, inputs and outputs of ½ MIC 932 or ½ MIC 944 may be simultaneously paralleled up to 4 common outputs. Each combined input=4 loads. Combined output=100 loads.
6. An external resistor should be used with MIC 944. With external R to 5 volt V_{CC} ±0.5 V; subtract output loads as follows: R=2KΩ, subtract 2 loads, R=1KΩ, subtract 4 loads, R=510Ω, subtract 8 loads.

INPUT EXTENSION AND "wired OR" LOADING

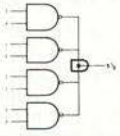
EXTENSION OF INPUTS



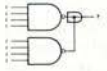
GATES WHEN "wired OR"



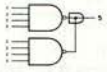
½ 930 and
2 x ¼ 946



4 x ¼ MIC 946



MIC 930 "wired OR"
ALSO 946, 962



MIC 961 "wired OR"
ALSO 949, 963

RULES FOR "wired OR"

1. Outputs of DTL gates with 6KΩ pull-up resistors, 930,946,962 and 936 may be tied together for the "wired OR" function. Subtract 1 unit of fan-out for each added gate. Subtract 5 fan-outs for 6 added gates.
2. Outputs of DTL gates with 2KΩ pull-up resistors, 949,961,963 and 937 may be tied together for the "wired OR" function. Subtract 2 units of fan-out for each added gate.
3. Outputs of MIC 932 may not be tied together for the "wired OR" function, however MIC 944 outputs may be used in the "wired OR" configuration.

NOISE IMMUNITY

There are two important types of noise immunity that must be considered when designing with ITT DTL 930 Series circuits. Both types are discussed below.

SIGNAL NOISE IMMUNITY

Signal Noise Immunity, V_{NS}, is defined by the equations

$$V_{NS} = |V_{IL}(\max) - V_{OL}(\max)|$$

or

$$V_{NS} = |V_{OH}(\min) - V_{IH}(\min)|$$

Where

$V_{OH}(\min)$ = Minimum high output voltage
$V_{IH}(\min)$ = Minimum high input voltage that will guarantee $V_{OL}(\max)$ at the output
$V_{IL}(\max)$ = Maximum low input voltage that will guarantee $V_{OH}(\min)$ at the output
$V_{OL}(\max)$ = Maximum low output voltage

The meaning of these equations is indicated in Fig. 1 and 2. The pulse shown at A in Fig. 2 is a noise signal induced on the signal line connecting two gates. The pulse at A is not sufficient to make the input voltage rise from V_{OL} (max) to $V_{IL}(\max)$ and, therefore the output of gate 2 will remain unchanged. However, the pulse at B will cause the input level to rise above $V_{IL}(\max)$ and, consequently, gate 2 may turn on, and its output voltage falls undesirably.

When gate 1 output is high, the output voltage is guaranteed to be greater or equal to $V_{OH}(\min)$ under the specified worst case conditions. The noise signal at C will not make the signal level fall below $V_{IH}(\min)$. Gate 2 will therefore maintain a low output level. However, the pulse at D may cause gate 2 to turn off, and its output voltage rises undesirably.

FIG. 1

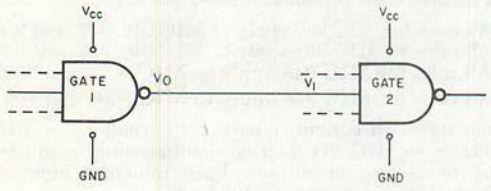
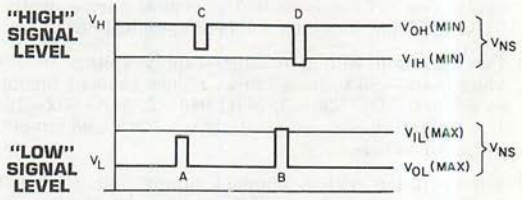


FIG. 2



GROUND NOISE IMMUNITY

Ground Noise immunity, V_{NG}, is usually the worst case noise immunity for DTL 930 Series circuits.

Notice that some curves show two values of V_{CC} at a given temperature for the same noise immunity. The upper V_{CC} ensures that the driving device is hard in saturation. Ground noise signals will therefore only add to output level $V_{OL}(\max)$. The noise immunity for this case will be defined by

$$V_{NG} = V_{NS} \simeq |V_{IL}(\max) - V_{OL}(\max)|$$

When the drive gate is hard in saturation due to high V_{CC}, ground noise signals will probably exceed the immunity defined by this equation before they reach a level tending to turn off the drive gate. As the V_{CC} is reduced, the load current in the output transistor will decline with a corresponding decrease in V_{OL}. The gate is still hard in saturation and we obtain a gain in noise immunity. However, as V_{CC} is lowered further, the gate reaches a region of soft saturation and the ground noise signal may turn off the drive gate. The gate amplifies the ground noise signal and the noise immunity is significantly less than $|V_{IL}(\max) - V_{OL}(\max)|$. Each of the curves shows V_N, the worst case of V_{NG} and V_{NS}.

As an example, the curves for a fan-out of 7 show a worst case $V_N = V_{NG}$ of 200 mV at $V_{CC} = 4V$ and $-55°F$. This, however, corresponds to a worst case signal noise immunity of $|V_{IL}(\max) - V_{OL}(\max)| \geqq 500$ mV for the same fan-out temperature and V_{CC}. This happens because V_{NS} only adds to $V_{OL}(\max)$ but V_{NG} deprives the output transistor of the drive gate of base current, thus turning it off.

FIG. 3

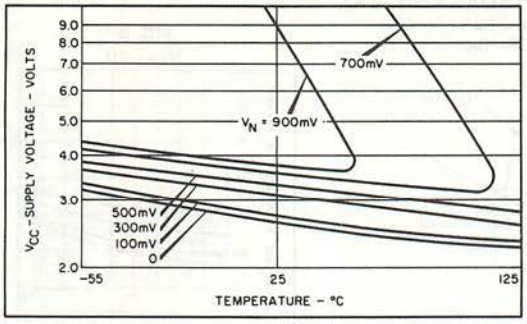


FIG. 4

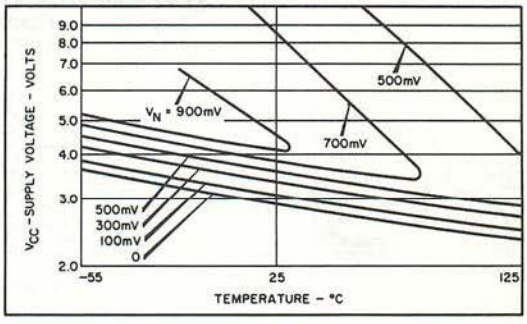


FIG. 5

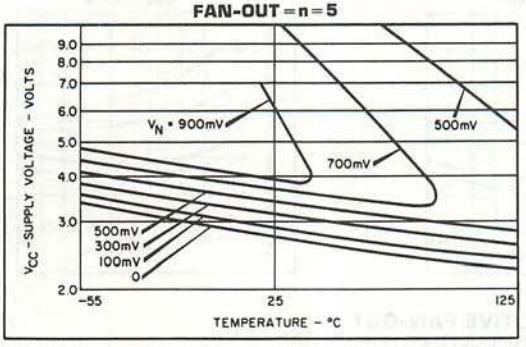
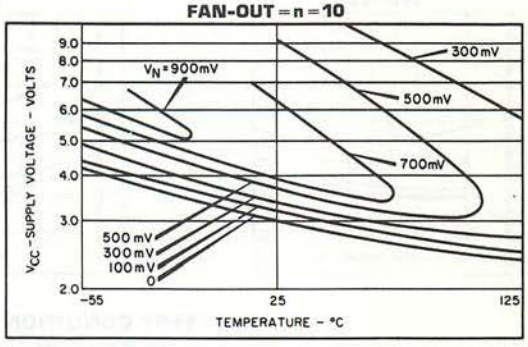
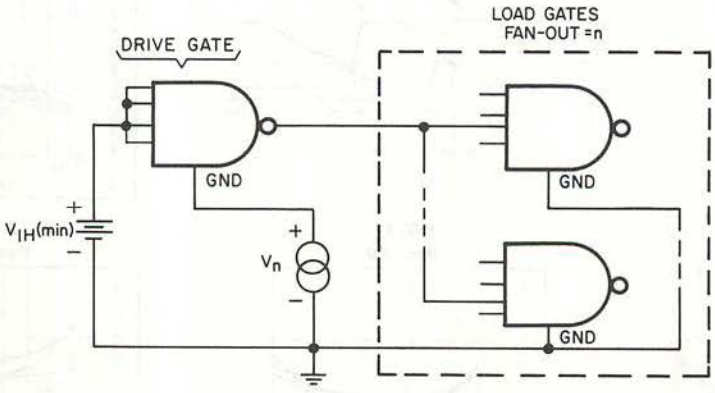


FIG. 6



TEST CONDITIONS FOR FIGURES 3, 4, 5, 6



PROPAGATION DELAY

AVERAGE tpd VS. TEMPERATURE

TEST CONDITION A, INACTIVE FAN-OUT

FAN-OUT = n, 5pf CAPACITANCE PER FAN-OUT
PULL UP RESISTOR = 6KΩ

FIG. 7

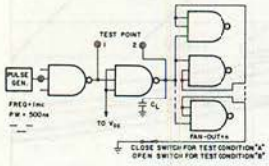
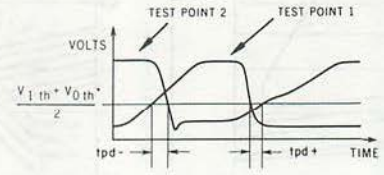


FIG. 8



$$AV\ tpd = \frac{tpd- + tpd+}{2}$$

FIG. 9
Vcc = 6V

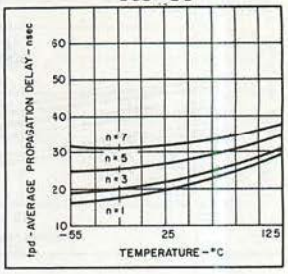


FIG. 10
Vcc = 5V

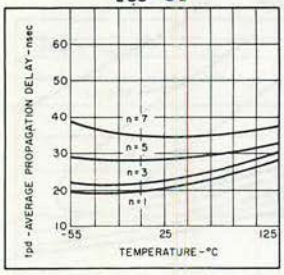


FIG. 11
Vcc = 4V

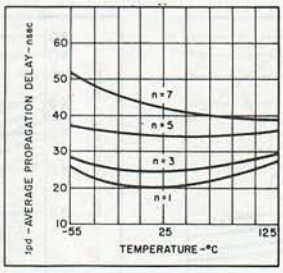
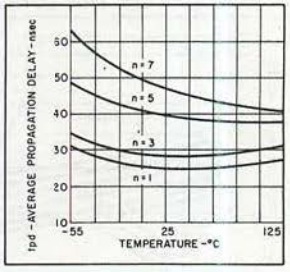


FIG. 12
Vcc = 3.6V



TEST CONDITION B, ACTIVE FAN-OUT

FAN-OUT = n, 5pf CAPACITANCE PER FAN-OUT
PULL UP RESISTOR = 6KΩ

FIG. 13

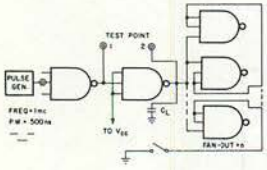
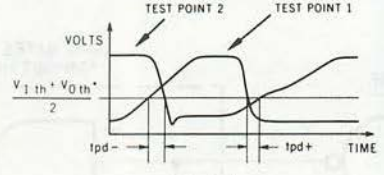


FIG. 14



$$AV\ tpd = \frac{tpd- + tpd+}{2}$$

FIG. 15
Vcc = 6V

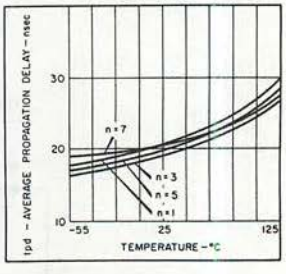


FIG. 16
Vcc = 5V

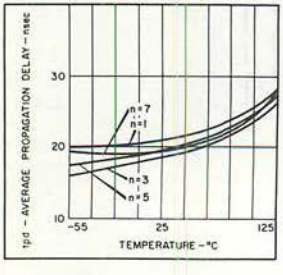


FIG. 17
Vcc = 4V

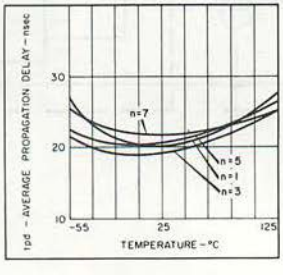
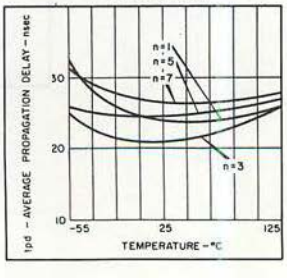


FIG. 18
Vcc = 3.6V



TIME DELAY VERSUS CAPACITIVE LOADS

(THRESHOLD ≈ +1.5 V. T = 25°C, Vcc = +5.0 V)

FIG. 19
2K PULL-UP RESISTOR

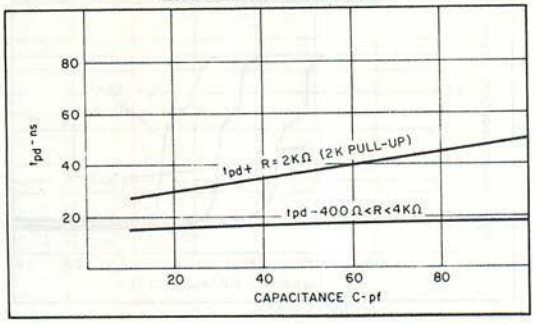


FIG. 20
6K PULL-UP RESISTOR

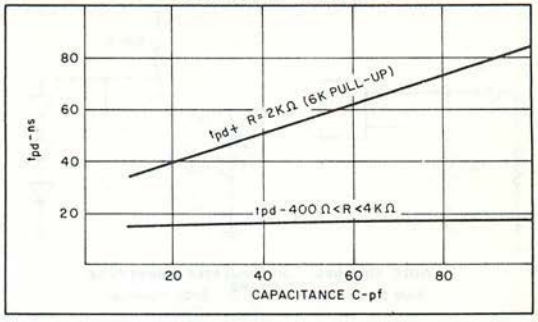
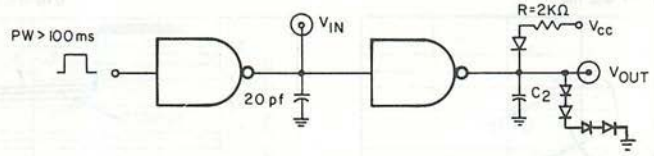


FIG. 21



ADDITIONAL DELAY TIME CHARACTERIZATION INTO CAPACITIVE LOADS

The curves on page 10 give extensive delay characterizations as functions of V_{CC}, temperature, fan-out and ratio of active to inactive fan-out. For each fan-out, active or inactive, 5pf wiring capacity was added. This page will show the effects of greater wiring capacities.

Most delay attributable to capacitive loads is associated with the positive going output. Two R-C time constants are seen in the positive going output, as shown in the pictures below. In the 1st time period, from the saturated low level to threshold, the R of the R-C time constant can be given by 6KΩ in parallel with $\frac{3.75K\Omega}{\text{active fan-out}}$.

Above the threshold which occurs at about 1.4 to 1.5 volts at 25°C, the R of the 2nd R-C time constant is 6KΩ and the rate of the voltage rise above threshold is slow. The logic signal propagates through at the threshold level; so voltage rise above threshold does not affect speed. By noting that both rise domains drive toward V_{CC}, the voltage rise waveform may be calculated. MIC 930, 932, 933, 936, 937, 946, 949, 961, 962, 963 are ~ 2pf per input for active or inactive fan-out; the remaining capacitance is from board, wiring, and connectors. Gates with 2KΩ pull resistors should be treated similarly.

The t_{pd} average curves, with one active fan-out, Fig. 23 below, gives the prediction of capacitive effects on switching speeds. In Fig. 22 below each output has 1 active fan-out, which is worst case.

FIG. 22

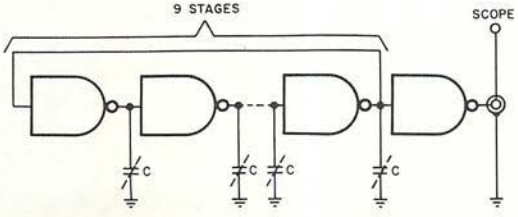
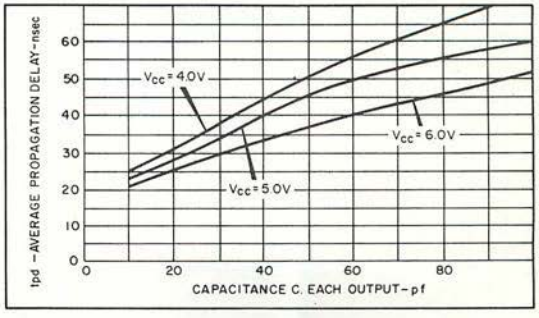


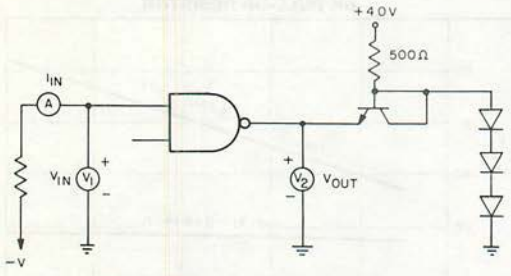
FIG. 23
tpd AVERAGE VS. CAPACITY
MIC 930, 946, 962. (+25°C)



TRANSFER CHARACTERISTICS

TYPICAL CHARACTERISTICS, FAN-OUT = 7, V_{CC} = 4V

FIG. 24



NOTE: 500Ω RESISTOR SIMULATES WORST CASE.
FAN-OUT = 7 SINCE $\frac{R1+R2}{7}$ = 500Ω NOMINAL.

FIG. 25
V_{OUT} VS V_{IN}

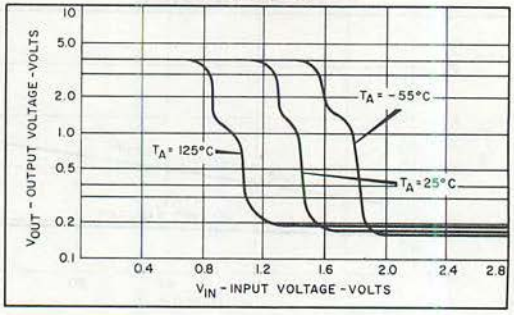


FIG. 26
V_{OUT} VS I_{IN}

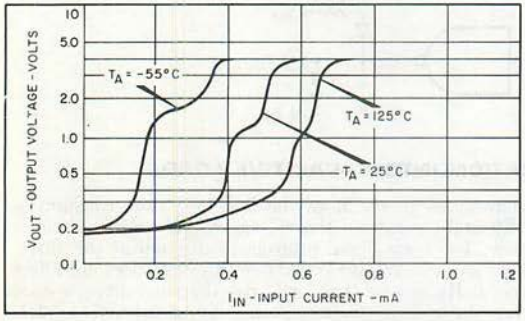
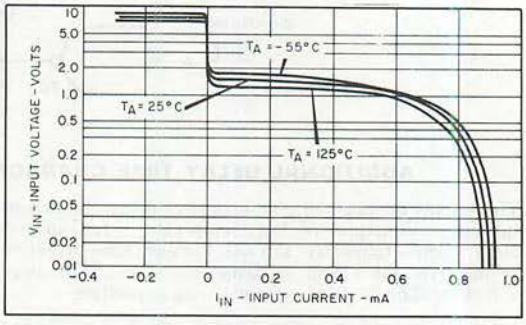


FIG. 27
V_{IN} VS I_{IN}



TRANSFER CHARACTERISTICS

TYPICAL CHARACTERISTICS, FAN-OUT = 0, V_{CC} = 4V

FIG. 28

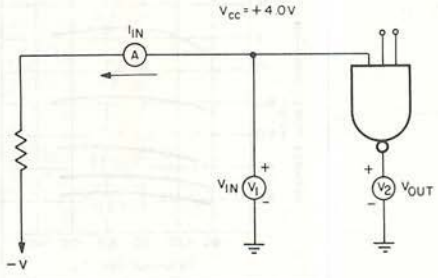


FIG. 29
VOUT VS. VIN

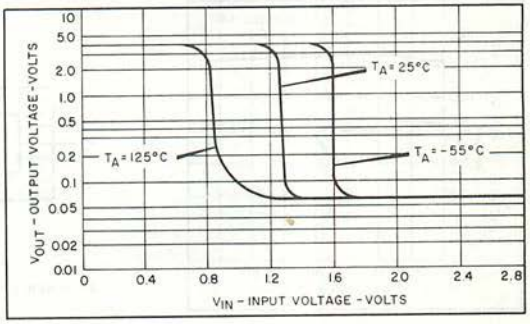


FIG. 30
VOUT VS. IIN

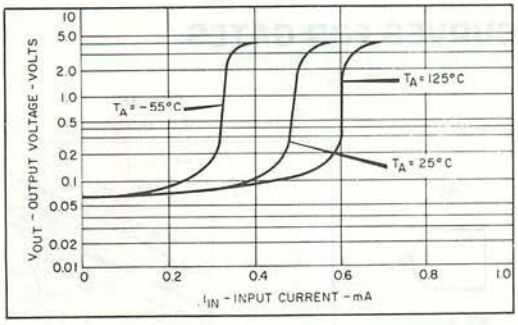
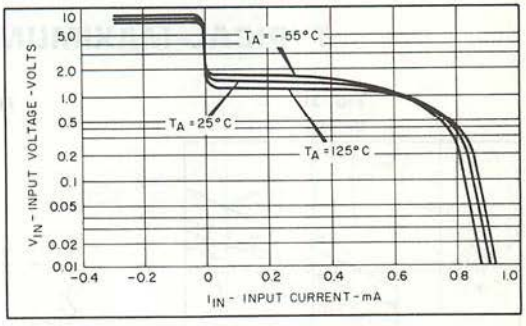


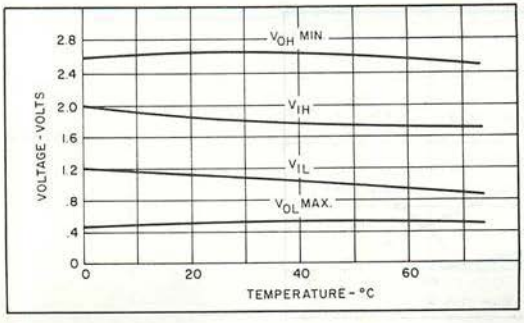
FIG. 31
VIN VS. IIN



OPERATING VOLTAGE PARAMETERS

VOH, VIH, VIL, VOL VS TEMPERATURE, Vcc = 5V

FIG. 32



DC CURVES

AVERAGE POWER DISSIPATION VS. TEMPERATURE FOR GATES

FIG. 33
$V_{CC} = 5V$

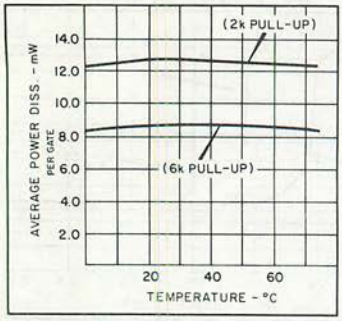
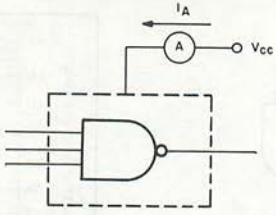
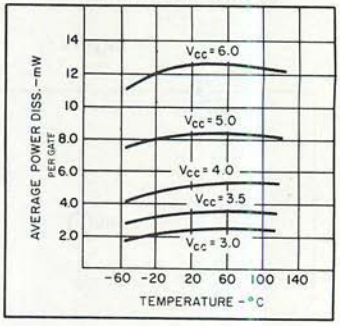


FIG. 34
TEST CIRCUIT



AV. POWER DISS. = $\frac{V_{CC} \; I_A}{2}$

FIG. 35
2K PULL-UP RESISTOR



NOTES: 1. Fig. 33, 6K pull-up curve for MIC 930, 936, 946, 962; 2K pull-up for MIC 937, 949, 961, 963.
2. Fig. 35 applies to MIC 937, 949, 961, 963 only.

TYPICAL-MAXIMUM I_F CURVES FOR GATES

FIG. 36
$V_F = 0V$

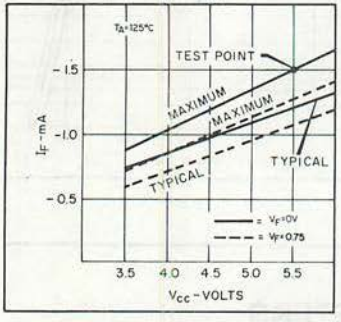


FIG. 37

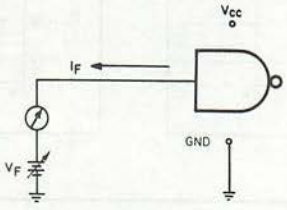
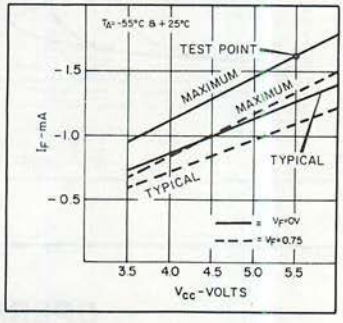


FIG. 38
$V_F = 0.75V$



OUTPUT CURRENT VS. OUTPUT VOLTAGE FOR 930, 936, 946, 962.

FIG. 39

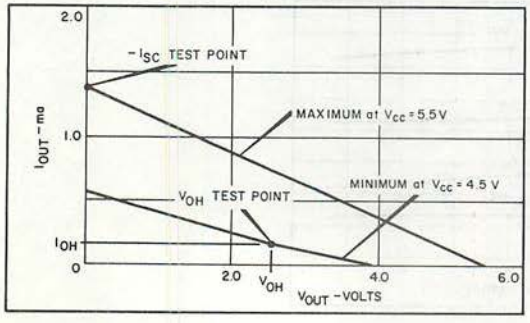
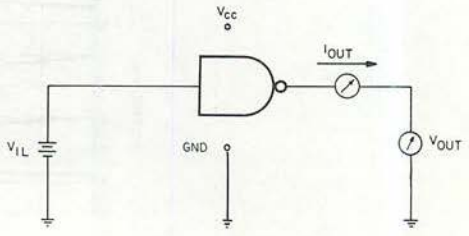


FIG. 40



OUTPUT LOW CURRENT VS. V_{CC} OR V_{OL} FOR MIC 930, 936, 946, 962.

FIG. 41

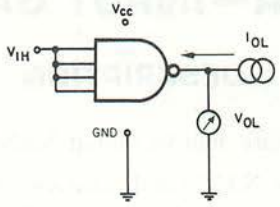


FIG. 42
I_{OL} VS. Vcc

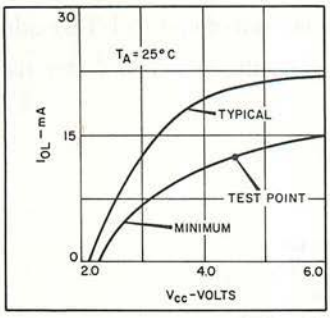


FIG. 43
I_{OL} VS. Vcc

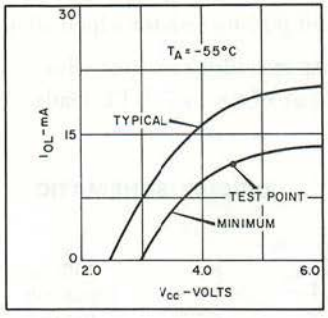
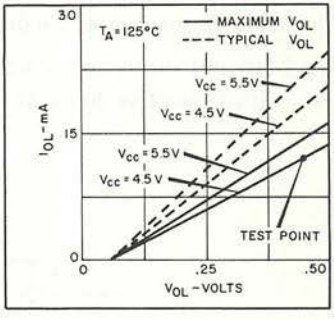


FIG. 44
I_{OL} VS. V_{OL} VS. Vcc

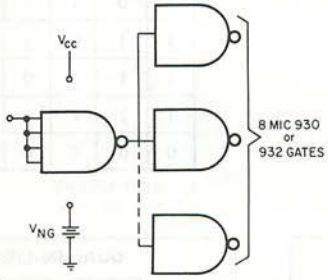


EXAMPLES OF USES FOR THE MINIMUM-MAXIMUM DC CURVES

EXAMPLE 1.

A low MIC 930 output at −55°C fans out to 8 inputs of MIC 930 or 932. V_{CC} = 5V. Positive DC ground noise (V_{NG}) of 350 mV is applied to the 1st 930. Its output may thus rise to .75 Volt ($V_{NG}+V_{OL}$). 4.65 Volts ($V_{CC}-V_{NG}$) remain from V_{CC} pin to ground pin; this is above V_{CCL} = 4.50 V, and test I_{OL} is conservative. Maximum current flowing out of each input of the 8 930/932's is given by Fig. 38 on Page 14 with V_F = 0.75V and V_{CC} = 5V; the current (I_F) is less than 1.25 mA and total current ($\leq 8 \times 1.25 = 10$ mA) is less than the I_{OL} test current used at −55°C to saturate the low output. Above the 350 mV of V_{NG} already applied, the difference between the common node voltage ($\leq$.75V) and the low input threshold (V_{IL} = 1.10V) of the 8 930/932's is still = 350 mV, allowing for signal noise to be superposed above ground noise.

FIG. 45



EXAMPLE 2.

The I_F and I_{OL} curves on Pages 12 & 13 may be expressed in analytical form, as follows: I_F (930 and 932) $\leq \frac{V_{CC}-V_F-V_{FD}}{3K\Omega}$ T_A <25°C.

For T_A greater than 25°C, the 3KΩ rises by 0.12%/°C to approximately 3.36KΩ at +125°C. V_{FD} is the temperature dependent silicon forward diode drop and is about 0.70V at 25°C and 1 mA. ΔV_{FD}/°C is roughly 1.8 mV/°C. The ratio of I_{OL}, on 930 (Figs. 41, 42, and 43) at V_{CC} below test V_{CC}, to I_{OL} at test V_{CC} can be given by

$$\frac{I_{OL} @ -55°C}{\text{Test } I_{OL} @ V_{CCL}=4.5V} \geq \frac{V_{CC}-3.0V}{4.5V-3.0V}$$

and by

$$\frac{I_{OL} @ 25°C}{\text{Test } I_{OL} @ V_{CCL}=4.5V} \geq \frac{V_{CC}-2.3V}{4.5V-2.3V}$$

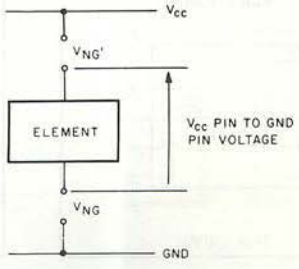
Since, at 25°C, $I_{OL} \geq 12$ mA at V_{CCL} = 4.5V is guaranteed by the device specifications, I_{OL} at V_{CC} pin to GND pin voltage of 3.6V is $\left(\frac{3.6-2.3.}{4.5-2.3.}\right)12$ mA = 7.1 mA.

The similar expression for the 932 gives a very conservative value due to the phase splitter gain. Above V_{CCL}, I_{OL} is limited by V_{OL} with an essentially resistive $\left(\frac{V_{OL}}{I_{OL}} \text{ saturation resistance}\right)$ slope. Fig. 44 at +125°C shows this, with V_{CC} having relatively small effect.

EXAMPLE 3.

The test sequences and tables of conditions and limits, use two values of V_{CC}, V_{CCL} and V_{CCH}. With a nominal 5 volts V_{CC}, for example, and assuming $\Delta V_{CC} = \pm .2V$, testing at V_{CCL} = 4.5V and V_{CCH} = 5.5V allows simulation of a 0.3V ground noise V_{NG} or V_{CC} line noise V_{NG}. Since there is gain associated with V_{NG} (refer to Page 7), particularly at lower temperatures and V_{CC} values; the test guarantees of output low current and voltage are the worst case test conditions to simulate worst case ground noise. Much better numbers could be shown, for example, in the ratio of output current to input current (I_{OL}/I_F) if both I_{OL} and I_F were measured at identical V_{CC} values and if input current was sunk into $V_F = V_{OL}$, the worst case low output level, or even into $V_F = V_{IL}$, the input threshold value. However, the test values would then guarantee only signal line noise immunity, where there is no gain associated with V_{NS}. By use of the Minimum/Maximum DC curves on Pages 12 & 13 or by the Example 2 equations, limits for the single V_{CC} testing approach could be recovered. More important, each design or components engineer can develop the fan-out, power, and noise margin tradeoffs for this unique application.

FIG. 46



DUAL FOUR—INPUT GATE MIC 930
FAST DUAL FOUR—INPUT GATE MIC 961

DESCRIPTION

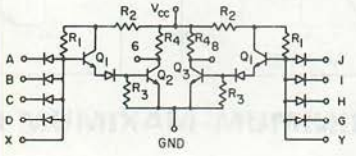
The MIC 930 and MIC 961 elements are dual four-input NAND/NOR gates.

In addition to performing the positive NAND and negative NOR logic functions, the gates can be cross-coupled to form a flip-flop or the outputs can be tied together to perform the "wired OR" function. Both gate inputs may be extended using MIC 933 elements to allow increased fan-in.

The MIC 930 incorporates a 6K output pull-up resistor which allows for a fan-out of up to 8 DTL loads.

The MIC 961 incorporates a 2K output pull-up resistor which typically results in a 30% faster rise time with capacitive loads at a fan-out of up to 7 DTL loads.

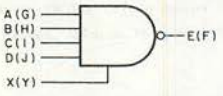
CIRCUIT SCHEMATIC



TYPICAL RESISTOR VALUES

$R_1 = 2.0\ K\Omega$
$R_2 = 1.75\ K\Omega$
$R_3 = 5.0\ K\Omega$
$R_4 = 6.0\ K\Omega$ (930)
$R_4 = 2.0\ K\Omega$ (961)

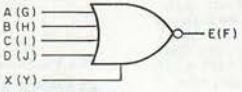
POSITIVE (NAND) LOGIC



$E = \overline{A \cdot B \cdot C \cdot D \cdot (X)}$

$F = \overline{G \cdot H \cdot I \cdot J \cdot (Y)}$

NEGATIVE (NOR) LOGIC



$E = \overline{A + B + C + D + (X)}$

$F = \overline{G + H + I + J + (Y)}$

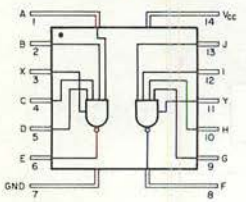
NOTE: Positive logic is used in specifications

TRUTH TABLE

A	B	C	D	X	E
G	H	I	J	Y	F
1	1	1	1	1	0
0	1	1	1	1	1
1	0	1	1	1	1
1	1	0	1	1	1
1	1	1	0	1	1
1	1	1	1	0	1
0	0	0	0	0	1

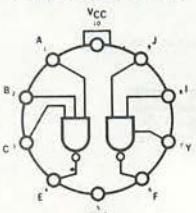
1 IS HIGH VOLTAGE
0 IS LOW VOLTAGE

FLAT PACK



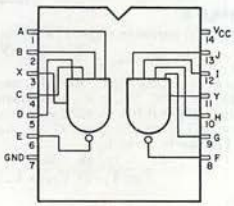
TOP VIEW

SIMILAR TO TO-5



TOP VIEW

DUAL IN-LINE



TOP VIEW

ABSOLUTE MAXIMUM RATINGS[1]

		UNITS
Supply Voltage (V_{CC}), −55°C to +125°C, Continuous	−.5 to +8	Volts
Supply Voltage (V_{CC}), Pulsed, <1 sec	+12	Volts
Output Current, Into Outputs	30	mA
Input Forward Current	−10	mA
Input Reverse Current	1	mA
Operating Temperature	−55 to +125	°C
Storage Temperature	−65 to +150	°C
Operating Junction Temperature[2]	+175	°C
Input Voltage Applied to Input	−1.5 to +5.5	V
Lead Temp. (soldering, 60 sec.)	300	°F

NOTES: 1. Above which useful life may be impaired.
2. Allow 200°C/Watt θ_{J-A} for TO-5; 300°C/Watt θ_{J-A} for ¼" x ¼" flatpack and dual in-line. Allow 50°C/Watt θ_{J-C} for TO-5; 180°C/Watt θ_{J-C} for ¼" x ¼" flatpack and dual in-line. Heat removal in ¼" x ¼" flatpack is highly dependent upon contact surfaces or air flow and on lead attachment and thermal paths thru leads, as well as number of soldered leads.

SUMMARY OF MIC 930 AND 961 CHARACTERISTICS (25°C)

Parameter		Note	FULL TEMPERATURE RANGE			LIMITED TEMPERATURE RANGE			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
Operating Supply Voltage		1	4.5	5.0	5.5		5.0		Volts
Network Dissipation	930	2		17	32.5		17	40	mW
	961			25	54.5		25	59	
Loading D.C. fan-out	930			8			8		DTL Unit
	961			7			7		Load
Output Logic 'I' (High)	930		2.6			2.6			Volts
	961		2.6			4.3			
'O' (Low)	930				0.4			0.45	
	961				0.4			0.5	
Input Threshold 'I' (High)		3	1.9			1.9			Volts
'O' (Low)					1.1			1.1	
Propagation $t_{pd}+$	930	4	25		80	25		80	Nano-
Delay Time	961		15		50	15		50	Second
$t_{pd}-$	930		10		30	10		30	
	961		10		30	10		30	
Noise Immunity		5	0.35	>.50		0.35	>.50		Volts

NOTES: 1. Exact specification limits for operating temperature range may be obtained by reference to the appropriate test.
2. Power supplied from V_{CC} supply (V_{CC} = 5V) during "ON" state, fan-out = 0.
3. Input threshold voltage is defined as the minimum (or maximum) voltage at the circuit input to guarantee a low (or high) output.
4. Propogation delay time terms ($t_{pd}+$ and $t_{pd}-$) are described in the t_{pd} test circuit, Page 8.
5. See Noise test circuit, Page 7, and Loading Factors, Page 5.

MIC 930 TIME DELAYS VS. CAPACITIVE LOADS

FIG. 47

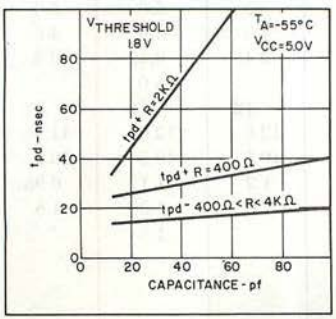


FIG. 48

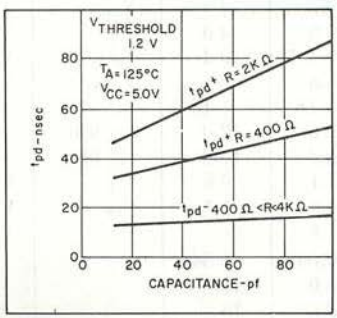
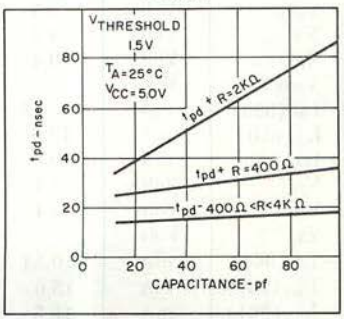


FIG. 49



TEST SEQUENCE

Abbreviated Test Sequences for the 930 and 961 elements are shown below. The ground pin is grounded on all tests.

Test No.	Notes	FORCING CONDITIONS								LIMITS	
		Pin A (G)	Pin B (H)	Pin C (I)	Pin D (J)	Pin X (Y)	Pin E (F)	V_{CC}	Sense	Min.	Max.
1, (2)		V_{IH}	V_{IH}	V_{IH}	V_{IH}		I_{OL}	V_{CCL}	V_E (V_F)		V_{OL}
3, 4, 5, 6											
(7, 8, 9, 10)	2, 3	V_{IL}	V_{IL}	V_{IL}	V_{IL}		$-I_{OH}$	V_{CCL}	V_E (V_F)	V_{OH}	
11, (12)		V_R	GND	GND	GND			V_{CCH}	I_A (I_G)		I_R
13, (14)		GND	V_R	GND	GND			V_{CCH}	I_B (I_H)		I_R
15, (16)	3	GND	GND	V_R	GND			V_{CCH}	I_C (I_I)		I_R
17, (18)	3	GND	GND	GND	V_R			V_{CCH}	I_D (I_J)		I_R
19, (20)		V_F	V_R	V_R	V_R			V_{CCH}	I_A (I_G)		$-I_F$
21, (22)		V_R	V_F	V_R	V_R			V_{CCH}	I_B (I_H)		$-I_F$
23, (24)	3	V_R	V_R	V_F	V_R			V_{CCH}	I_C (I_I)		$-I_F$
25, (26)	3	V_R	V_R	V_R	V_F			V_{CCH}	I_D (I_J)		$-I_F$
27, (28)		GND					V_{CEX}	V_{CEX}	I_E (I_F)		I_{CEX}
29, (30)		GND					GND	V_{CCH}	I_E (I_F)	$-I_{SC}$	$-I_{SC}$
31								V_{PD}	I_{VCC}		I_{PDH}
32	4	GND						V(max)	I_{VCC}		I(max)
33, (34)	3					V_X	$-I_{OH}$	V_{CCL}	V_E (V_F)	V_{OH}	
35, 36		$t_{pd}+$, $t_{pd}-$ —See table of test circuit conditions and limits, Page 17									
37, (38)		V_F	V_R	V_R	V_R			V_{CCL}	I_A (I_G)		$-I_{F2}$
39, (40)		V_R	V_F	V_R	V_R			V_{CCL}	I_B (I_H)		$-I_{F2}$
41, (42)	3	V_R	V_R	V_F	V_R			V_{CCL}	I_C (I_I)		$-I_{F2}$
43, (44)	3	V_R	V_R	V_R	V_F			V_{CCL}	I_D (I_J)		$-I_{F2}$
45, (46)		V_{IH}	V_{IH}	V_{IH}	V_{IH}		I_{OL2}	V_{CCH}	V_E (V_F)		V_{OL2}
47	6	GND	GND	GND	GND			V_{PD}	I_{VCC}		I_{PDL}

NOTES:

1. Both elements are dual "NAND" gates; therefore, the test sequences for each are identical. Tests on each side of the dual are identical; therefore, matching test and pin numbers are shown in parentheses.
2. V applied individually to 1 input each test. Other inputs open.
3. Delete these tests for 10-pin TO-5 package: 6, 9, 10, 16, 17, 18, 24, 25, 26, 33, 41, 42, 43, 44.
4. Ground one input on each gate.
5. Tests 37/47 apply to full temperature range only.
6. Ground all inputs simultaneously.

FORCING CONDITIONS — 930,961

FULL TEMPERATURE RANGE					LIMITED TEMPERATURE RANGE				
Parameter	Units	−55° C	+25° C	+125° C	Parameter	Units	0° C	+25° C	+75° C
V(max)	Volts		8.0		V (max)	Volts		8.0	
V_{PD}	Volts		5.0		V_{PD}	Volts		5.0	
V_{CCH}	Volts	5.5	5.5	5.5	V_{CCH}	Volts	5.0	5.0	5.0
V_{CCL}	Volts	4.5	4.5	4.5	V_{CCL}	Volts	5.0	5.0	5.0
V_R	Volts	4.0	4.0	4.0	V_R	Volts	4.0	4.0	4.0
V_F	Volts	0.4	0.4	0.4	V_F	Volts	0.45	0.45	0.5
V_{CEX}	Volts		4.5		V_{CEX}	Volts		5.0	
$-I_{OH}$(930)	mA	.18	.18	.18	$-I_{OH}$	mA	.12	.12	.12
I_{OL1} 930	mA	12.0	12.0	12.0	I_{OL} 930	mA	12.0	12.0	11.4
I_{OL1} 961	mA	10.8	10.8	10.8	I_{OL} 961	mA	10.5	10.5	10.2
V_{IL}	Volts	1.4	1.1	0.8	V_{IL}	Volts	1.2	1.1	0.95
V_{IH}	Volts	2.1	1.9	1.7	V_{IH}	Volts	2.0	1.9	1.8
V_X	Volts		1.8		V_X	Volts		1.8	
$-I_{OH}$(961)	mA	0.54	0.54	0.54					
I_{OL2}(930)	mA	15.0	15.0	15.0					
I_{OL2}(961)	mA	13.5	13.5	13.5					

TEST LIMITS

Parameter MIC 930	Units	FULL TEMPERATURE RANGE						LIMITED TEMPERATURE RANGE					
		−55°C		+25°C		+125°C		0°C		+25°C		+75°C	
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.
V_{OL1}	Volts		.40		.40		.40		.45		.45		.50
V_{OH}	Volts	2.5		2.6		2.5		2.6		2.6		2.5	
I_R	μA		2.0		2.0		5.0		5.0		5.0		10.0
$-I_{F1}$	mA		1.5		1.5		1.4		1.40		1.40		1.33
I_{CEX}	μA				50.0						100		
$-I_{SC}$	mA	.610	1.34	.610	1.34	.535	1.30	.610	1.30	.610	1.30	.535	1.25
I(max)	mA				5.50						8.0		
I_{PDH}	mA				6.50						8.0		
$-I_{F2}$	mA		1.16		1.16		1.08						
V_{OL2}	Volts		.4		.4		.4						
I_{PDL}	mA		2.0		2.94								
MIC 961													
V_{OL1}	Volts		.40		.40		.45		0.50		0.50		0.55
V_{OH}	Volts	2.5		2.6		2.5		4.3		4.3		4.2	
I_R	μA		2.0		2.0		5.0		5.0		5.0		10.0
$-I_{F1}$	mA		1.5		1.5		1.4		1.40		1.40		1.33
I_{CEX}	μA				50.0						100		
$-I_{SC}$	mA	2.1	3.7	2.1	3.7	1.86	3.28			1.85	3.68		
I(max)	mA				5.2						5.72		
I_{PDH}	mA				10.9						11.8		
$-I_{F2}$	mA		1.16		1.16		1.08						
V_{OL2}	Volts		.4		.4		.4						
I_{PDL}	mA				2.94								

PROPAGATION DELAY Tpd TESTS

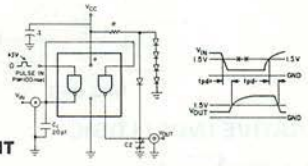


FIG. 50 tpd TEST CIRCUIT

t_{pd}— of 930, 961 elements will be read from input at 1.5 V.

All diodes 1N916 or equivalent.

C_1 and C_2 includes probe and jig capacitance.

$V_{Threshold}$= 1.5V at 25°C; at other temperatures $V_{Threshold}$ will be stated.

TABLE OF CONDITIONS & LIMITS t_{pd} TESTS

(See Test Circuit.)
(V_{CC} = 5V, T = 25°C)

		R	C_2 (pf)	Min. (nsec)	Max. (nsec)
$t_{pd}+$	930	3.9 K	30	25	80
$t_{pd}-$	930	400 Ω	50	10	30
$t_{pd}+$	930	400 Ω	50	15	40 [1]
$t_{pd}-$	930	3.9 K	20	5	20 [1]
$t_{pd}+$	961	3.9 K	30	15	50
$t_{pd}-$	961	400 Ω	50	10	30

NOTE: 1. Correlating limit provided as design information only.

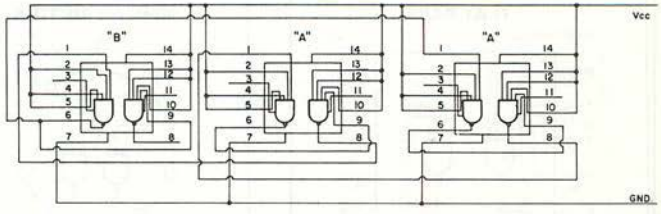
RELIABILITY TESTS

PERFORMED DURING ITT RELIABILITY PROGRAM

MEASUREMENTS OF THE FOLLOWING PARAMETERS ARE RECORDED:

Parameter	Test Sequence Number on Page 16
V_{OL}	#1
V_{OH}	#4
I_R	#15 & #16
I_F	#20 & #25
I(max)	#32

FIG. 51 **LIFE TEST CIRCUIT**



NOTE: V_{CC}= +5.5 Volts Ambient Temperature= +125° C
Circuit may have any number of units connected like "A", with one connected like "B". The circuit must contain an odd number of gates in series in the ring.

DUAL FOUR-INPUT BUFFER MIC 932
DUAL FOUR-INPUT POWER GATE MIC 944

DESCRIPTION

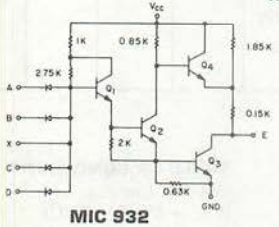
The MIC 932 and MIC 944 elements are dual four-input NAND/NOR buffer and power gates respectively.

Both elements have typical output currents of up to 100 ma. This enables them to provide much higher fan-out than a typical NAND/NOR gate. Both elements are extendable. The MIC 932 incorporates an emitter follower pull-up which combines high fan-out with superior capacitance driving capability.

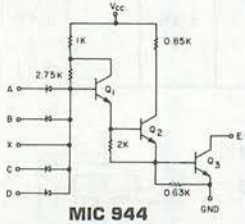
The MIC 932 cannot be externally connected to perform the "wired OR" logic function. The MIC 944, which does not incorporate the emmitter pull-up, can be used either as a high fan-out interface driver or low power lamp driver. The output can be tied to an external pull-up resistor and returned to a supply voltage of up to 12 volts. The supply may be located near the output or at the far end of an open transmission line or twisted pair interconnection. This allows the MIC 944 to be used as a line driver.

The MIC 944 can be externally connected to perform the "wired OR" logic function.

CIRCUIT SCHEMATIC
(ONE GATE ONLY)



MIC 932



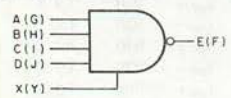
MIC 944

TRUTH TABLE

A	B	C	D	X	E
G	H	I	J	Y	F
1	1	1	1	1	0
0	1	1	1	1	1
1	0	1	1	1	1
1	1	0	1	1	1
1	1	1	0	1	1
1	1	1	1	0	1
0	0	0	0	0	1

1 IS HIGH VOTAGE
0 IS LOW VOLTAGE

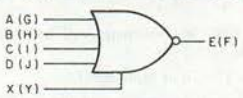
POSITIVE (NAND) LOGIC



$E = \overline{A \cdot B \cdot C \cdot D \cdot (X)}$

$F = \overline{G \cdot H \cdot I \cdot J \cdot (Y)}$

NEGATIVE (NOR) LOGIC

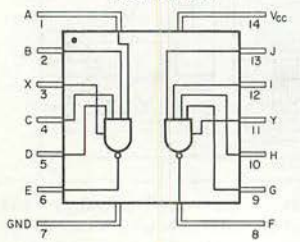


$E = \overline{A + B + C + D + (X)}$

$F = \overline{G + H + I + J + (Y)}$

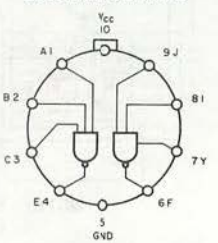
NOTE: Positive logic is used in specifications

FLAT PACK



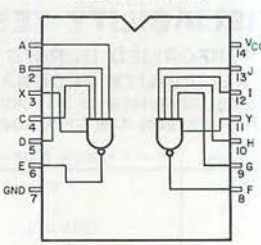
TOP VIEW

SIMILAR TO TO-5



TOP VIEW

DUAL IN-LINE



TOP VIEW

ABSOLUTE MAXIMUM RATINGS[1]

	UNITS
Supply Voltage (V_{CC}), −55°C to +125°C, Continuous ..... −.5 to +8.0	Volts
Supply Voltage (V_{CC}), pulsed, <1.0 sec. ..... +12	Volts
Output Current, into Outputs, Continuous 150	mA
Output Current, into Outputs, pulsed, <30 milliseconds 300	mA
Input Forward Current ..... −10	mA
Input Reverse Current 1	mA
Operating Ambient Temperature ..... −55 to +125	°C
Storage Temperature ..... −65 to +150	°C
Operating Junction Temperature[2] ..... +175	°C
Input Voltage Applied to Input ..... −1.5 to +5.5	Volts
Lead Temp. (soldering, 60 sec.) 300	°C

NOTES: 1. Above which useful life may be impaired.

2. Allow 200°C/Watt θ_{J-A} for TO-5; 300°C/Watt θ_{J-A} for ¼" x ¼" flatpack and dual in-line. Allow 50°C/Watt θ_{J-C} for TO-5; 180°C/Watt θ_{J-C} for ¼" x ¼" flatpack and dual in-line. Heat removal in ¼" x ¼" flatpack is highly dependent upon contact surfaces or air flow and on lead attachment and thermal paths thru leads, as well as number of soldered leads.

SUMMARY OF MIC 932 AND 944 CHARACTERISTICS (25°C)

Parameter		Note	FULL TEMPERATURE RANGE			LIMITED TEMPERATURE RANGE			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
Operating Supply Voltage		1	4.5	5.0	5.5		5.0		Volts
Network Dissipation	932	2		56.0	133.0		56.0	150.0	mW
	944			44.0	100.0		44.0	100.0	
Loading D.C. Fanout					25.0			25.0	DTL Unit Load
Output Logic '1' (High)	932			2.6			2.6		Volts
	944								
'0' (Low)	932				0.4			0.45	
	944				0.4			0.45	
Input Threshold '1' (High)		3	1.9			1.9			Volts
'0' (Low)					1.1			1.1	
Propagation $t_{pd}+$	932	4	25.0		80.0	25.0		80.0	Nano-
Delay Time	944		15.0		50.0	15.0		50.0	Second
$t_{pd}-$	932		15.0		40.0	15.0		40.0	
	944		10.0		35.0	10.0		35.0	
Noise Immunity		5	0.35	>0.5		0.35	>0.5		Volts

NOTES: 1. Exact specification limits for operating temperature range may be obtained by reference to the appropriate test.

2. Power supplied from V_{CC} (5V) during "ON" state fan-out = 0.

3. Input threshold voltage is defined as the minimum (or maximum) voltage at the circuit input to guarantee a low (or high) output.

4. Propogation delay time terms ($t_{pd}+$ and $t_{pd}-$) are described in the t_{pd} test circuit, Page 8.

5. See Loading Factors, Page 5.

TEST SEQUENCE

Both elements are dual "NAND" gates; therefore, the test sequences for each are identical. Tests on each side of the dual are identical; therefore, matching test and pin numbers are shown in parentheses.

Test No.	Notes	Pin A (G)	Pin B (H)	Pin C (I)	Pin D (J)	Pin X (Y)	Pin E (F)	V_{CC}	Sense	LIMITS Min.	LIMITS Max.
1, (2)		V_{IH}	V_{IH}	V_{IH}	V_{IH}		I_{OL}	V_{CCL}	$V_E(V_F)$		V_{OL}
3, 4, 5, 6, (7, 8, 9, 10)	1, 3	V_{IL}	V_{IL}	V_{IL}	V_{IL}		I_{OH}	V_{CCL}	$V_E(V_F)$	V_{OH}	
11, (12)		V_R	GND	GND	GND			V_{CCH}	$I_A(I_G)$		I_R
13, (14)		GND	V_R	GND	GND			V_{CCH}	$I_B(I_H)$		I_R
15, (16)		GND	GND	V_R	GND			V_{CCH}	$I_C(I_I)$		I_R
17, (18)		GND	GND	GND	V_R			V_{CCH}	$I_D(I_J)$		I_R
19, (20)		V_F	V_R	V_R	V_R			V_{CCH}	$I_A(I_G)$		I_F
21, (22)		V_R	V_F	V_R	V_R			V_{CCH}	$I_B(I_H)$		I_F
23, (24)		V_R	V_R	V_F	V_R			V_{CCH}	$I_C(I_I)$		I_F
25, (26)		V_R	V_R	V_R	V_F			V_{CCH}	$I_D(I_J)$		I_F
27, (28)	3	GND					V_{CEX}	V_{CEX}	$I_E(I_F)$		I_{CEX}
29, (30)	2, 3	GND					GND	V_{CCH}	$I_E(I_F)$	I_{SC}	
31								V_{PD}	I_{VCC}		I_{PDH}
32	2,	GND						V(max)	I_{VCC}		I(max)
33, (34)	3					V_X	I_{OH}	V_{CCL}	$V_E(V_F)$	V_{OH}	
35, 36		$t_{pd}+$, $t_{pd}-$ See Table of test circuit conditions and limits, Page 21									
35, 36, 37, 38, (39, 40, 41, 42)	1, 4	V_{IL}	V_{IL}	V_{IL}	V_{IL}		V_{CEX}	V_{CCH}	$I_E(I_F)$		I_{CEX}
43, (44)	4					V_X	V_{CEX}	V_{CCH}	$I_E(I_F)$		I_{CEX}
45, (46)	4	GND					I_{CE}	V_{CCH}	$V_E(V_F)$	LV_{CE}	
47, (48)		V_F	V_R	V_R	V_R			V_{CCL}	$I_A(I_G)$		$-I_{F2}$
49, (50)		V_R	V_F	V_R	V_R			V_{CCL}	$I_B(I_H)$		$-I_{F2}$
51, (52)		V_R	V_R	V_F	V_R			V_{CCL}	$I_C(I_I)$		$-I_{F2}$
53, (54)		V_R	V_R	V_R	V_F			V_{CCL}	$I_D(I_J)$		$-I_{F2}$
54, (55)		V_{IH}	V_{IH}	V_{IH}	V_{IH}		I_{OL2}	V_{CCH}	$V_E(V_F)$		V_{OL2}
56	6	GND	GND	GND	GND			V_{PD}	I_{VCC}		I_{PDL}

NOTES: 1. V applied individually to 1 input each test. Other inputs open. 2. Apply GND to both pins A and G. 3. MIC 932 only. 4. MIC 944 only. 5. On 10 Pin TO-5 units, pins D, X, I and J are omitted. Thus tests 6, 9, 10, 16, 17, 18, 24, 25, 26, 33, 38, 41, 42 and 43 do not apply. 6. Ground all inputs simultaneously. 7. Tests 45/56 apply to full temperature range only.

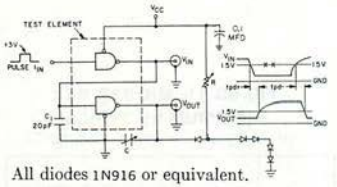
FORCING CONDITIONS

Parameter	Units	FULL TEMPERATURE RANGE −55°C	FULL TEMPERATURE RANGE +25°C	FULL TEMPERATURE RANGE +125°C	Parameter	Units	LIMITED TEMPERATURE RANGE 0°C	LIMITED TEMPERATURE RANGE +25°C	LIMITED TEMPERATURE RANGE +75°C
V_{CCH}	Volts	5.5	5.5	5.5	V_{CCH}	Volts	5.0	5.0	5.0
V_{CCL}	Volts	4.5	4.5	4.5	V_{CCL}	Volts	5.0	5.0	5.0
V_{CEX} (932)	Volts		4.5		V_{CEX}(932)	Volts		5.0	
V_{MAX}	Volts		8.0		V_{MAX}	Volts		8.0	
V_{PD}	Volts		5.0		V_{PD}	Volts		5.0	
V_{IH}	Volts	2.1	1.9	1.7	V_{IH}	Volts	2.0	1.9	1.8
V_{IL}	Volts	1.4	1.1	0.8	V_{IL}	Volts	1.2	1.1	0.95
V_F	Volts	0.4	0.4	0.4	V_F	Volts	0.45	0.45	0.5
V_R	Volts	4.0	4.0	4.0	V_R	Volts	4.0	4.0	4.0
V_X	Volts		1.8		V_X	Volts		1.8	
$-I_{OH}$ (932)	mA	2.0	2.5	4.0	$-I_{OH}$ (932)	mA	2.0	2.5	3.0
I_{OL1}	mA	36.0	36.0	36.0	I_{OL1}	mA	36.0	36.0	34.0
I_{OL2}	mA	37.5	37.5	37.5	I_{OL2}				
I_{CE} (944)	mA	5.0	5.0	5.0	I_{CE} (944)	mA	5.0	5.0	5.0
V_{CEX} (944)	Volts	4.5	4.5	4.5	V_{CEX}(944)	Volts		5.0	

TEST LIMITS

Parameter	Units	FULL TEMPERATURE RANGE						LIMITED TEMPERATURE RANGE					
		−55°C		+25°C		+125°C		0°C		+25°C		+75°C	
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.
V_{OL}	Volts		0.4		0.4		0.45		0.45		0.45		0.5
V_{OH} (932)	Volts	2.5		2.6		2.50		2.6		2.6		2.5	
I_R	μA		2.0		2.0		5.0		5.0		5.0		10.0
$-I_F$	mA		1.6		1.6		1.5		1.4		1.4		1.33
$-I_{SC}$ (932)	mA	16.0		18.0		16.0		15.0		16.0		14.0	
I_{PDH} (932)	mA				26.6						30.0		
I_{PDH} (944)	mA				20.0						20.0		
$-I_{MAX}$ (932)	mA				6.0						8.0		
$-I_{MAX}$ (944)	mA				6.0						6.0		
I_{CEX} (932)	μA				50.0						100.0		
I_{CEX} (944)	μA		50.0		100.0		200.0				100.0		
LV_{CE}(944)	Volts			6.0						6.0			
$-I_{F2}$	mA		1.16		1.16		1.08						
V_{OL2}	Volts		.4		.4		.4						
I_{PDL}	mA				2.94								

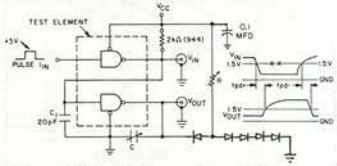
CIRCUIT FOR MIC 932
FIG. 52



All diodes 1N916 or equivalent.

C_1 and C includes probe and jig capacitance.

CIRCUIT FOR MIC 944
FIG. 53



C_1 and C includes probe and jig capacitance.

PROPAGATION DELAY

tpd TESTS

TABLE OF CONDITIONS & LIMITS tpd TESTS

(See Test Circuit.)

(V_{CC} = 5V, T = 25°C)		R (Ω)	C (pf)	Min. (nsec)	Max. (nsec)
$t_{pd}+$	944	510	20	15	50
$t_{pd}-$	944	150	100	10	35
$t_{pd}+$	932	510	500	25	80
$t_{pd}-$	932	150	500	15	40
$t_{pd}+$	944	150	20	10	35 (1)
$t_{pd}-$	944	510	20	5.0	20 (1)
$t_{pd}+$	932	150	500	20	65 (1)
$t_{pd}-$	932	510	200	8.0	30 (1)

NOTE: 1. Correlating limit provided as design information only.

TYPICAL tpd VS. CAPACITY

FIG. 54 MIC 932, 944

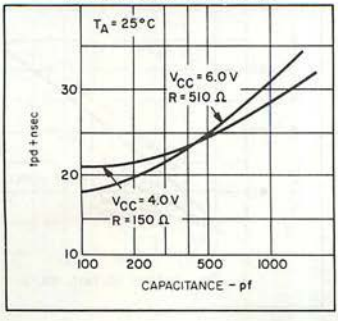


FIG. 55 MIC 944

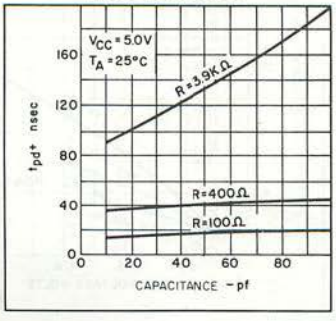
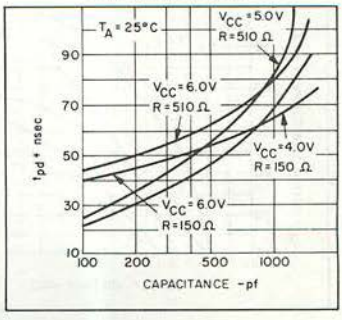


FIG. 56 MIC 932



ADDITIONAL CHARACTERISTICS

FIG. 57 TYPICAL POWER DISSIPATION PER SIDE VS. SUPPLY VOLTAGE
(OUTPUT NOT LOADED) (932, 944)

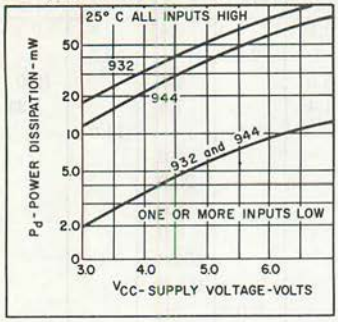


FIG. 58 DTL INPUT THRESHOLDS VS. TEMPERATURE (932, 944)

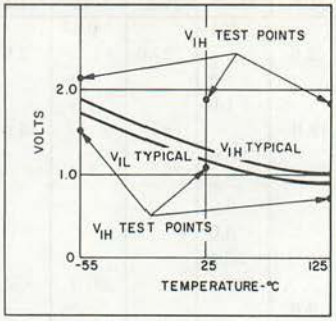


FIG. 59 TYPICAL OUTPUT CURRENT WITH INPUTS LOW (932)

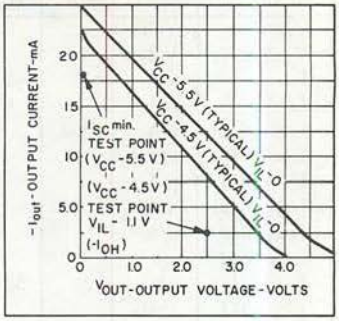


FIG. 60

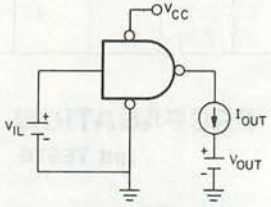


FIG. 61

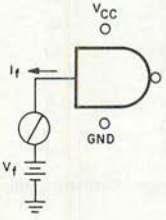


FIG. 62 1 I_F MIC 932, 944 MAXIMUM VS. TYPICAL
(T_A = −55°C & +25°C)

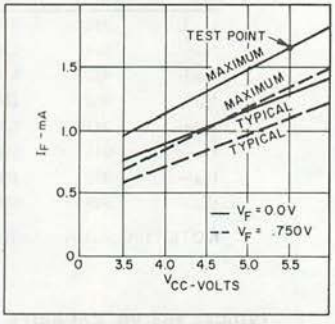


FIG. 63 1 I_F MIC 932, 944 MAXIMUM VS. TYPICAL
(V_F = OV & V_F = .750V T_A = +125°C)

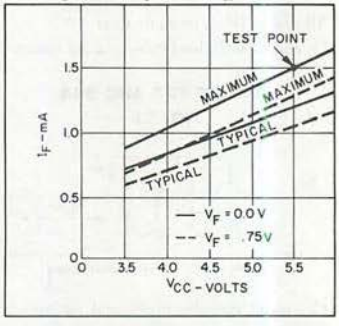


FIG. 64 TYPICAL OUTPUT LOW CURRENT VS. SUPPLY VOLTAGE
(−55°C and +25°C) (932)

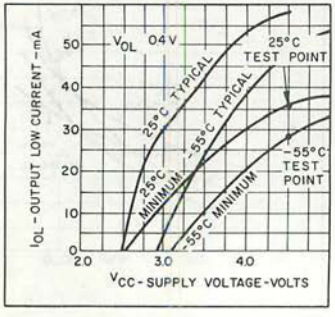


FIG. 65 TYPICAL OUTPUT LOW CURRENT VS. OUTPUT VOLTAGE
(+125°C) (932)

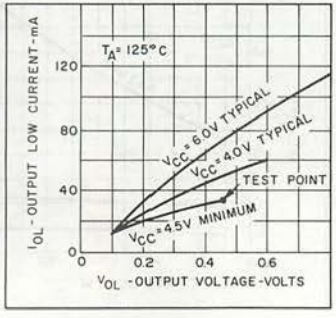


FIG. 66 TYPICAL OUTPUT LOW CURRENT VS. OUTPUT VOLTAGE
(+125°C) (944)

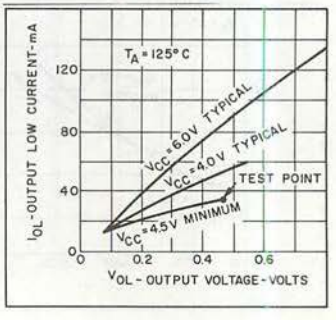
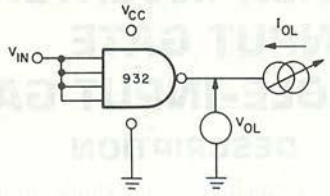


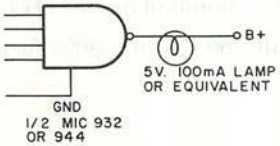
FIG. 67



MISCELLANEOUS APPLICATIONS

NOTE: In some of these applications, use of the elements is made within the design of the element but beyond the guaranteed test limits on page 23. Consult your sales representative for additional information and/or selection requirements.

FIG. 68



LAMP DRIVING

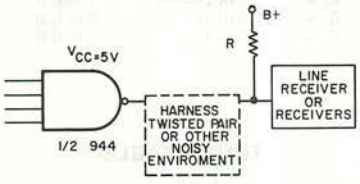
Suggested Ratings $T_A \leq 75°C$: Power Dissipation TO-5 400 mW Maximum—Power Dissipation Flatpak 240 mW Maximum.

Maximum "hot" lamp current		Maximum "hot" lamp current	
120 mA TO-5	one side only ON	90 mA TO-5	both sides ON
100 mA Flatpak	one side only ON	75 mA Flatpak	both sides ON

"Cold" lamp current is limited by saturation resistance, emitter resistance, and base current to about 200 to 250 mA.
The most significant thermal time constants for 932 and 944: TO-5 Package 50 msec Cerpak 100 msec.
Thermal time constant is measured by forward diode drop in one gate with power pulsed into opposite gate. A high current β selection is desirable in this application.

INTERFACING

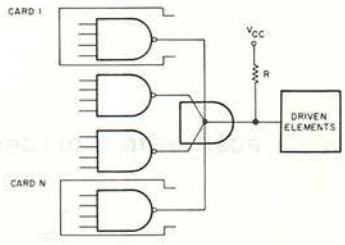
FIG. 69



B^+ up to 12 volts. Line Receiver may have nominal low level ≤ 1 volt; nominal threshold $\approx$ 4V and nominal high level ≥ 8V, for example. Resistor selected should be as low as possible consistent with required low input level of receiver, number of receivers, and power dissipation of system. For a guaranteed V_{OH} level above 6 volts, an LV_{CE} selection may be desirable; for use of resistor that requires the 944 to sink more than 40 mA (at V_{OL} above .40 volt), a high current $I_{OL} - V_{OL}$ selection may be desirable.

POWER GATING

FIG. 70



Each output driver is ½ MIC 944. Note that the MIC 944 is a direct high fan-out replacement for MIC 930, except that an external resistor must be used.

RELIABILITY TESTS

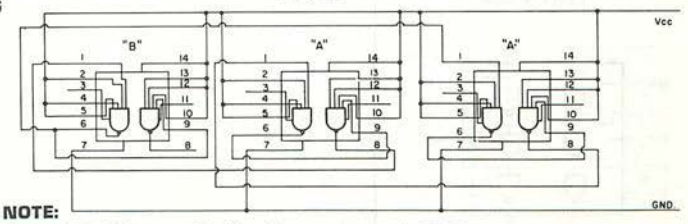
PERFORMED DURING ITT RELIABILITY PROGRAM

MEASUREMENTS OF THE FOLLOWING PARAMETERS ARE RECORDED:

	Parameter	Test Sequence Number on Page 20
932	V_{OL}	#1
	V_{OH}	#4
	I_R	#15 & #16
	I_F	#20 & #25
	I_{MAX}	#32
944	V_{OL}	#1
	I_R	#15
	I_R	#16
	I_F	#20
	I_F	#25
	I_{MAX}	#32
	I_{CEX}	#36

LIFE TEST CIRCUIT

FIG. 71



NOTE:
V_{CC} = +5.5 Volts Ambient Temperature = +125°C
Circuit may have any number of units connected like "A", with one connected like "B". The circuit must contain an odd number of gates in series in the ring.

EXTENDABLE HEX INVERTER MIC 935
HEX SINGLE-INPUT GATE MIC 936
FAST HEX SINGLE-INPUT GATE MIC 937

DESCRIPTION

The MIC 935, MIC 936, and MIC 937 elements are hex single-input inverters.

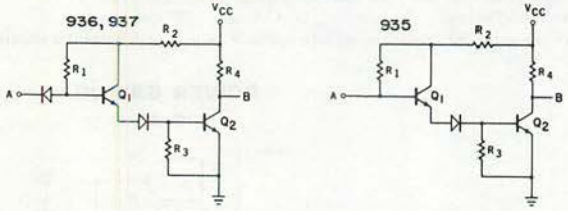
The MIC 935 is intended for use with discrete diode expansion of the input. When extending inputs with diodes, care should be taken to minimize capacitance on the input node.

These inverter gates can be cross-coupled to form a flip-flop or the outputs can be tied together to perform the "wired OR" function.

The MIC 936 incorporates a 6K output pull-up resistor which allows for a fan-out of up to 8 DTL loads.

The MIC 937 incorporates a 2K output pull-up resistor which typically results in a 30% faster rise time with capacitive loads at a fan-out of up to 7 DTL loads.

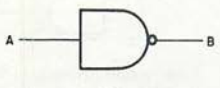
CIRCUIT SCHEMATICS
(ONE GATE ONLY)



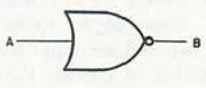
TYPICAL RESISTOR VALUES

	935, 936	937
R_1 =	2.00K Ω	2.00K Ω
R_2 =	1.75K Ω	1.75K Ω
R_3 =	5.00K Ω	5.00K Ω
R_4 =	6.00K Ω	2.00K Ω

POSITIVE (NAND) LOGIC



NEGATIVE (NOR) LOGIC



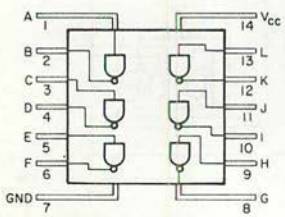
TRUTH TABLE

A	B
1	0
0	1

"1" IS HIGH
"0" IS LOW

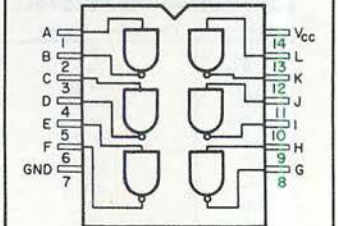
NOTE: POSITIVE LOGIC IS USED IN SPECIFICATION

FLAT PACK



TOP VIEW

DUAL IN-LINE



TOP VIEW

ABSOLUTE MAXIMUM RATINGS[1]

	UNITS
Supply Voltage (V_{CC}), −55°C to +125°C, Continuous ..... −1.5 to +8	Volts
Supply Voltage (V_{CC}), Pulsed, <1 sec ..... +12	Volts
Output Current, Into Outputs 30	mA
Input Current (935) 5	mA
Input Forward Current ..... −10	mA
Input Reverse Current 1	mA
Operating Temperature ..... −55 to +125	°C
Storage Temperature ..... −65 to +150	°C
Operating Junction Temperature[2] ..... +175	°C
Input Voltage Applied to Input ..... −1.5 to +5.5	V
Lead Temp. (soldering, 60 sec.) 300	°C

NOTES: 1. Above which useful life may be impaired.

2. Allow 200°C/Watt θ_{J-A} for TO-5; 300°C/Watt θ_{J-A} for ¼" x ¼" flatpack and dual in-line. Allow 50°C/Watt θ_{J-C} for TO-5; 180°C/Watt θ_{J-C} for ¼" x ¼" flatpack and dual in-line. Heat removal in ¼" x ¼" flatpack is highly dependent upon contact surfaces or air flow and on lead attachment and thermal paths thru leads, as well as number of soldered leads.

SUMMARY OF MIC 936 AND 937 CHARACTERISTICS (25°C)

Parameter		Note	FULL TEMPERATURE RANGE			LIMITED TEMPERATURE RANGE			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
Operating Supply Voltage		1	4.5	5.0	5.5		5.0		Volts
Network Dissipation	935	2			93.0			110.0	mW
	936	2			97.5			115.0	mW
	937				163.5			177.5	mW
Loading D.C. fan-out	935, 936				8.0			8.0	DTL Unit
	937				7.0			7.0	Load
Output Logic '1'	935, 936		2.6			2.6			Volts
Levels (High)	937		2.6			3.8			Volts
Output Logic 'O'	935, 936				0.4			0.45	Volts
Levels (Low)	937				0.4			0.50	Volts
Input Threshold '1'	936	3	1.9			1.9			Volts
	935	3	2.6						Volts
'O'					1.8			1.8	Volts
Propagation $t_{pd}+$	935, 936	4	25.0		80.0	25.0		80.0	Nanosec.
Delay Time	937		15.0		50.0	15.0		50.0	Nanosec.
$t_{pd}-$	936, 937		10.0		30.0	10.0		30.0	Nanosec.
	935		10.0		40.0				
Noise Immunity		5	350.0	>500.0		350.0	>500.0		mV

NOTES: 1. Exact specification limits for operating temperature range may be obtained by reference to the appropriate test.

2. Power supplied from V_{CC} (5V) during "ON" state fan-out = 0.

3. Input threshold voltage is defined as the minimum (or maximum) voltage at the circuit input to guarantee a low (or high) output.

4. Propogation delay time terms ($t_{pd}+$ and $t_{pd}-$) are described in the t_{pd} test circuit, Page 8.

5. See Loading Factors, Page 5.

FIG. 72

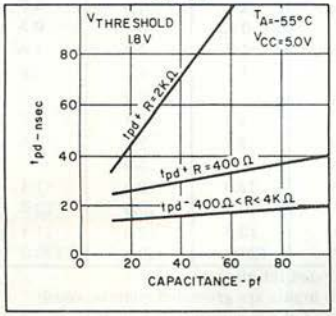


FIG. 73

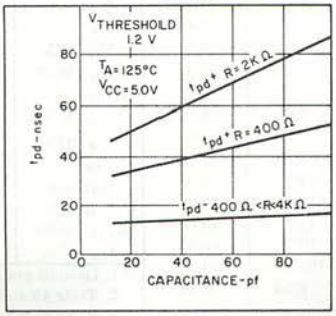
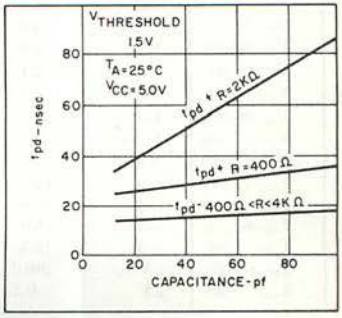


FIG. 74



TEST SEQUENCE*

Test No.	FORCING CONDITIONS AT PINS A	B	C	D	E	F	V_{CC}	Sense	TEST LIMITS Min.	Max.
	L	K	J	I	H	G				
1, (2)	V_{IH}	I_{OL1}	GND		GND		V_{CCL}	$V_B(V_K)$		V_{OL1}
3, (4)	GND		V_{IH}	I_{OL1}	GND		V_{CCL}	$V_D(V_I)$		V_{OL1}
5, (6)	GND		GND		V_{IH}	I_{OL1}	V_{CCL}	$V_F(V_G)$		V_{OL1}
7, (8)	V_F						V_{CCH}	$I_A(I_L)$		I_F
9, (10)			V_F				V_{CCH}	$I_C(I_J)$		I_F
11, (12)					V_F		V_{CCH}	$I_E(I_H)$		I_F
13, (14)	V_R						V_{CCH}	$I_A(I_L)$		I_R
15, (16)			V_R				V_{CCH}	$I_C(I_J)$		I_R
17, (18)					V_R		V_{CCH}	$I_E(I_H)$		I_R
19, (20)	V_{IL}	$-I_{OH}$					V_{CCL}	$V_B(V_K)$	V_{OH}	
21, (22)			V_{IL}	$-I_{OH}$			V_{CCL}	$V_D(V_K)$	V_{OH}	
23, (24)					V_{IL}	$-I_{OH}$	V_{CCL}	$V_F(V_G)$	V_{OH}	
25, (26)	V_{IL2}	V_{CEX}					V_{CEX}	$I_B(I_K)$		I_{CEX}
27, (28)			V_{IL2}	V_{CEX}			V_{CEX}	$I_D(I_I)$		I_{CEX}
29, (30)					V_{IL2}	V_{CEX}	V_{CEX}	$I_F(I_G)$		I_{CEX}
31, (32)	GND	GND					V_{CCH}	$I_B(I_K)$		$-I_{SC}$
33, (34)	GND	GND					V_{CCH}	$I_B(I_K)$	$-I_{SC}$	
35, (36)			GND	GND			V_{CCH}	$I_D(I_I)$		$-I_{SC}$
37, (38)			GND	GND			V_{CCH}	$I_D(I_I)$	$-I_{SC}$	
39, (40)					GND	GND	V_{CCH}	$I_F(I_G)$		$-I_{SC}$
41, (42)					GND	GND	V_{CCH}	$I_F(I_G)$	$-I_{SC}$	
43, (44)							V_{PD}	I_{VCC}		I_{pdh}
45	GND		GND		GND		V_{MAX}	I_{VCC}		I_{MAX}
46, 47	For $t_{pd}+$ and $t_{pd}-$ Conditions and Limits See Page 27.									
48, (49)	V_F						V_{CCL}	$I_A(I_L)$		$-I_{F2}$
50, (51)			V_F				V_{CCL}	$I_C(I_J)$		$-I_{F2}$
52, (53)					V_F		V_{CCL}	$I_E(I_H)$		$-I_{F2}$
54, (55)	V_{IH}	I_{OL2}					V_{CCH}	$V_B(V_K)$		V_{OL2}
56, (57)			V_{IH}	I_{OL2}			V_{CCH}	$V_D(V_I)$		V_{OL2}
58, (59)					V_{IH}	I_{OL2}	V_{CCH}	$V_F(V_G)$		V_{OL2}
60	GND		GND		GND		V_{PD}	I_{VCC}		I_{PDL}

FORCING CONDITIONS

FULL TEMPERATURE RANGE Parameter	Units	−55°C	+25°C	+125°C
V_{MAX}	Volts		8.0	
V_{PD}	Volts		5.0	
V_{CCH}	Volts	5.5	5.5	5.5
V_{CCL}	Volts	4.5	4.5	4.5
V_R	Volts	4.0	4.0	4.0
V_F	Volts	0.4	0.4	0.4
V_{IL} 936, 937	Volts	1.4	1.1	0.8
V_{IL} 935	Volts	2.1	1.8	1.5
V_{IL2}	Volts		0.0	
V_{IH} 936, 937	Volts	2.1	1.9	1.7
V_{IH} 935	Volts	2.8	2.6	2.4
V_{CEX}	Volts		4.5	
I_{OL1} 935, 936	mA	12.0	12.0	12.0
I_{OL1} 937	mA	10.8	10.8	10.8
I_{OL2} 935, 936	mA	15.0	15.0	15.0
I_{OL2} 937	mA	13.5	13.5	13.5
$-I_{OH}$ 935, 936	μA	180.0	180.0	180.0
I_{OH} 937	μA	0.54	0.54	0.54

LIMITED TEMPERATURE RANGE Parameter	Units	0°C	+25°C	+75°C
V_{MAX}	Volts		8.0	
V_{PD}	Volts		5.0	
V_{CCH}	Volts	5.0	5.0	5.0
V_{CCL}	Volts	5.0	5.0	5.0
V_R	Volts	4.0	4.0	4.0
V_F	Volts	0.45	0.45	0.5
V_{IL} 935	Volts	1.9	1.8	1.65
V_{IL} 936, 937	Volts	1.4	1.1	0.8
V_{IL2}	Volts		0.0	
V_{IH} 936, 937	Volts	2.1	1.9	1.7
V_{IH} 935	Volts	2.7	2.6	2.5
V_{CEX}	Volts		5.0	
I_{OL1} 936	mA	12.0	12.0	11.4
I_{OL1} 937	mA	10.5	10.5	10.2
I_{OL} 935, 936	mA	12.0	12.0	11.4
$-I_{OH}$	μA	120.0	120.0	120.0

*1. Ground pin is grounded for all tests.
2. Tests 45 and 60, all inputs are grounded simultaneously.
3. Tests 48/60 apply to full temperature units only.

TEST LIMITS

Parameter	Units	FULL TEMPERATURE RANGE						LIMITED TEMPERATURE RANGE					
		−55°C		+25°C		+125°C		0°C		+25°C		+75°C	
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.
V_{OL}(935, 936)	Volts		0.4		0.4		0.45		0.45		0.45		0.5
V_{OL} (937)	Volts		0.4		0.4		0.45		0.5		0.5		0.55
V_{OH}(935 936)	Volts	2.5		2.6		2.5		2.6		2.6		2.5	
V_{OH} (937)	Volts	2.5		2.6		2.5		4.3		4.3		4.2	
I_R	μA		2.0		2.0		5.0		5.0		5.0		10.0
$-I_F$	mA		1.5		1.5		1.4		1.4		1.4		1.33
I_{CEX}	μA				50.0						100.0		
$-I_{SC}$(935, 936)	mA	0.61	1.34	0.61	1.34	0.535	1.3	0.61	1.3	0.61	1.3	0.535	1.25
$-I_{SC}$ (937)	mA	2.1	3.7	2.1	3.7	1.86	3.28			1.85	3.68		
I_{PDH}(935, 936)	mA				19.2						23.0		
I_{PDH} (937)	mA				32.7						35.5		
I_{MAX}(935,936)	mA				16.5						24.0		
I_{MAX} (937)	mA				16.5						24.0		
$-I_{F2}$ (936, 937)	mA		1.16		1.16		1.08						
$-I_{F2}$ (935)	mA		1.2		1.2		1.2						
V_{OL2}	Volts		0.4		0.4		0.4						
I_{PDL}(936, 937)	mA				8.82								
I_{PDL} (935)	mA				10.2								

PROPAGATION DELAY

tpd TESTS

tpd TEST CIRCUIT MIC 936/937

FIG. 75

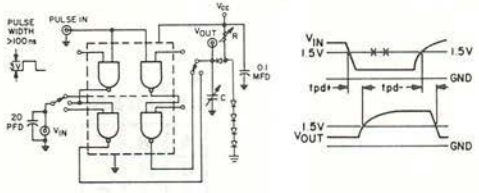


TABLE OF CONDITIONS & LIMITS tpd TESTS

(See Test Circuit.)

(V_{CC} = 5V, T = 25°C)

		R	C	Min.	Max.
$t_{pd}+$	936	3.9 K	30 pf	25 nsec	80 nsec
$t_{pd}-$	936	400 Ω	50 pf	10 nsec	30 nsec
$t_{pd}+$	936	400 Ω	50 pf	15 nsec	40 nsec[1]
$t_{pd}-$	936	3.9 K	20 pf	5 nsec	20 nsec[1]
$t_{pd}+$	937	3.9 K	30 pf	15 nsec	50 nsec
$t_{pd}-$	937	400 Ω	50 pf	10 nsec	30 nsec

NOTE: 1. Correlating limit provided as design information only.

RELIABILITY TESTS

PERFORMED DURING ITT RELIABILITY PROGRAM

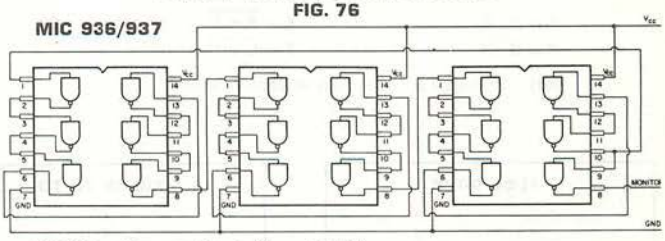
MEASUREMENTS OF THE FOLLOWING PARAMETERS ARE RECORDED:

Parameter	Test Sequence Number on Page 26
935/937 V_{OL}	#1, #2
I_R	#13, #14
I_F	#7, #8
V_{OH}	#19, #20
I_{MAX}	#45

LIFE TEST CIRCUITS

FIG. 76

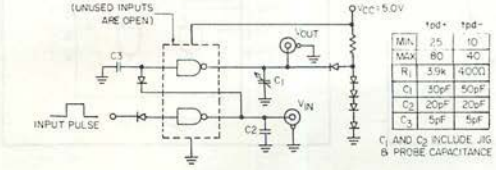
MIC 936/937



NOTES: 1. V_{CC}=5.5V 2. T_a= +125°C

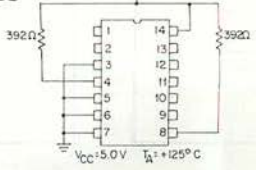
3. Ring must be made up of an odd number of inverters.

tpd TEST CIRCUIT MIC 935



	tpd+	tpd-
MIN.	25	10
MAX	80	40
R_1	3.9k	400Ω
C1	30pF	50pF
C2	20pF	20pF
C3	5pF	5pF

MIC 935



QUAD TWO-INPUT GATE MIC 946
FAST QUAD TWO-INPUT GATE MIC 949

DESCRIPTION

The MIC 946 and MIC 949 elements are quad two-input NAND/NOR gates.

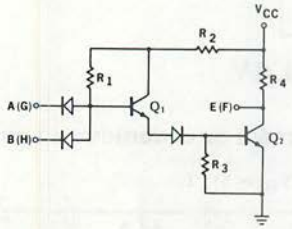
In addition to performing the positive NAND and negative NOR logic functions, the gates can be cross-coupled to form a flip-flop or the outputs can be tied together to perform the "wired OR" function.

These quad two-input gates can also be wired to perform the "exclusive OR" function, while two elements can be wired together to form a full adder.

The MIC 946 incorporates a 6K output pull-up resistor which allows for a fan-out of up to 8 DTL loads.

The MIC 949 incorporates a 2K output pull-up resistor which allows for typically 30% faster rise times with capacitive loads at a fan-out of up to 7 DTL loads.

CIRCUIT SCHEMATIC
(ONE GATE ONLY)



TYPICAL RESISTOR VALUES

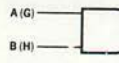
	946	949
R_1 =	2.00K Ω	2.00K Ω
R_2 =	1.75K Ω	1.75K Ω
R_3 =	5.00K Ω	5.00K Ω
R_4 =	6.00K Ω	2.00K Ω

TRUTH TABLE

A	B	E
G	H	F
I	I	O
O	I	I
I	O	I
O	O	I

"I" IS HIGH
"O" IS LOW

POSITIVE (NAND) LOGIC



$E = \overline{A \cdot B}$

$F = \overline{G \cdot H}$

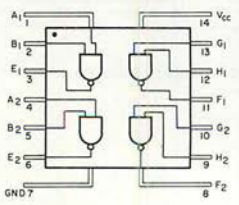
NEGATIVE (NOR) LOGIC

$E = \overline{A + B}$

$F = \overline{G + H}$

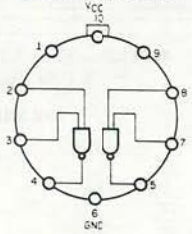
NOTE: POSITIVE LOGIC IS USED IN SPECIFICATION

FLAT PACK



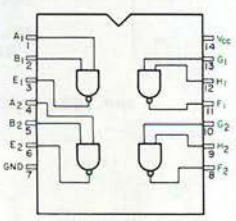
TOP VIEW

SIMILAR TO TO-5



TOP VIEW

DUAL IN-LINE



TOP VIEW

ABSOLUTE MAXIMUM RATINGS[1]

	UNITS
Supply Voltage (V_{CC}), −55°C to +125°C, continuous ..... −.5 to +8	Volts
Supply Voltage (V_{CC}), pulsed, <1 sec ..... +12	Volts
Output Current, into outputs 30	mA
Input Forward Current ..... −10	mA
Input Reverse Current 1	mA
Operating Temperature ..... −55 to +125	°C
Storage Temperature ..... −65 to +150	°C
Operating Junction Temperature[2] ..... +175	°C
Input Voltage Applied to Input ..... −1.5 to +5.5	Volts
Lead Temp. (soldering, 60 sec.) 300	°C

NOTES: 1. Above which useful life may be impaired.
2. Allow 200°C/Watt θ_{J-A} for TO-5; 300°C/Watt θ_{J-A} for ¼" x ¼" flatpack and dual in-line. Allow 50°C/Watt θ_{J-C} for TO-5; 180°C/Watt θ_{J-C} for ¼" x ¼" flatpack and dual in-line. Heat removal in ¼" x ¼" flatpack is highly dependent upon contact surfaces or air flow and on lead attachment and thermal paths thru leads, as well as number of soldered leads.

SUMMARY OF MIC 946 AND 949 CHARACTERISTICS (25° C)

Parameter		Note	FULL TEMPERATURE RANGE			LIMITED TEMPERATURE RANGE			Unit
			Min.	Typ	Max.	Min.	Typ.	Max.	
Operating Supply Voltage		1	4.5	5.0	5.5		5.0		Volts
Network Dissipation	946	2		35.0	65.0		35.0	80.0	mW
	949			50.0	109.0		50.0	117.0	
Loading D.C. fan-out	946				8.0			8.0	DTL Unit
	949				7.0			7.0	Load
Output Logic '1' (High)	946		2.6			2.6			Volts
Levels	949		2.6			4.3			Volts
'0' (Low)	946				0.4			0.45	Volts
	949				0.4			0.50	Volts
Input Threshold '1' (High)		3	1.9			1.9			Volts
'0' (Low)					1.1			1.1	
Propagation	946	4	25.0		80.0	25.0		80.0	Nano-
Delay Time $t_{pd}+$	949		15.0		50.0	15.0		50.0	Second
$t_{pd}-$			10.0		30.0	10.0		30.0	
Noise Immunity		5	350.0	>500.0		350.0	>500.0		mV

NOTES: 1. Exact specification limits for operating temperature range may be obtained by reference to the appropriate test.
2. Power supplied from V_{CC} supply (V_{CC} = 5V) during "ON" state, fan-out = 0.
3. Input threshold voltage is defined as the minimum (or maximum) voltage at the circuit input to guarantee a low (or high) output.
4. Propogation delay time terms ($t_{pd}+$ and $t_{pd}-$) are described in the t_{pd} test circuit, Page 8.
5. See Noise test circuit, Page 7, and Loading Factors, Page 5.

TIME DELAY VS. CAPACITIVE LOADS

FIG. 77

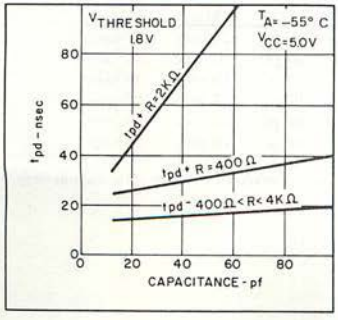


FIG. 78

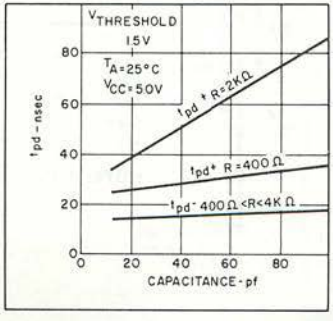
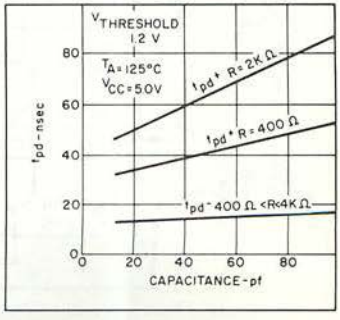


FIG. 79



TEST SEQUENCE

Both elements are "NAND" gates; therefore, the test sequences for each are identical. Tests on each side of the dual are identical; therefore, matching test and pin numbers are shown in parentheses.

Test No.	Notes	FORCING CONDITIONS AT PINS A_1 (G_1)	B_1 (H_1)	E_1 (F_1)	A_2 (G_2)	B_2 (H_2)	E_2 (F_2)	V_{CC}	Sense	TEST LIMITS Min.	Max.
1, (2)	1	V_{IH}	V_{IH}	I_{OL1}				V_{CCL}	V_{E1} (V_{F1})		V_{OL}
3, (4)	1				V_{IH}	V_{IH}	I_{OL1}	V_{CCL}	V_{E2} (V_{F2})		V_{OL}
5, (6)	1	V_{IL}		$-I_{OH}$				V_{CCL}	V_{E1} (V_{F1})	V_{OH}	
7, (8)	1		V_{IL}	$-I_{OH}$				V_{CCL}	V_{E1} (V_{F1})	V_{OH}	
9, (10)	1				V_{IL}		$-I_{OH}$	V_{CCL}	V_{E2} (V_{F2})	V_{OH}	
11, (12)	1					V_{IL}	$-I_{OH}$	V_{CCL}	V_{E2} (V_{F2})	V_{OH}	
13, (14)	1	V_R	GND					V_{CCH}	I_{A1} (I_{G1})		I_R
15, (16)	1	GND	V_R					V_{CCH}	I_{B1} (I_{H1})		I_R
17, (18)	1				V_R	GND		V_{CCH}	I_{A1} (I_{A2})		I_R
19, (20)	1				GND	V_R		V_{CCH}	I_{B2} (I_{H2})		I_R
21, (22)	1	V_F	V_R					V_{CCH}	I_{A1} (I_{G1})		$-I_F$
23, (24)	1	V_R	V_F					V_{CCH}	I_{B1} (I_{H1})		$-I_F$
25, (26)	1				V_F	V_R		V_{CCH}	I_{A2} (I_{G2})		$-I_F$
27, (28)	1				V_R	V_F		V_{CCH}	I_{B2} (I_{H2})		$-I_F$
29, (30)	1	V_{IL2}		V_{CEX}				V_{CEX}	I_{E1} (I_{F1})		I_{CEX}
31, (32)	1				V_{IL2}		V_{CEX}	V_{CEX}	I_{E2} (I_{F2})		I_{CEX}
33, (34)	1	GND		GND				V_{CCH}	I_{E1} (I_{F1})	$-I_{SC}$	
35, (36)	1				GND		GND	V_{CCH}	I_{E2} (I_{F2})	$-I_{SC}$	
37, (38)	1	GND		GND				V_{CCH}	I_{E1} (I_{F1})		$-I_{SC}$
39, (40)	1				GND		GND	V_{CCH}	I_{E2} (I_{F2})		$-I_{SC}$
41	1							V_{PD}	I_{VCC}		I_{PDH}
42	1, 2	GND			GND			V_{MAX}	I_{VCC}		I_{MAX}
43, 44		For $t_{pd}+$ and $t_{pd}-$ Conditions and Limits see Page 31.									
45, (46)	1,3	V_F	V_R					V_{CCL}	I_{A1} (I_{G1})		$-I_{F2}$
47, (48)	1,3	V_R	V_F					V_{CCL}	I_{B1} (I_{H1})		$-I_{F2}$
49, (50)	1,3				V_F	V_R		V_{CCL}	I_{A2} (I_{G2})		$-I_{F2}$
51, (52)	1,3				V_R	V_F		V_{CCL}	I_{B2} (I_{H2})		$-I_{F2}$
53, (54)	1,3	V_{IH}	V_{IH}	I_{OL2}				V_{CCH}	V_{E1} (V_{F1})		V_{OL2}
55, (56)	1, 3				V_{IH}	V_{IH}	I_{OL2}	V_{CCH}	V_{E2} (V_{F2})		V_{OL2}
57	1, 4	GND	GND		GND	GND		V_{PD}	I_{VCC}		I_{PDL}

NOTES: 1. Ground pin is grounded for all tests. 2. One input of each gate is grounded.
3. Tests 45/57 apply to full temperature range only. 4. Ground all inputs.

PROPAGATION DELAY

tpd TESTS

tpd TEST CIRCUIT

FIG. 80

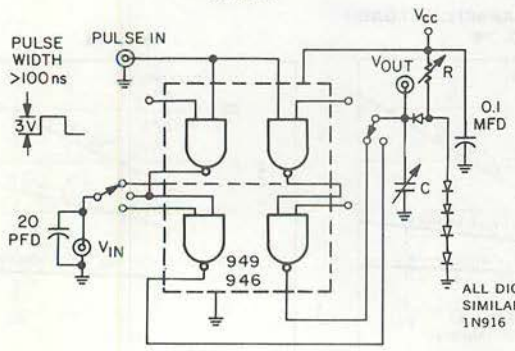


TABLE OF CONDITIONS & LIMITS tpd TESTS

(See Test Circuit.)
(V_{CC} = 5V, T = 25°C)

		R	C	Min.	Max.
$t_{pd}+$	946	3.9 K	30 pf	25 nsec	80 nsec
$t_{pd}-$	946	400 Ω	50 pf	10 nsec	30 nsec
$t_{pd}+$	946	400 Ω	50 pf	15 nsec	40 nsec[1]
$t_{pd}-$	946	3.9 K	20 pf	5 nsec	20 nsec[1]
$t_{pd}+$	949	3.9 K	30 pf	15 nsec	50 nsec
$t_{pd}-$	949	400 Ω	50 pf	10 nsec	30 nsec

NOTE: 1. Correlating limit provided as design information only.

TEST LIMITS

Parameter	Units	FULL TEMPERATURE RANGE						LIMITED TEMPERATURE RANGE					
		−55°C		+25°C		+125°C		0°C		+25°C		+75°C	
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.
V_{OL} (946)	Volts		0.40		0.40		0.45		0.45		0.45		0.5
V_{OL} (949)	Volts		0.40		0.40		0.45		0.50		0.50		0.55
V_{OH} (946)	Volts	2.50		2.60		2.50		2.60		2.60		2.50	
V_{OH} (949)	Volts	3.80		3.80		3.70		4.30		4.30		4.20	
I_R	μA		2.0		2.0		5.0		5.0		5.0		10.0
$-I_F$	mA		1.5		1.5		1.4		1.4		1.4		1.33
I_{CEX}	μA				50.0						100.0		
$-I_{SC}$ (946)	mA	0.61	1.34	0.61	1.34	0.535	1.30	0.61	1.30	0.61	1.30	0.535	1.25
$-I_{SC}$ (949)	mA	2.1	3.7	2.10	3.7	1.86	3.28			1.85	3.68		
I_{PDH} (946)	mA				12.5						16.0		
I_{PDH} (949)	mA				21.8						23.3		
I_{MAX} (946)	mA				11.0						16.0		
I_{MAX} (949)	mA				10.4						11.44		
V_{OL2} (946)	Volts		0.40		0.40		0.40						
V_{OL2} (949)	Volts		0.40		0.40		0.40						
$-I_{F2}$	mA		1.16		1.16		1.08						
I_{PDL} (949)	mA				5.88								

FORCING CONDITIONS

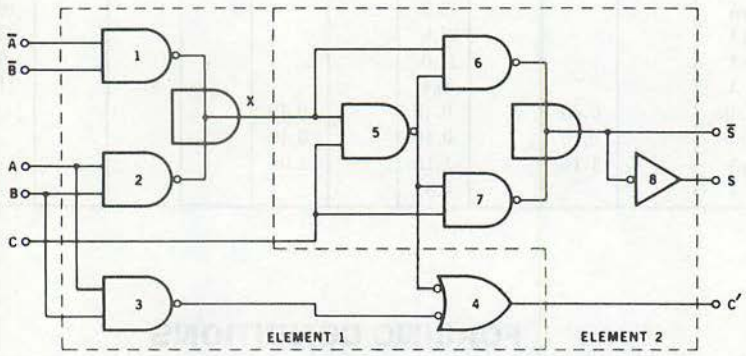
FULL TEMPERATURE RANGE					LIMITED TEMPERATURE RANGE				
Parameter	Units	−55°C	+25°C	+125°C	Parameter	Units	0°C	+25°C	+75°C
V_{MAX}	Volts		8.0		V_{MAX}	Volts		8.0	
V_{PD}	Volts		5.0		V_{PD}	Volts		5.0	
V_{CCH}	Volts	5.5	5.5	5.5	V_{CCH}	Volts	5.0	5.0	5.0
V_{CCL}	Volts	4.5	4.5	4.5	V_{CCL}	Volts	5.0	5.0	5.0
V_R	Volts	4.0	4.0	4.0	V_R	Volts	4.0	4.0	4.0
V_F	Volts	0.4	0.4	0.4	V_F	Volts	0.45	0.45	0.50
V_{IL}	Volts	1.4	1.1	0.8	V_{IL}	Volts	1.2	1.1	0.95
V_{IL2}	Volts		0.0		V_{IL2}	Volts		0.0	
V_{IH}	Volts	2.1	1.9	1.7	V_{IH}	Volts	2.0	1.9	1.8
V_{CEX}	Volts		4.5		V_{CEX}	Volts		5.0	
I_{OL1} 946	mA	12.0	12.0	12.0	I_{OL1} 946	mA	12.0	12.0	11.4
I_{OL1} 949	mA	10.8	10.8	10.8	I_{OL1} 949	mA	10.5	10.5	10.2
$-I_{OH}$ 946	μA	180.0	180.0	180.0	$-I_{OH}$	μA	120.0	120.0	120.0
$-I_{OH}$ 949	mA	.54	.54	.54					
I_{OL2} 946	mA	15.0	15.0	15.0					
I_{OL2} 949	mA	13.5	13.5	13.5					

APPLICATIONS

Most of the advantages in reducing element count and assembly cost by having four 2-Input gates in one package are obvious. Considering the large percentage of occurrences of fan-in 1 and 2 in the typical system, savings of 50% of elements needed to accomplish the fan-in 1 and 2 gating is substantial. However, some logic manipulation using the output "OR"ing capability may lead to yet greater savings. Thus, it is a further advantage of ITT Diode-Transistor Logic that the gates (MIC 930 Dual 4-Input Gate Element and MIC 946 Quad 2-Input Gate Element) may be output "OR"ed with fractional fan-out subtraction and without a separate gate with open collector required.
The example 1 , a 2-element full adder, shows the typical use of the Quad 2-Input Gate in an optimized logic configuration.

DESIGN OF A BINARY FULL ADDER

FIG. 81



The classical Binary Full Adder is often split into two half-adder circuits for economy. Such a mechanization, while slower, significantly reduces the logic circuitry involved. The arrangement given in 1 accomplishes all of the functions required of a full-adder with only two MIC 946 elements and introduces a logic delay of only four gate propagation times. All of the signals required for a "carry lookahead" organization are also present.
The rationale for this mechanization derives from the following factorization of the expressions for the full-adder sum (S) and carry (C). Output carry signals are distinguished from the carry input by a prime mark:

$$S = \overline{A}\overline{B}C + \overline{A}B\overline{C} + A\overline{B}\overline{C} + ABC$$
$$= (\overline{A}B + A\overline{B})\overline{C} + (\overline{A}\overline{B} + AB)C$$

$$C = \overline{A}BC + A\overline{B}C + AB\overline{C} + ABC$$
$$= (\overline{A}B + A\overline{B})C + AB(\overline{C} + C)$$
$$= (\overline{A}B + A\overline{B})C + AB$$

Note also that

$$(\overline{A}B + A\overline{B}) = \overline{A}B + A\overline{B}$$

It is apparent that the sum is the exclusive "OR" of the carry input with the result of the exclusive "OR" of the arguments A and B.
Two different exclusive "OR" circuits are used. In the first, composed of NAND Gates 1 and 2, it is assumed that both true and complement values of the arguments are available. The direct connection of the outputs at point X has logical effect; namely, that of ANDing the NAND outputs together.
Therefore, $\overline{A}B \cdot A\overline{B} = \overline{\overline{A}B + A\overline{B}} = \overline{A}B + A\overline{B}$
The second exclusive "OR", composed of NAND Gates 5, 6, 7, and 8, requires only true inputs, avoiding the need for two inverters at its input.
Both the true and complement sum outputs are obtained by the "wired OR" connection and NAND Gate 8, which is used as an inverter.
The output of NAND Gate 5 is the term $(\overline{A}B + A\overline{B})C$ with the proper polarity for NOR Gate 4.
The remaining term of the carry originates in NAND Gate 3 with the proper polarity for NOR Gate 4. The output polarity of NOR Gate 4 is correct for a cascaded full-adder.

RELIABILITY TESTS

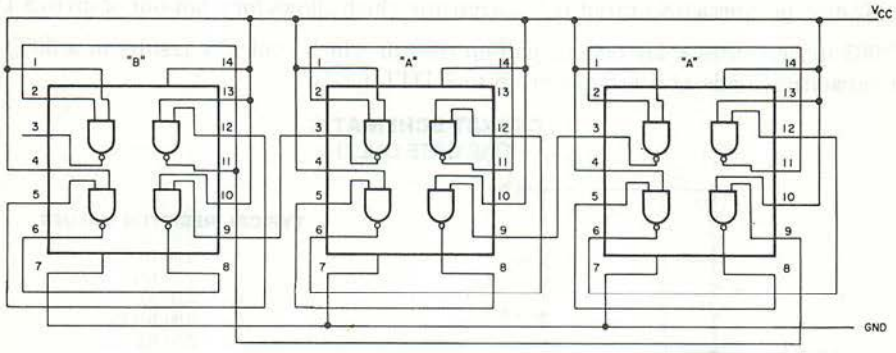
PERFORMED DURING ITT RELIABILITY PROGRAM

MEASUREMENTS OF THE FOLLOWING PARAMETERS ARE RECORDED:

Parameter	Test Sequence Number on Page 30
V_{OL}	#1
V_{OH}	#5
I_R	#13 & #15
I_F	#27 & #28
I_{MAX}	#42

LIFE TEST CIRCUIT

FIG. 82



NOTE: V_{CC} = +5.5 Volts Ambient Temperature = +125°C.
Circuit may have any number of units connected like "A", and one connected like "B". Circuit must contain an odd number of gates connected in series in the ring.

TRIPLE THREE-INPUT GATE MIC 962
FAST TRIPLE THREE-INPUT GATE MIC 963

DESCRIPTION

The MIC 962 and MIC 963 elements are triple three-input NAND/NOR gates.

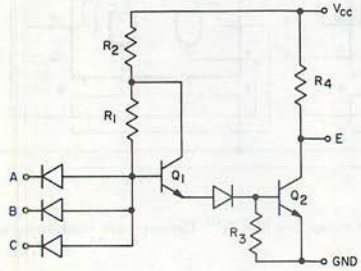
In addition to performing the positive NAND and negative NOR logic functions, the gates can be cross-coupled to form a flip-flop or the outputs can be tied together to perform the "wired OR" function.

These triple three-input gates can also be wired together to perform the "exclusive OR" function.

The MIC 962 incorporates a 6K output pull-up resistor which allows for a fan-out of up to 8 DTL loads.

The MIC 963 incorporates a 2K output pull-up resistor which typically results in a 30% faster rise time with capacitive loads at a fan-out of up to 7 DTL loads.

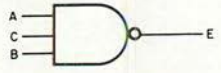
CIRCUIT SCHEMATIC
(ONE GATE ONLY)



TYPICAL RESISTOR VALUES

R_1 = 2.00 KΩ
R_2 = 1.75 KΩ
R_3 = 5.00 KΩ
R_4 = 6.00 KΩ (962)
R_4 = 2.00 KΩ (963)

POSITIVE (NAND) LOGIC



$E = \overline{A \cdot B \cdot C}$

NEGATIVE (NOR) LOGIC

$E = \overline{A + B + C}$

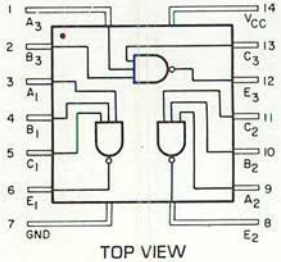
NOTE: Positive Logic is used in this specification.

TRUTH TABLE

A	B	C	E
1	1	1	0
0	1	1	1
1	0	1	1
1	1	0	1
0	0	0	1

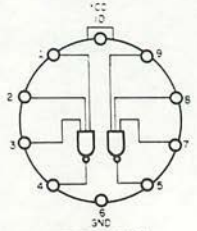
"1" is High Voltage.
"0" is Low Voltage.

FLAT PACK



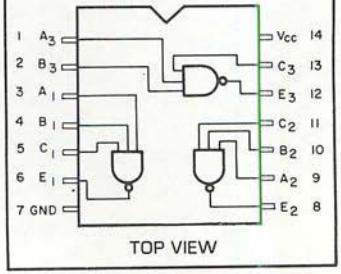
TOP VIEW

SIMILAR TO TO-5



TOP VIEW

DUAL IN-LINE



TOP VIEW

ABSOLUTE MAXIMUM RATINGS[1]

		UNITS
Supply Voltage (V_{CC}), −55°C to +125°C, continuous	−.5 to +8.0	Volts
Supply Voltage (V_{CC}), pulsed, <1 sec	+12	Volts
Output Current, into outputs	30	mA
Input Forward Current	−10	mA
Input Reverse Current	1	mA
Operating Temperature	−55 to +125	°C
Storage Temperature	−65 to +125	°C
Input Voltage Applied to Input	−1.5 to +5.5	Volts
Lead Temp. (soldering, 60 sec.)	300	°C

NOTES: 1. Above which useful life may be impaired.

2. Allow 200°C/Watt θ_{J-A} for TO-5; 300°C/Watt θ_{J-A} for ¼" x ¼" flatpack and dual in-line. Allow 50°C/Watt θ_{J-C} for TO-5; 180°C/Watt θ_{J-C} for ¼" x ¼" flatpack and dual in-line. Heat removal in ¼" x ¼" flatpack is highly dependent upon contact surfaces or air flow and on lead attachment and thermal paths thru leads, as well as number of soldered leads.

SUMMARY OF MIC 962 AND 963 CHARACTERISTICS (25°C)

Parameter		Note	FULL TEMPERATURE RANGE			LIMITED TEMPERATURE RANGE			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
Operating Supply Voltage		1	4.5	5.0	5.5		5.0		Volts
Network Dissipation	962	2		25.5	48.8		25.5	60.0	mW
	963			37.5	81.5		37.5	88.5	
Loading D.C. fan-out	962				8.0			8.0	DTL Unit
	963				7.0			7.0	Load
Output Logic '1' (High)	962		2.6			2.6			Volts
	963		2.6			4.3			
'0' (Low)	962				0.4			0.45	
	963				0.4			0.5	
Input Threshold '1' (High		3	1.9			1.9			Volts
'0' (Low)					1.1			1.1	
Propogation	962	4	25.0		80.0	25.0		80.0	Nano-
Delay Time $t_{pd}+$	963		15.0		50.0	15.0		50.0	Second
	962		10.0		30.0	10.0		30.0	
$t_{pd}-$	963		10.0		30.0	10.0		30.0	
Noise Immunity		5	0.35	>0.5		0.35	>0.5		Volts

NOTES: 1. Exact specification limits for operating temperature range may be obtained by reference to the appropriate test.

2. Power supplied from V_{CC} (5V) during on state fan-out = 0.

3. Input threshold voltage is defined as the minimum (or maximum) voltage at the circuit input to guarantee a low (or high) output.

4. Propogation delay time terms ($t_{pd}+$ and $t_{pd}-$) are described in the t_{pd} test circuit, Page 8.

5. See noise test circuit, Page 7, and Loading Factors, Page 5.

TEST SEQUENCE

Both elements are triplet "NAND" gates; therefore, the test sequences for each are identical. Tests on each side of the triplet are identical; therefore, matching test and pin numbers are shown in parentheses.

Test No.	Notes	FORCING CONDITIONS AT PINS A_1 (A_2,A_3)	B_1 (B_2,B_3)	C_1 (C_2,C_3)	E_1 (E_2,E_3)	V_{CC}	Sense	TEST LIMITS Min.	Max.
1,(2,3)	1	V_{IH}	V_{IH}	V_{IH}	I_{OL1}	V_{CCL}	V_{E1}(V_{E2}, V_{E3})		V_{OL1}
4,(5,6)	1	V_R	GND	GND		V_{CCH}	I_{A1}(I_{A2}, I_{A3})		I_R
7,(8,9)	1	GND	V_R	GND		V_{CCH}	I_{B1}(I_{B2}, I_{B3})		I_R
10,(11,12)	1	GND	GND	V_R		V_{CCH}	I_{C1}(I_{C2}, I_{C3})		I_R
13,(14,15)	1	V_F	V_R	V_R		V_{CCH}	I_{A1}(I_{A2}, I_{A3})		$-I_{F1}$
16,(17,18)	1	V_R	V_F	V_R		V_{CCH}	I_{B1}(I_{B2}, I_{B3})		$-I_{F1}$
19,(20,21)	1	V_R	V_R	V_F		V_{CCH}	I_{C1}(I_{C2}, I_{C3})		$-I_{F1}$
22,(23,24)	1	V_{IL}			$-I_{OH}$	V_{CCL}	V_{E1}(V_{E2}, V_{E3})	V_{OH}	
25,(26,27)	1		V_{IL}		$-I_{OH}$	V_{CCL}	V_{E1}(V_{E2}, V_{E3})	V_{OH}	
28,(29,30)	1			V_{IL}	$-I_{OH}$	V_{CCL}	V_{E1}(V_{E2}, V_{E3})	V_{OH}	
31,(32,33)	1	GND			GND	V_{CCH}	I_{E1}(I_{E2}, I_{E3})	$-I_{SC}$	
34,(35,36)	1	GND			GND	V_{CCH}	I_{E1}(I_{E2}, I_{E3})		$-I_{SC}$
37,(38,39)	1		V_{IL2}		V_{CEX}	V_{CEX}	I_{E1}(I_{E2}, I_{E3})		I_{CEX}
40	1					V_{PD}	I_{VCC}		I_{PDH}
41	1, 2	GND				V_{MAX}	I_{VCC}		I_{MAX}
42 t_{pd}+				t_{pd}+ and t_{pd}− See page 37 for test conditions and limits					
43 t_{pd}−									
44, (45,46)	1	V_F	V_R	V_R	V_{CEX}	V_{CCL}	I_{A1}(I_{A2}, I_{A3})		$-I_{F2}$
47, (48,49)	1	V_R	V_F	V_R		V_{CCL}	I_{B1}(I_{B2}, I_{B3})		$-I_{F2}$
50, (51,52)	1	V_R	V_R	V_F		V_{CCL}	I_{C1}(I_{C2}, I_{C3})		$-I_{F2}$
53, (54,55)	1	V_{IH}	V_{IH}	V_{IH}	I_{OL2}	V_{CCH}	V_{E1}(V_{E2}, V_{E3})		V_{OL2}
56,	1,3,4	GND	GND	GND		V_{PD}	I_{VCC}		I_{PDL}

NOTES: 1. Ground pin is grounded for all tests.
2. One input of all four gates is grounded.
3. Tests 44/56 apply to full temperature range only.
4. Ground all inputs.

FORCING CONDITIONS

FULL TEMPERATURE RANGE					LIMITED TEMPERATURE RANGE				
Parameter	Units	−55°C	+25°C	+125°C	Parameter	Units	0°C	+25°C	+75°C
V_{CCH}	Volts	5.5	5.5	5.5	V_{CCH}	Volts	5.0	5.0	5.0
V_{CCL}	Volts	4.5	4.5	4.5	V_{CCL}	Volts	5.0	5.0	5.0
V_{MAX}	Volts		8.0		V_{MAX}	Volts		8.0	
V_{PD}	Volts		5.0		V_{PD}	Volts		5.0	
V_R	Volts	4.0	4.0	4.0	V_R	Volts	4.0	4.0	4.0
V_F	Volts	0.4	0.4	0.4	V_F	Volts	0.45	0.45	0.5
V_{CEX}	Volts		4.5		V_{CEX}	Volts		5.0	
V_{IL}	Volts	1.4	1.1	0.8	V_{IL}	Volts	1.20	1.10	0.95
V_{IL2}	Volts		0.0		V_{IL2}	Volts		0.0	
V_{IH}	Volts	2.1	1.9	1.7	V_{IH}	Volts	2.0	1.9	1.8
I_{OL1} 962	mA	12.0	12.0	12.0	I_{OL1} 962	mA	12.0	12.0	11.4
I_{OL1} 963	mA	10.8	10.8	10.8	I_{OL1} 963	mA	10.5	10.5	10.2
$-I_{OH}$ 962	µA	180.0	180.0	180.0	$-I_{OH}$	µA	120.0	120.0	120.0
$-I_{OH}$ 963	mA	.54	.54	.54					
I_{OL2} 962	mA	15.0	15.0	15.0					
I_{OL2} 963	mA	13.5	13.5	13.5					

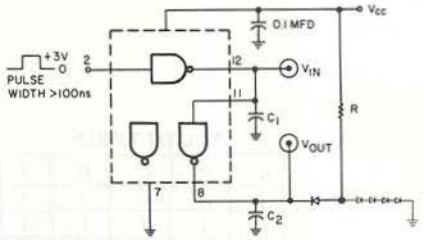
TEST LIMITS

		FULL TEMPERATURE RANGE						LIMITED TEMPERATURE RANGE					
		−55°C		+25°C		+125°C		0°C		+25°C		+75°C	
Parameter	Units	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.
V_{OL1} (962)	Volts		0.4		0.4		0.40		0.45		0.45		0.5
V_{OL1} (963)	Volts		0.4		0.4		0.40		0.5		0.5		0.55
V_{OH} (962)	Volts	2.5		2.6		2.5		2.6		2.6		2.5	
V_{OH} (963)	Volts	2.5		2.6		2.5		4.3		4.3		4.2	
I_R	μA		2.0		2.0		5.0		5.0		5.0		10.0
$-I_{F1}$	mA		1.5		1.5		1.4		1.4		1.4		1.33
$-I_{SC}$ (962)	mA	0.61	1.34	0.61	1.34	0.535	1.30	0.61	1.30	0.61	1.30	0.535	1.25
$-I_{SC}$ (963)	mA	2.10	3.70	2.10	3.70	1.86	3.28			1.85	3.68		
I_{CEX}	μA				50.0						100.0		
I_{PDH} (962)	mA				9.75						12.0		
I_{PDH} (963)	mA				16.3						17.7		
I_{MAX} (962)	mA				8.25						12.0		
I_{MAX} (963)	mA				7.8						8.6		
$-I_{F2}$	mA		1.16		1.16		10.8						
V_{OL2}	Volts		0.4		0.4		0.4						
I_{PDL}	mA				4.41								

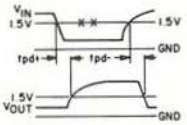
PROPAGATION DELAY

tpd TEST CIRCUIT

FIG. 83



tpd TESTS



t_{pd}− of 962 and 963 elements will be read from input at 1.5V.

All diodes 1N916 or equivalent.

C_1 and C_2 includes probe and jig capacitance.

$V_{Threshold}$= 1.5V at 25°C; at other temperatures $V_{Threshold}$ will be stated.

TABLE OF CONDITIONS & LIMITS tpd TESTS

(See Test Circuit.)

(V_{CC} = 5.0 V, T_A = 25°C)

		R ohms	C_1 pf	C_2 pf	Min. nsec	Max. nsec
t_{pd}+	962	3.9K	20	30	25	80
t_{pd}−	962	400	20	50	10	30
t_{pd}+	963	3.9K	20	30	15	50
t_{pd}−	963	400	20	50	10	30

RELIABILITY TESTS

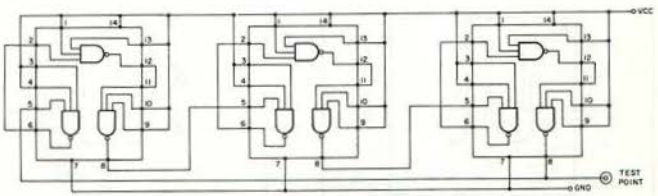
PERFORMED DURING ITT RELIABILITY PROGRAM

MEASUREMENTS OF THE FOLLOWING PARAMETERS ARE RECORDED:

Parameter	Test Sequence Number on Page 36
V_{OL}	#1
V_{OH}	#7, #8, & #9
I_F	#16, #17, & #18
I_R	#22
I_{CEX}	#41

LIFE TEST CIRCUIT

FIG. 84



NOTES: V_{CC} = +5.5 Volts Ambient Temperature = +125°C

The circuit must contain an odd number of gates connected serially in a ring.

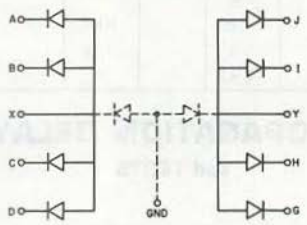
DUAL FOUR-INPUT EXTENDER MIC 933

DESCRIPTION

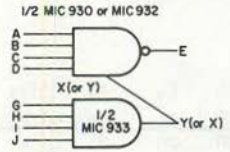
The MIC 933 element is a dual four-input extender. The MIC 933 consists of two independent diode arrays identical in every respect to the input diodes of the DTL gates and buffer elements. It can be used to extend the fan-in capability to more than 20 without adversely affecting the noise immunity or load driving capability of the elements to which they are connected. Good practice dictates that extension interconnection paths be as short as possible to minimize the effects of distributed capacitance on circuit performance. The MIC 933 has a typical input capacitance of 2pf and an output capacitance of 5 pf.

The MIC 933 can extend the fan-in of the MIC 930, 932, 944, and 961 elements.

CIRCUIT SCHEMATIC

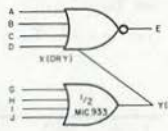


POSITIVE (NAND) LOGIC



POSITIVE LOGIC $E = \overline{ABCDGHIJ}$

NEGATIVE (NOR) LOGIC



NEGATIVE LOGIC $E = \overline{A+B+C+D+G+H+I+J}$

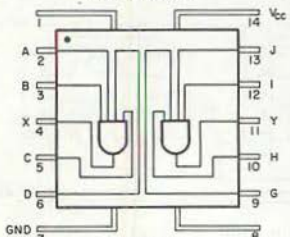
NOTE: Positive logic is used in this specification.

TRUTH TABLE

A	B	C	D	X
G	H	I	J	Y
I	I	I	I	I
O	I	I	I	O
I	O	I	I	O
I	I	O	I	O
I	I	I	O	O
O	O	O	O	O

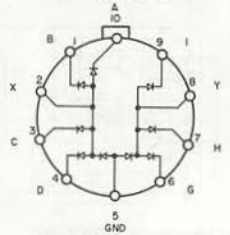
I is High
O is Low

FLAT PACK



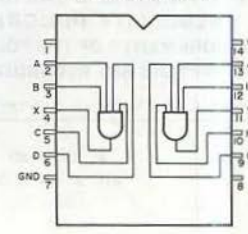
TOP VIEW

SIMILAR TO TO-5



TOP VIEW

DUAL IN-LINE



TOP VIEW

ABSOLUTE MAXIMUM RATINGS[1]

		UNITS
Supply Voltage (V_{CC}), −55°C to + 125°C, continuous	−.5 to +8	Volts
Supply Voltage (V_{CC}), pulsed <1.0 sec	+12	Volts
Input Forward Current, I_F	−10	mA
Input Reverse Current, I_R	1	mA
Operating Temperature Range	−55 to −125	°C
Storage Temperature Range	−65 to −150	°C
Operating Junction Temperature[2]	+175	°C
Input Voltage Applied to Input	−1.5 to +5.5	Volts
Lead Temp. (soldering, 60 sec.)	300	°C

NOTES: 1. Above which useful life may be impaired.

2. Allow 200°C/Watt θ_{J-A} for TO-5; 300°C/Watt θ_{J-A} for ¼" x ¼" flatpack and dual in-line. Allow 50°C/Watt θ_{J-C} for TO-5; 180°C/Watt θ_{J-C} for ¼" x ¼" flatpack and dual in-line. Heat removal in ¼" x ¼" flatpack is highly dependent upon contact surfaces or air flow and on lead attachment and thermal paths thru leads, as well as number of soldered leads.

TEST SEQUENCE

Test No.	Note	Pin A (G)	Pin B (H)	Pin C (I)	Pin D (J)	Pin X (Y)	Sense	Symbol
1,2,3,4, (5,6,7,8)	2,3,4	GND	GND	GND	GND	I_{FD}	$V_X(V_Y)$	V_{FD}
11,(12)	3	V_R	GND	GND	GND	—	$I_A(I_G)$	I_{R1}
13,(14)	3	GND	V_R	GND	GND	—	$I_B(I_H)$	I_{R2}
15,(16)	3	GND	GND	V_R	GND	—	$I_C(I_I)$	I_{R3}
17,(18)	3	GND	GND	GND	V_R	—	$I_D(I_J)$	I_{R4}
19,(20)	3	—	—	—	—	V_R	$I_X(I_Y)$	$5I_R$

NOTES:

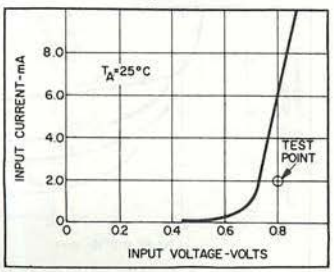
1. Forcing Conditions { V_R = 4.0 volts, I_{FD} = 2.0 mA (0 to +75°C); V_R = 4.0 volts, I_{FD} = 2.0 mA (−55 to +125°C) }
2. The MIC 933 is a dual element. Tests for each side are identical. Matching tests and pin numbers are shown in parenthesis.
3. The ground pin is grounded on all tests.
4. Ground applied individually to one input, each test. Other inputs open.

TEST LIMITS

		FULL TEMPERATURE RANGE						LIMITED TEMPERATURE RANGE					
		−55°C		+25°C		+125°C		0°C		+25°C		+75°C	
Parameter	Units	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.
V_{FD}	Volts	.840	.980	.700	.820	.480	.620	.700	.900	.660	.840	.560	.760
I_R	μA		2.0		2.0		5.0		5.0		5.0		10.0
$5I_R$	μA		10.0		10.0		25.0		25.0		25.0		50.0

FORWARD VOLTAGE VERSUS FORWARD CURRENT +25°C

FIG. 85



TYPICAL CURVES

TO SHOW THE EFFECTS OF EXTENDER PIN CAPACITANCE (RESULTING FROM USE OF MIC 933) ON TIME DELAY OF MIC 930 DUAL GATE AND MIC 932 DUAL BUFFER

FIG. 86

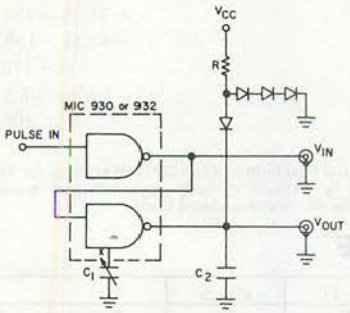


FIG. 87

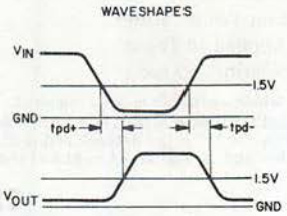


FIG. 88

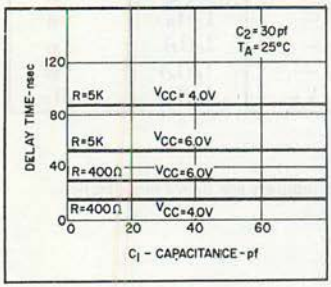


FIG. 89

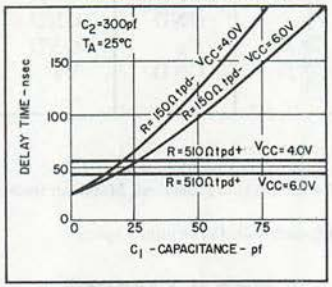
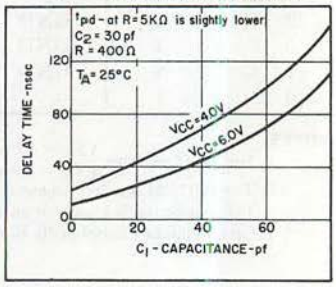


FIG. 90



NOTE:

C_1 represents the summation of the MIC 933 Dual Extender Element output capacitances ($\approx$5 pf per output) and associated board, connector and wiring capacitances.

TO SHOW THE EFFECTS OF EXTENDER PIN CAPACITANCE ON NOISE THRESHOLD OF MIC 930 DUAL GATE

FIG. 91

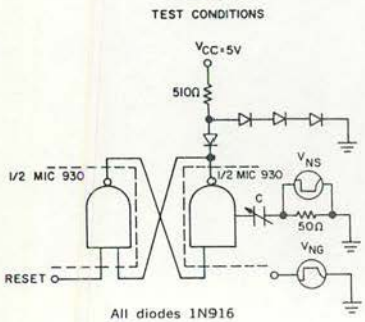


FIG. 92

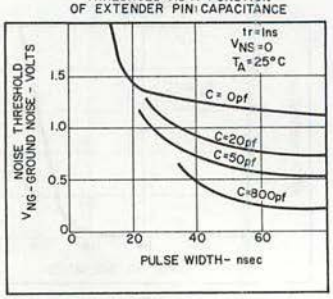
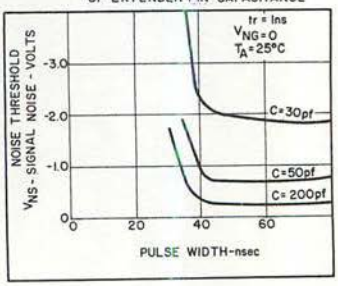


FIG. 93



RELIABILITY TESTS

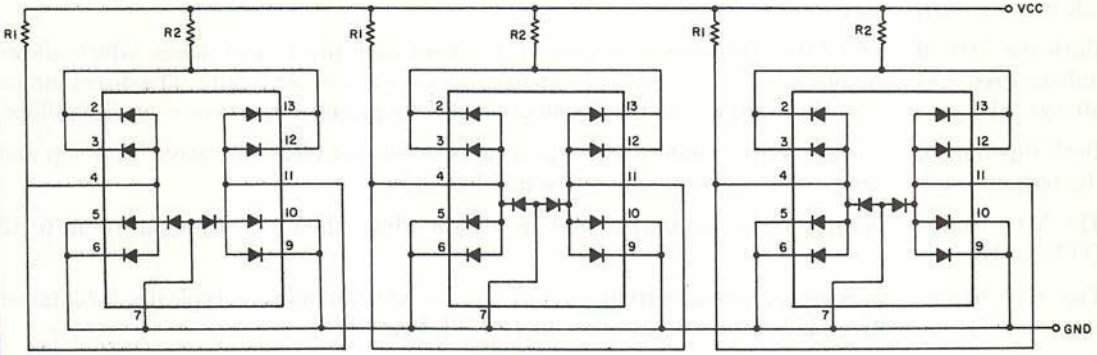
PERFORMED DURING ITT RELIABILITY PROGRAM

MEASUREMENTS OF THE FOLLOWING PARAMETERS ARE RECORDED:

Parameter	Test Sequence Number on Page 39
V_F	#1
V_F	#5
$5I_R$	#19
$5I_R$	#20

LIFE TEST CIRCUIT

FIG. 94



NOTE: V_{CC} = +5.5 Volts Ambient Temperature = +125°C
R_1 = 220Ω, 10%, ½ watt. R_2 = 390Ω, 10%, ½ watt.

CLOCKED FLIP-FLOP MIC 945
CLOCKED FLIP-FLOP MIC 948

DESCRIPTION

The MIC 945 and MIC 948 elements are clocked flip-flops.

Both the MIC 945 and MIC 948 flip-flops operate on the "master-slave" principle. Information enters the "master" flip-flop when trigger clock input voltage is high and transfers to the "slave" flip-flop when trigger clock input voltage goes low. Since operation depends only on voltage levels any sort of waveshape having the proper voltage levels may be used as a trigger signal. (The rise and fall times are irrelevant.)

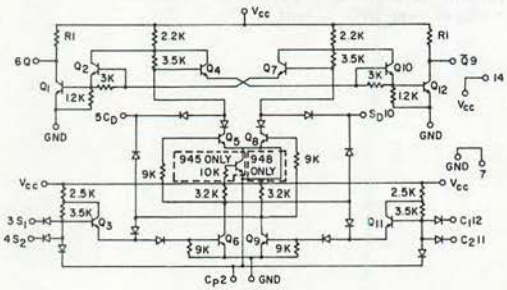
Both the MIC 945 and MIC 948 have an improved direct set and direct clear design which allows unhampered asynchronous entry irrespective of signals applied to any other inputs. The direct inputs always take precedence, thus simplifying the design of arbitrarily preset counters or control flip-flops.

Both flip-flops incorporate output buffers which provide isolation between the "slave" flip-flop and the output load, thereby enhancing immunity to signal line noise.

The MIC 945 incorporates a 6K ohm output pull up resistor which allows for a fan-out of up to 12 DTL loads.

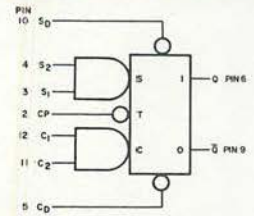
The MIC 948 incorporates a 2K ohm output pull up resistor which allows for typically 30% faster rise times for capacitive loads at a fan-out of up to 11 DTL loads.

CIRCUIT SCHEMATIC



NOTES: Pins 1, 8, 13 not used
945, $R_1 = 6K$
948, $R_1 = 2K$
PIN NUMBERS REFER TO FLAT PACKAGE AND DIP

POSITIVE LOGIC SYMBOLS



NOTES:

1. Pin numbers refer to flat package.
2. Abbreviations used in the body of tables:
   NC = no change, the trigger-pulse has equal effect.
   0 = low, the more negative voltage level.
   1 = high, the more positive voltage level
   (In all cases, unused pins have the same effect as high.)
   Φ = immaterial, either 1 or 0 has no effect on outputs.

SYNCHRONOUS ENTRY

Inputs t_n				Output t_{n+1}
3	4	11	12	6
0	Φ	0	Φ	NC
0	Φ	Φ	0	NC
Φ	0	0	Φ	NC
Φ	0	Φ	0	NC
0	Φ	1	1	0
Φ	0	1	1	0
1	1	0	Φ	1
1	1	Φ	0	1
1	1	1	1	Undetermined

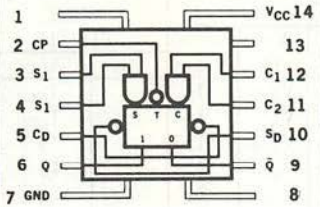
For J-K Mode Operation:
Connect 4 to 9 and 11 to 6

ASYNCHRONOUS ENTRY

Inputs		Outputs	
5	10	6	9
1	1	NC	NC
1	0	1	0
0	1	0	1
0	0	1	1

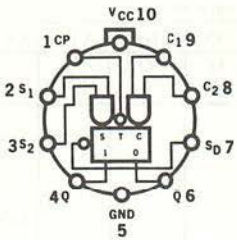
Asynchronous entry is independent of all other inputs and overrides synchronous entry.

FLAT PACK



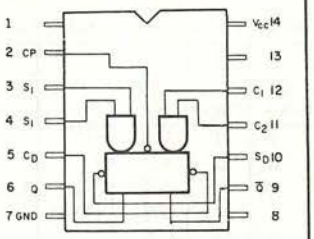
TOP VIEW

SIMILAR TO TO-5



TOP VIEW

DUAL IN-LINE



TOP VIEW

ABSOLUTE MAXIMUM RATINGS[1]

	UNITS
Supply Voltage (V_{CC}), −55°C to +125°C, continuous ..... −0.5 to +8	Volts
Supply Voltage (V_{CC}), pulsed, <1 sec ..... +12	Volts
Output Current, into outputs 30	mA
Input Forward Current ..... −10	mA
Input Reverse Current 1	mA
Operating Temperature ..... −55 to +125	°C
Storage Temperature ..... −65 to +150	°C
Operating Junction Temperature[2] ..... +175	°C
Input Voltage Applied to Input ..... −1.5 to +5.5	V
Lead Temp. (soldering, 60 sec.) 300	°C

NOTES: 1. Above which useful life may be impaired.

2. Allow 200°C/Watt θ_{J-A} for TO-5; 300°C/Watt θ_{J-A} for ¼" x ¼" flatpack and dual in-line. Allow 50°C/Watt θ_{J-C} for TO-5; 180°C/Watt θ_{J-C} for ¼" x ¼" flatpack and dual in-line. Heat removal in ¼" x ¼" flatpack is highly dependent upon contact surfaces or air flow and on lead attachment and thermal paths thru leads, as well as number of soldered leads.

SUMMARY OF MIC 945 AND 948 CHARACTERISTICS (25°C)

Network Parameter		Note	FULL TEMPERATURE RANGE Min.	Typ.	Max.	LIMITED TEMPERATURE RANGE Min.	Typ.	Max.	Unit
Operating Supply Voltage		1	4.5	5.0	5.5		5.0		Volts
Network Dissipation	945	2			70.0			75.0	mW
	948				81.0			87.5	
Loading D.C. Fanout	945				10.0			12.0	DTL Unit
	948				9.0			11.0	Load
Output Logic '1' (High)	945		2.5			3.1			Volts
	948		2.5			4.3			
'O' (Low)	945				0.4			0.45	
	948				0.4			0.45	
Input Threshold '1' (High)		3	1.9			1.9			Volts
'O' (Low)					1.1			1.1	
Propagation $t_{pd}+$	945	4	35.0		75.0	35.0		75.0	Nano-
Delay Time	948		30.0		65.0	30.0		65.0	Second
$t_{pd}-$	945		30.0		75.0	30.0		75.0	
	948		30.0		75.0	30.0		75.0	
Noise Immunity			0.35	>0.5		0.35	>0.5		Volts

NOTES: 1. Exact specification limits for operating temperature range may be obtained by reference to the appropriate test.
2. Power supplied from V_{CC}(5V) during "ON" state, Fanout = 0.
3. Input threshold voltage is defined as the minimum (or maximum) voltage at the circuit input to guarantee a low (or high) output.
4. Propagation delay time terms ($t_{pd}+$ and $t_{pd}-$) are described in the t_{pd} test circuit, Page 46

TEST SEQUENCE

NOTE: Pin numbers refer to flat package and dual in line package.

Test No.	Notes	C_P Pin 2	S_1 3	FORCING CONDITIONS AT PINS S_2 4	C_D 5	Q 6	$\overline{Q}$ 9	S_D 10	C_2 11	C_1 12	V_{CC} 14	Sense	TEST LIMITS Min.	Max.
1	1	V_R	GND	GND	GND						V_R	I_2		I_{RCP}
2	1	V_R						GND	GND	GND	V_R	I_2		I_{RCP}
3	1	GND	V_R	GND							V_{CCH}	I_3		I_R
4	1	GND	GND	V_R							V_{CCH}	I_4		I_R
5	1	GND							GND	V_R	V_{CCH}	I_{12}		I_R
6	1	GND							V_R	GND	V_{CCH}	I_{11}		I_R
7	1	CP	GND	GND	V_R			V_{CCH}			V_{CCH}	I_5		I_R
8	1	CP			V_{CCH}			V_R	GND	GND	V_{CCH}	I_{10}		I_R
9	1				GND	V_{CEX}		GND			V_{CEX}	I_6		I_{CEX}
10	1				GND		V_{CEX}	GND			V_{CEX}	I_9		I_{CEX}
11	1	GND	GND	GND	GND			GND	GND	GND	V_{MAX}	I_{14}		I_{MAX}
12	1	CP	GND	GND	V_{CCL}	$-I_{OH}$		V_{ILS}			V_{CCL}	V_6	V_{OH}	
13	1	CP			V_{ILS}		$-I_{OH}$	V_{CCL}	GND	GND	V_{CCL}	V_9	V_{OH}	
14	1, 2	CP	V_{IL}		V_{CCL}	I_{OL1}		V_{IH}	V_{IH}	V_{IH}	V_{CCL}	V_6		V_{OL1}
15	1, 2	CP		V_{IL}	V_{CCH}	I_{OL2}		V_{IH}	V_{IH}	V_{IH}	V_{CCH}	V_6		V_{OL2}
16	1, 2	CP	V_{IH}	V_{IH}	V_{IH}		I_{OL1}	V_{CCL}	V_{IL}		V_{CCL}	V_9		V_{OL1}
17	1, 2	CP	V_{IH}	V_{IH}	V_{IH}		I_{OL2}	V_{CCH}		V_{IL}	V_{CCH}	V_9		V_{OL2}
18	1	V_R	V_F	V_R							V_{CCH}	$-I_3$		$-2/3\ I_{F1}$
19	1	V_R	V_R	V_F							V_{CCH}	$-I_4$		$-2/3\ I_{F1}$
20	1	V_R							V_R	V_F	V_{CCH}	$-I_{12}$		$-2/3\ I_{F1}$
21	1	V_R							V_F	V_R	V_{CCH}	$-I_{11}$		$-2/3\ I_{F1}$
22	1	GND			V_F			GND			V_{CCH}	$-I_5$		$-I_{FSI1}$
23	1	GND			GND			V_F			V_{CCH}	$-I_{10}$		$-I_{FSI1}$
24	1				V_F				GND	GND	V_{CCH}	$-I_5$		$-I_{FS}$
25	1		GND	GND				V_F			V_{CCH}	$-I_{10}$		$-I_{FS}$
26	1	V_F			V_{ILS}						V_{CCH}	$-I_2$		$-I_{FCP1}$
27	1	V_F						V_{ILS}			V_{CCH}	$-I_2$		$-I_{FCP1}$
28	1	CP			V_{CCH}	GND		V_{CCH}	GND	GND	V_{CCH}	$-I_6$	$-I_{SC}$	
29	1	CP			V_{CCH}	GND		V_{CCH}	GND	GND	V_{CCH}	$-I_6$		$-I_{SC}$
30	1	CP	GND	GND	V_{CCH}		GND	V_{CCH}			V_{CCH}	$-I_9$	$-I_{SC}$	
31	1	CP	GND	GND	V_{CCH}		GND	V_{CCH}			V_{CCH}	$-I_9$		$-I_{SC}$
32	1										V_{PD}	I_{14}		I_{PDH}
33	$t_{pd}+$, 945	See Page 45 for Test Limits and Conditions.												
34	$t_{pd}-$, 945	See Page 45 for Test Limits and Conditions.												
35	$t_{pd}+$, 948	See Page 45 for Test Limits and Conditions.												
36	$t_{pd}-$, 948	See Page 45 for Test Limits and Conditions.												
37	1,3	V_R	V_F	V_R							V_{CCL}	$-I_3$		$-2/3\ I_{F2}$
38	1,3	V_R	V_R	V_F							V_{CCL}	$-I_4$		$-2/3\ I_{F2}$
39	1,3	V_R							V_R	V_F	V_{CCL}	$-I_{12}$		$-2/3\ I_{F2}$
40	1,3	V_R							V_F	V_R	V_{CCL}	$-I_{11}$		$-2/3\ I_{F2}$
41	1,3	GND			V_F			GND			V_{CCL}	$-I_5$		$-I_{FSI2}$
42	1,3	GND			GND			V_F			V_{CCL}	$-I_{10}$		$-I_{FSI2}$
43	1,3	V_F			V_{ILS}						V_{CCL}	$-I_2$		$-I_{FCP2}$
44	1,3	V_F						V_{ILS}			V_{CCL}	$-I_2$		$-I_{FCP2}$

NOTES: 1. Ground pin is grounded.
2. Delay application of I_{OL} current source until after completion of clock pulse. Alternatively clamp current source compliance voltage below V_{CEX}.
3. Tests 37/44 apply to full temperature range only.

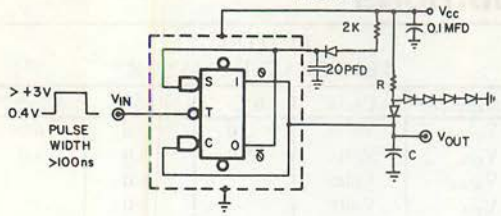
FORCING CONDITIONS

FULL -TEMPERATURE RANGE					LIMITED TEMPERATURE RANGE				
Parameter	Units	−55°C	+25°C	+125°C	Parameter	Units	0°C	+25°C	+75°C
V_{CCH}	Volts	5.5	5.5	5.5	V_{CCH}	Volts	5.0	5.0	5.0
V_{CCL}	Volts	4.5	4.5	4.5	V_{CCL}	Volts	5.0	5.0	5.0
V_{MAX}	Volts		8.0		V_{MAX}	Volts		8.0	
V_{PD}	Volts		5.0		V_{PD}	Volts		5.0	
V_R	Volts	4.0	4.0	4.0	V_R	Volts	4.0	4.0	4.0
V_F	Volts	0.4	0.4	0.4	V_F	Volts	0.45	0.45	0.5
V_{CEX}	Volts		5.5		V_{CEX}	Volts		4.5	
V_{IL}	Volts	1.4	1.1	0.8	V_{IL}	Volts	1.2	1.1	0.95
V_{ILS}	Volts	1.4	1.1	0.8	V_{ILS}	Volts	1.2	1.1	0.95
V_{IH}	Volts	2.1	1.9	1.7	V_{IH}	Volts	2.0	1.9	1.8
I_{OL1} 945	mA	12.0	12.0	12.0	I_{OL1} 945	mA	16.8	16.8	16.0
I_{OL1} 948	mA	13.0	13.0	13.0	I_{OL1} 948	mA	15.4	15.4	14.6
I_{OL2} 945	mA	15.0	15.0	15.0	I_{OL2} 945	mA	16.8	16.8	16.0
I_{OL2} 948	mA	13.6	13.6	13.6	I_{OL2} 948	mA	15.4	15.4	14.6
$-I_{OH}$ 945	μA	180.0	180.0	180.0	$-I_{OH}$	μA	120.0	120.0	120.0
$-I_{OH}$ 948	μA	540.0	540.0	540.0					

TEST LIMITS

		FULL TEMPERATURE RANGE						LIMITED TEMPERATURE RANGE					
		−55°C		+25°C		+125°C		0°C		+25°C		+75°C	
Parameter	Units	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.
V_{OL1}	Volts		0.4		0.4		0.4		0.45		0.45		0.5
V_{OL2} 945	Volts		0.4		0.4		0.4		0.45		0.45		0.45
V_{OL2} 948	Volts		0.4		0.4		0.4		0.45		0.45		0.5
V_{OH} 945	Volts	2.5		2.5		2.5		2.6		2.6		2.5	
V_{OH} 948	Volts	2.5		2.5		2.5		4.3		4.3		4.2	
I_{RCP}	μA		10.0		10.0		20.0		20.0		20.0		30.0
I_R	μA		2.0		2.0		5.0		5.0		5.0		10.0
I_{CEX}	μA				50.0						100.0		
I_{MAX} 945 Flat Pack	mA				16.0						17.0		
I_{MAX} 948 Flat Pack	mA				16.0						17.5		
I_{MAX} 945 TO-5	mA				20.0						21.0		
I_{MAX} 948 TO-5	mA				23.0						25.0		
$-2/3\ I_{F1}$	mA		.98		.98		.92		0.95		0.95		0.9
$-I_{FSI1}$	mA		2.93		2.93		2.57		2.8		2.8		2.66
$-I_{FS}$	mA		2.4		2.4		2.1		2.1		2.1		2.0
$-I_{FCP1}$ 945	mA		2.93		2.93		2.57		2.8		2.8		2.66
$-I_{FCP1}$ 948	mA		2.35		2.35		2.03		2.24		2.24		2.13
$-I_{SC}$ 945	mA	0.7	1.33	0.7	1.33	0.625	1.3	0.59	1.41	0.59	1.41	0.55	1.38
$-I_{SC}$ 948	mA	2.1	3.96	2.1	3.96	1.86	3.54	1.77	4.2	1.77	4.2	1.6	4.0
I_{PDH} 945					14.0						15.0		
I_{PDH} 948					16.2						17.5		
$-2/3\ I_{F2}$	mA		.76		.76		.72						
$-I_{FSI2}$	mA		2.26		2.26		2.20						
$-I_{FCP2}$ 945	mA		2.26		2.26		2.02						
$-I_{FCP2}$ 948	mA		1.83		1.83		1.59						

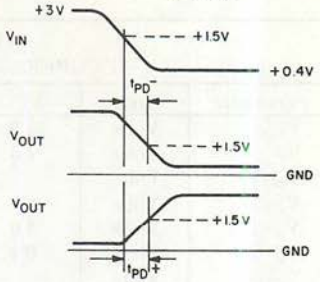
FIG. 95



All diodes 1N916

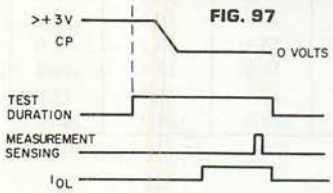
All capacitances include wiring and probe capacitances.

FIG. 96



PROPAGATION DELAY CONDITIONS AND LIMITS

FIG. 97



			TEST CONDITIONS				LIMITS	
Test No.	Device	Test	R Ohms	C Picofarad	T °C	V_{cc} Volts	Min. Nanosecond	Max. Nanosecond
33	945	$t_{pd}+$	2.0K	30	+25	5.0	35	75
34	945	$t_{pd}-$	330	50	+25	5.0	30	75
35	948	$t_{pd}+$	2.0K	30	+25	5.0	30	65
36	948	$t_{pd}-$	330	50	+25	5.0	30	75

ELECTRICAL CHARACTERISTICS

FIG. 98
TYPICAL POWER DISSIPATION VS. Vcc

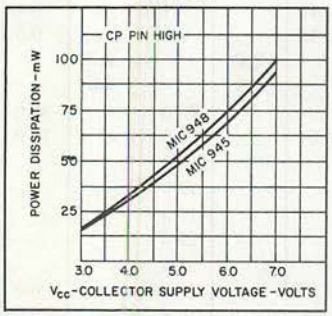


FIG. 99
TYPICAL Tpd VS. CAPACITANCE*

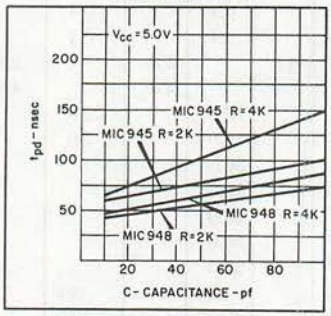


FIG. 100
TYPICAL Tpd VS. CAPACITANCE*

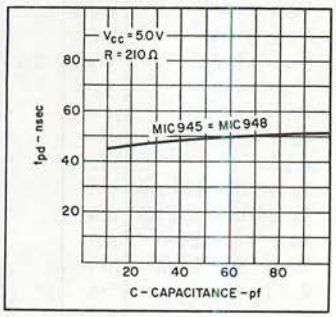


FIG. 101
TYPICAL MAXIMUM BINARY COUNTING RATE VS. CAPACITY

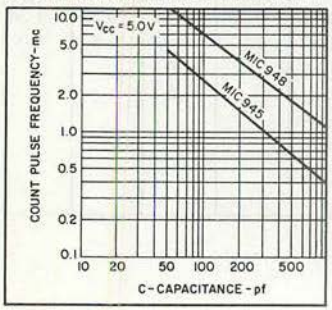
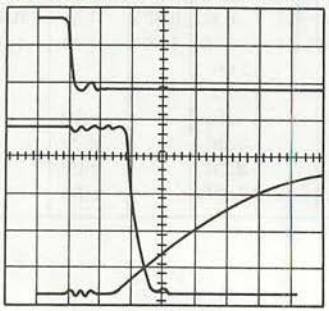


FIG. 102
948 DIVIDE BY TWO WAVEFORM



MIC 948 as a binary counter.

Upper Trace: Input, 2 volts per division.

Lower Traces: Outputs, 1 volt per division.

Falling output loaded by 50 pf and 330Ω to V_{cc}.

Rising output loaded by 50 pf.
25 nsec per division.

V_{cc} = 5V.

*SEE TEST CIRCUIT.

RELIABILITY TESTS

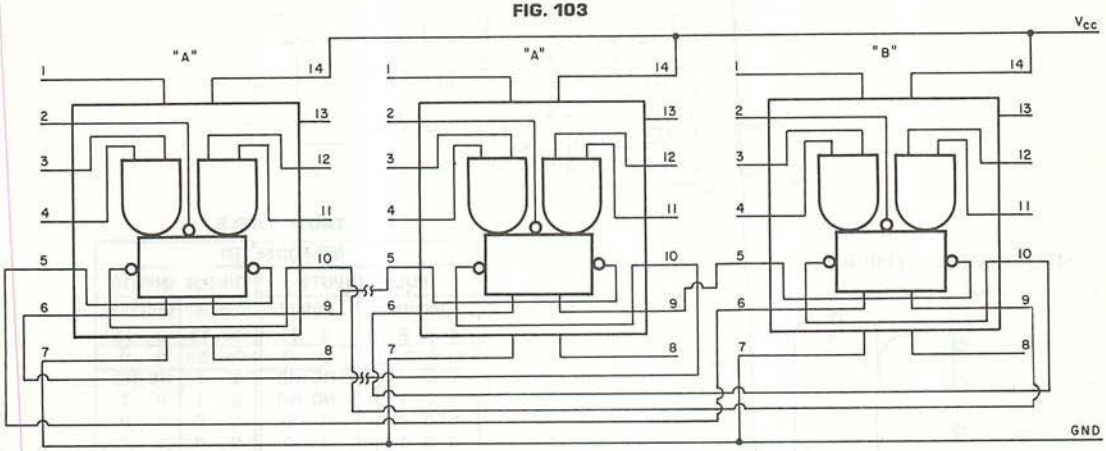
PERFORMED DURING ITT RELIABILITY PROGRAM

MEASUREMENTS OF THE FOLLOWING PARAMETERS ARE RECORDED:

Parameter	Test Sequence Number on Page 44
I_{RCP}	#1
I_R	#4 & #5
V_{OH}	#13
V_{OL}	#14
$-2/3I_F$	#18 & #20
I_{PDH}	#32

LIFE TEST CIRCUIT

FIG. 103



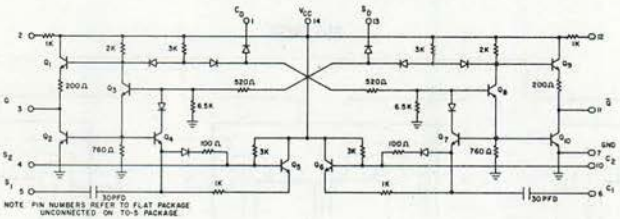
NOTE:
V_{CC}= +5.5 Volts, Ambient Temperature= +125° C
Circuit may have an odd number of units connected like "A", with one connected like "B".

PULSE-TRIGGERED BINARY FLIP-FLOP MIC 950

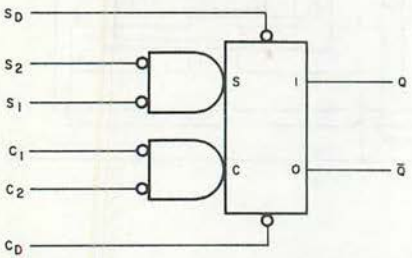
DESCRIPTION

The MIC 950 element is a pulse-triggered, high-speed gated flip-flop and can be used either as an R-S or J-K flip-flop. It will operate in a binary counter application in excess of 20 MHz over the full temperature range and it dissipates typically less than 30 milliwatts. The pulse-triggered set and clear inputs are capacitively coupled while the corresponding steering inputs are directly coupled. The direct set and clear inputs which respond to voltage levels take precedence over the pulse triggered inputs, thus simplifying the design of arbitrarily preset counters or control flip-flops.

CIRCUIT SCHEMATIC



POSITIVE LOGIC SYMBOLS



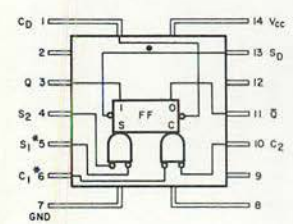
TRUTH TABLE

RESPONSE TO										
PULSE INPUTS							DIRECT INPUTS			
Inputs				Outputs			Inputs		Outputs	
4	5	6	10	3	11		1	13	3	11
S_2	S_1	C_1	C_2	Q	$\bar{Q}$		C_D	S_D	Q	$\bar{Q}$
1	Φ	1	Φ	NC	NC		1	1	NC	NC
Φ	1	Φ	1	NC	NC		0	1	0	1
0	0	Φ	1	1	0		1	0	1	0
0	0	1	Φ	1	0		0	0	1	1
1	Φ	0	0	0	1					
Φ	1	0	0	0	1					
0	0	0	0	Ambiguous						

NOTES: 1. Pin numbers refer to flat package.

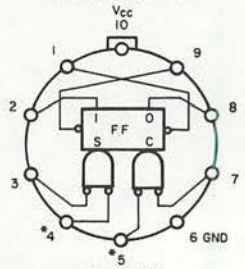
2. Abbreviations used in the body of tables:
   0 = low, the more negative voltage level.
   1 = high, the more positive voltage level (In all cases, unused pins have the same effect as high.)
   Φ = immaterial, either 1 or 0 has equal effect.
   NC = no change, the trigger-pulse has no effect on outputs.
3. 1 or 0 for pins 5 and 6 represent voltage transitions to the level indicated rather than the levels themselves.
4. The tables assume independent use of pulsed inputs and direct inputs. Otherwise, direct inputs will predominate.

FLAT PACK



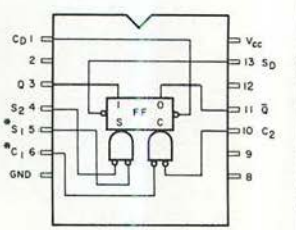
TOP VIEW
*These inputs are capacitively coupled.

SIMILAR TO TO-5



TOP VIEW
*These inputs are capacitively coupled.

DUAL IN-LINE



TOP VIEW
*These inputs are capacitively coupled.

ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage (V_{CC}), −55°C to +125°C, Continuous	−.5 to +8	Volts
Supply Voltage (V_{CC}), pulsed, <1.0 sec.	+12	Volts
Output Current, into Outputs, Continuous	50	mA
Output Current, into Outputs, pulsed, <30 milliseconds	100	mA
Input Forward Current, Pins 1, 4, 10, 13 (flat package)	−10	mA
Input Reverse Current	5.0	mA
Input Voltage, Pins 5, 6 (flat package)	−1.0 to +8.0	Volts
Operating Ambient Temperature	−55 to +125	°C
Storage Temperature	−65 to +150	°C
Operating Junction Temperature[2]	+175	°C
Input Voltage Applied to Input	−1.5 to +5.5	V
Lead Temp. (soldering, 60 sec.)	300	°C

NOTES: 1. Above which useful life may be impaired.

2. Allow 200°C/Watt θ_{J-A} for TO-5; 300°C/Watt θ_{J-A} for ¼" x ¼" flatpack and dual in-line. Allow 50°C/Watt θ_{J-C} for TO-5; 180°C/Watt θ_{J-C} for ¼" x ¼" flatpack and dual in-line. Heat removal in ¼" x ¼" flatpack is highly dependent upon contact surfaces or air flow and on lead attachment and thermal paths thru leads, as well as number of soldered leads.

SUMMARY OF MIC 950 CHARACTERISTICS (25° C)

Network Parameter		Note	MILITARY Min.	MILITARY Typ.	MILITARY Max.	INDUSTRIAL Min.	INDUSTRIAL Typ.	INDUSTRIAL Max.	Unit
Operating Supply Voltage		1	4.5	5.0	5.5		5.0		Volts
Network Dissipation		2			43.5			46.5	mW
Loading D.C. Fanout					8.0			10.0	DTL Unit Load
Output Logic	'1' (High)		2.6			2.8			Volts
	'0' (Low)				0.4			0.45	
Input D.C. Threshold	'1' (High)	3	1.9			1.9			Volts
	'0' (Low)				0.8			0.78	
Propagation Delay Time	$t_{pd}+$	4			30.0			35.0	Nano-Second
	$t_{pd}-$				30.0			35.0	

NOTES: 1. Exact specification limits for operating temperature range may be obtained by reference to the appropriate test.

2. Power supplied from V_{CC} (5V) fanout = 0.

3. Input threshold voltage is defined as the minimum (or maximum) voltage at the ciruit input to guarantee a low (or high) output.

4. Propagation delay time terms ($t_{pd}+$ and $t_{pd}-$) are described in the t_{PD} test circuit, Page 10.

FREQUENCY CHARACTERISTICS

FIG. 104

TYPICAL FREQUENCY OF OPERATION VS. LOADING CAPACITANCE

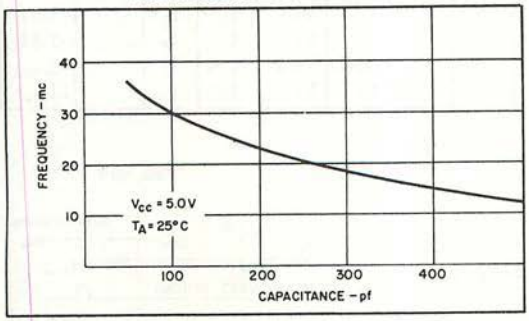
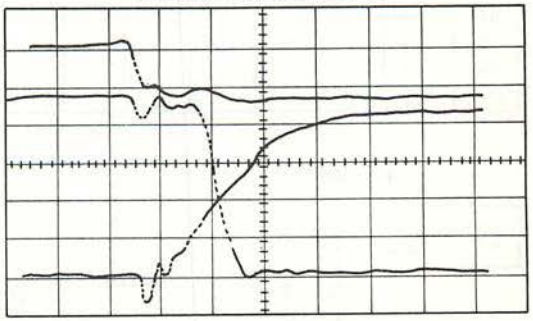


FIG. 105

MIC 950 – DIVIDING BY 2

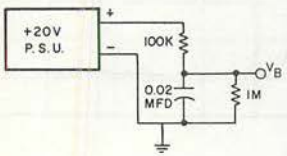


10 nsec/division
25°C Vcc = 5.0 V
UPPER TRACE – Input to CP (2 volts/division)
POSITIVE GOING TRACE – Output Going High (1 volt/division)
NEGATIVE GOING TRACE – Output Going Low (1 volt/division)
20 pf each output

TEST SEQUENCE

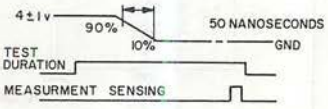
Test No.	Notes	FORCING CONDITIONS AT PINS 1	2	3	4	5	6	10	11	12	13	14	TO5	DIP	TEST LIMITS	
		1		2	3	4	5	7	8		9	10	Sense	Sense		
		C_D		Q	S_2	S_1	C_1	C_2	$\overline{Q}$		S_D	V_{CC}			Min.	Max.
1	1, 2				GND	V_B						V_{CCH}	V_4	V_5	2V	
2	1				GND	V_{MAX}						V_{CCH}	I_4	I_5		I_R
3	1, 2						V_B	GND				V_{CCH}	V_5	V_6	2V	
4	1						V_{MAX}	GND				V_{CCH}	I_5	I_6		I_R
5	1, 3	V_R			V_{CCH}		CP	GND				V_{CCH}	I_1	I_1		I_R
6	1, 3				GND	CP		V_{CCH}			V_R	V_{CCH}	I_9	I_{13}		I_R
7	1			V_{CEX}							GND	V_{CEX}	I_2	I_3		I_{CEX}
8	1	GND							V_{CEX}			V_{CEX}	I_8	I_{11}		I_{CEX}
9	1											V_{CCH}	V_3	V_4	V_L	
10	1											V_{CCH}	V_7	V_{10}	V_L	
11	1				GND			GND				V_{MAX}	I_{10}	I_{14}		I_{MAX}
12	1				GND							V_{PD}	I_{10}	I_{14}		I_{PD}
13	1	GND		I_{OL1}	GND						V_{IHS}	V_{CCL}	V_2	V_3		V_{OL1}
14	1	GND		I_{OL2}								V_{CCH}	V_2	V_3		V_{OL2}
15	1	V_{IHS}						GND	I_{OL1}		GND	V_{CCL}	V_8	V_{11}		V_{OL1}
16	1								I_{OL2}		GND	V_{CCH}	V_8	V_{11}		V_{OL2}
17	1, 3			$-I_{OH}$		CP	CP	GND			V_{ILS}	V_{CCL}	V_2	V_3	V_{OH}	
18	1, 3	V_{ILS}			GND	CP	CP		$-I_{OH}$			V_{CCL}	V_8	V_{11}	V_{OH}	
19	1				V_F							V_{CCH}	I_3	I_4		$-1.5I_{F_1}$
20	1							V_F				V_{CCH}	I_7	I_{10}		$-1.5I_{F_1}$
21	1	V_F									GND	V_{CCH}	I_1	I_1		$-I_{FS1}$
22	1	GND									V_F	V_{CCH}	I_9	I_{13}		$-I_{FS1}$
23	1			GND							GND	V_{CCH}	I_2	I_3	$-I_{SC}$	
24	1			GND							GND	V_{CCH}	I_2	I_3		$-I_{SC}$
25	1	GND							GND			V_{CCH}	I_8	I_{11}	$-I_{SC}$	
26	1	GND							GND			V_{CCH}	I_8	I_{11}		$-I_{SC}$
27	1		GND									V_{CCH}		I_2	I_{1K}	
28	1		GND									V_{CCH}		I_2		I_{1K}
29	1									GND		V_{CCH}		I_{12}	I_{1K}	
30	1									GND		V_{CCH}		I_{12}		I_{1K}
31	$t_{pd}+$	See Page 52 for Test Limits and Conditions.														
32	$t_{pd}-$	See Page 52 for Test Limits and Conditions.														
33	20MHZ	See Page 52 for Test Circuit.														
34	1, 4				V_F							V_{CCL}	I_3	I_4		$-1.5I_{F_2}$
35	1, 4							V_F				V_{CCL}	I_7	I_{10}		$-1.5I_{F_2}$
36	1, 4	V_F									GND	V_{CCL}	I_1	I_1		$-I_{FS2}$
37	1, 4	GND									V_F	V_{CCL}	I_9	I_{13}		$-I_{FS2}$

FIG. 106



NOTES:
1. GROUND PIN IS GROUNDED FOR ALL TESTS.
2. V_B FOR TESTS 1 & 3.
3. CLOCK PULSE FOR TESTS 5,6,17, & 18
4. 34/37 APPLY TO FULL TEMPERATURE RANGE.

FIG. 107



FORCING CONDITIONS

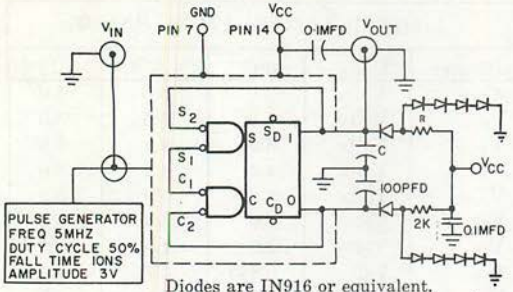
FULL TEMPERATURE RANGE					LIMITED TEMPERATURE RANGE				
Parameter	Units	−55°C	+25°C	+125°C	Parameter	Units	0°C	+25°C	+75°C
V_{CCH}	Volts	5.5	5.5	5.5	V_{CCH}	Volts	5.0	5.0	5.0
V_{CCL}	Volts	4.5	4.5	4.5	V_{CCL}	Volts	5.0	5.0	5.0
V_{MAX}	Volts	8.0	8.0	8.0	V_{MAX}	Volts	8.0	8.0	8.0
V_R	Volts	4.0	4.0	4.0	V_R	Volts	4.0	4.0	4.0
V_{CEX}	Volts	5.0	5.0	5.0	V_{CEX}	Volts	5.0	5.0	5.0
V_{PD}	Volts	5.0	5.0	5.0	V_{PD}	Volts	5.0	5.0	5.0
V_{IHS}	Volts	2.1	1.9	1.7	V_{IHS}	Volts	2.0	1.9	1.8
V_{ILS}	Volts	0.95	0.8	0.605	V_{ILS}	Volts	0.883	0.78	0.73
V_F	Volts	0.4	0.4	0.4	V_F	Volts	.45	.45	.5
I_{OL1}	mA	12.0	12.0	12.0	I_{OL1}	mA	14.0	14.0	13.3
I_{OL2}	mA	15.0	15.0	15.0	I_{OL2}	mA	14.0	14.0	14.0
$-I_{OH}$	mA	1.5	1.5	1.5	$-I_{OH}$	mA	1.5	1.5	1.5

TEST LIMITS

		FULL TEMPERATURE RANGE						LIMITED TEMPERATURE RANGE					
		−55°C		+25°C		+125°C		0°C		+25°C		+75°C	
Parameter	Units	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.
V_{OL1}	Volts		0.4		0.4		0.4		0.45		0.45		0.5
V_{OL2}	Volts		0.4		0.4		0.4		0.45		0.45		0.5
V_L	Volts	5.0		5.0		5.0		4.0		4.0		4.0	
V_{OH}	Volts	2.5		2.6		2.5		2.7		2.8		2.7	
I_R	μA		2.0		2.0		5.0		5.0		5.0		10.0
I_{CEX}	μA		50.0		50.0		100.0		100.0		100.0		100.0
I_{MAX}	mA		18.4		18.4		18.4		19.6		19.6		19.6
$-1.5\ I_{F1}$	mA		2.22		2.22		2.09		2.1		2.1		2.0
$-I_{FS1}$	mA		1.64		1.64		1.46		1.6		1.6		1.52
$-I_{SC}$	mA	12.6	27.0	15.7	27.0	14.0	26.0	13.7	29.3	13.7	29.3	12.6	29.3
$-I_{IK}$	mA	4.05			7.35	4.22	7.35	3.65	7.9	3.7	7.9	3.4	7.9
I_{PD}	mA		8.7		8.7		8.7		9.3		9.3		9.3
$-1.5\ I_{F2}$	mA		1.83		1.83		1.71						
$-I_{FS2}$	mA		1.2		1.24		1.14						

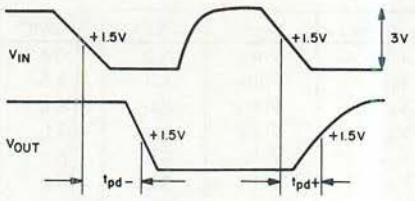
MIC 950 PROPAGATION DELAY TEST CIRCUIT AND LIMITS

FIG. 108



Diodes are IN916 or equivalent.
Capacitances include wiring and probe capacitances.

FIG. 109

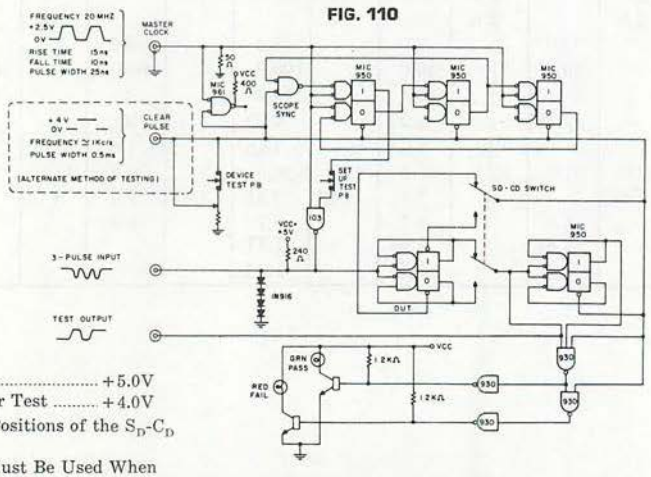


TEST CONDITIONS							FULL TEMPERATURE RANGE		LIMITED TEMPERATURE RANGE	
Test No.	Device	Test	R Ohms	C Picofarad	T °C	V_{CC} Volts	Min. Nanoseconds	Max.	Min. Nanoseconds	Max.
31	950	$t_{pd}+$	3.9K	100	+25°C	5.0		30		35
32	950	$t_{pd}-$	390	100	+25°C	5.0		30		35

TEST CIRCUIT

20 MHZ (3 PULSE) TOGGLE TEST

FIG. 110



V_{CC} For Test Circuit ..... +5.0V
V_{CC} For MIC 950 Under Test ..... +4.0V
Test Device For Both Positions of the S_D-C_D Switch.
Suitable Precautions Must Be Used When Wiring Test Jig.

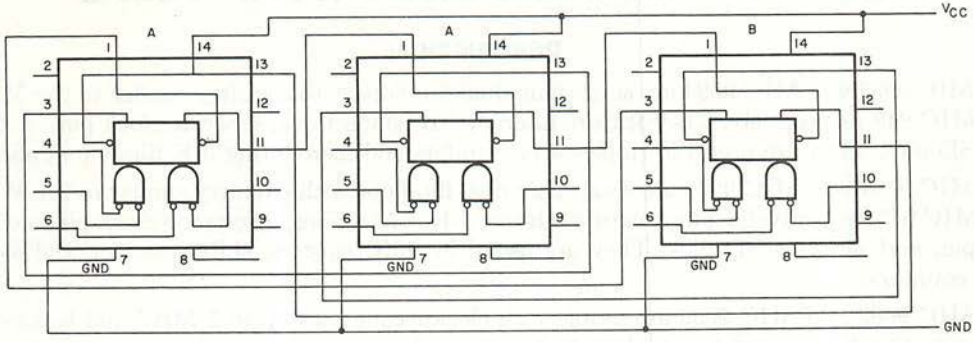
RELIABILITY TESTS

PERFORMED DURING ITT RELIABILITY PROGRAM
MEASUREMENTS OF THE FOLLOWING PARAMETERS ARE RECORDED:

Parameter	Test Sequence Number on Page 50
I_R	#2 & #6
I_{MAX}	#11
V_{OL}	#15
V_{OH}	#17
$-I_{FS}$	#21 & #22

LIFE TEST CIRCUIT

FIG. 111



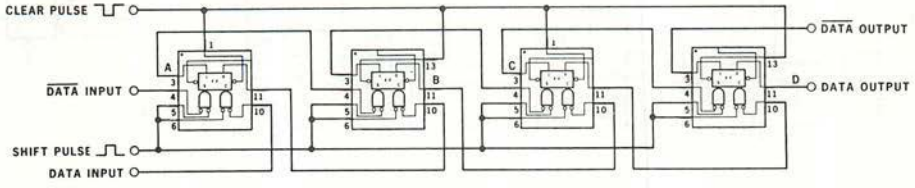
NOTE:

V_{CC} = +5.5 Volts Ambient Temperature = +125°C
Circuit may have an odd number of units connected like "A", with one connected like "B"

APPLICATIONS

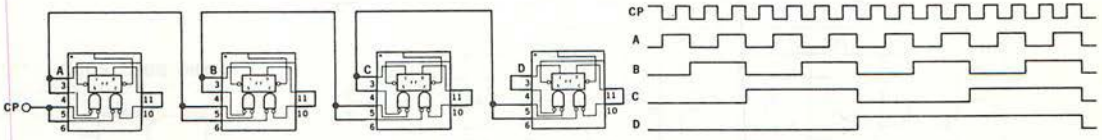
SHIFT REGISTER

FIG. 112



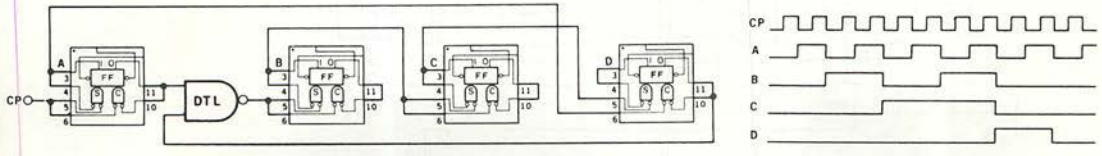
RIPPLE-CARRY BINARY COUNTER

FIG.113



RIPPLE-CARRY DECADE COUNTER

FIG. 114



DUAL FLIP-FLOPS

MIC 9093 MIC 9094 MIC 9097 MIC 9099
DUAL DTL MASTER-SLAVE J-K FLIP-FLOPS

DESCRIPTION

The MIC 9093 and MIC 9094 are single chip dual flip-flops with circuitry similar to the MIC 945 and MIC 948 respectively. They feature internal J-K connections, separate clock pins, and separate SD pins. They are useful in ripple-carry counters and many other J-K flip-flop applications.

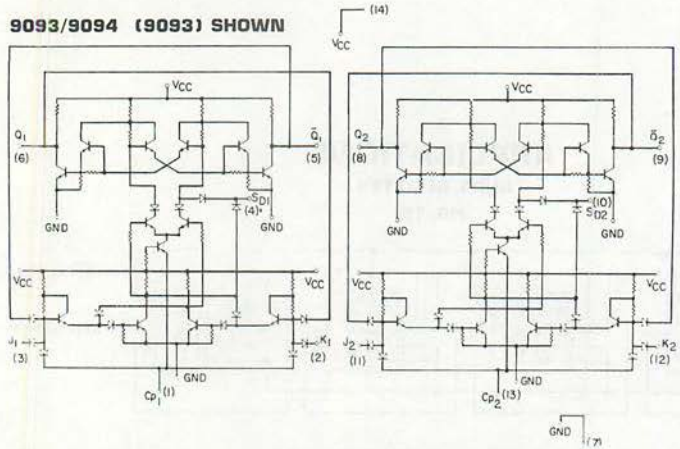
The MIC 9097 and MIC 9099 are single chip dual flip-flops with circuitry similar to the MIC 948 and MIC 945 respectively. They feature internal J-K connections, a common clock pin, a common CD pin, and separate SD pins. They are useful in shift registers, shift counters, and synchronous counters.

The MIC 9093 and MIC 9099 are usable with clock frequencies up to 5 MHZ and feature a DC level sensitive clock input for stable operation regardless of clock waveshape.

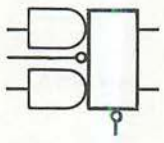
The MIC 9094 and MIC 9097 are usable with clock frequencies up to 8 MHZ.

These circuits are fully compatible with the ITT MIC 930 series DTL family and the ITT MIC 9000 series TTL family.

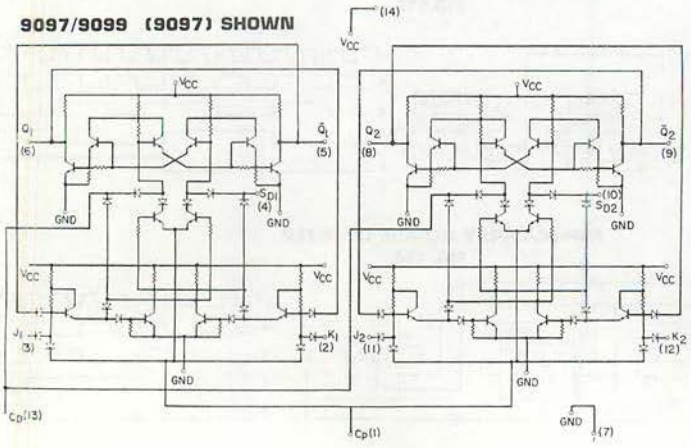
9093/9094 (9093) SHOWN



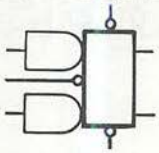
½ MIC 9093/9094



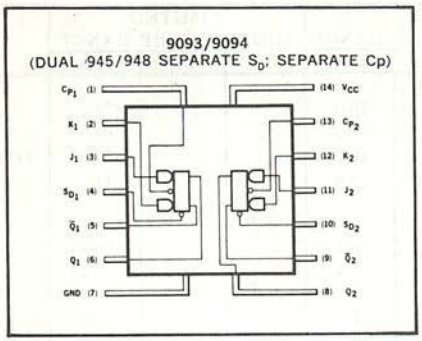
9097/9099 (9097) SHOWN

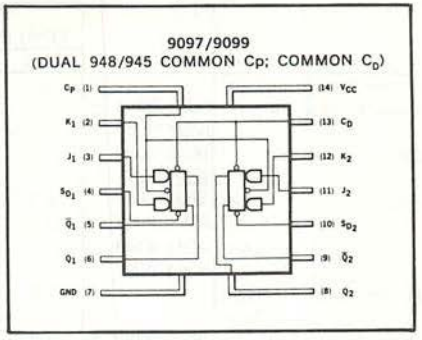


½ MIC 9097/9099



PIN CONFIGURATION (9093/9094 AND 9097/9099)





ABSOLUTE MAXIMUM RATINGS

(Above which useful life may be impaired)

Supply Voltage (V_{CC}) Continuous	−0.5 to +8.0	Volts
Supply Voltage (V_{CC}) Pulsed <1.0 second	+12.0	Volts
Power Dissipation 25°C Ambient (Note 1)	500	mw
Operating Temperature Range	−55 to +125	°C
Storage Temperature Range	−65 to +150	°C
Lead Temperature (soldering 60 second)	+300	°C
Input Voltage Applied to Input	−1.5 to +5.5	Volts

NOTE 1: Degradation by 3.3 mw per degree C for ambient temperatures above 25°C.

TRUTH TABLES

SYNCHRONOUS ENTRY

Inputs		Output
J	K	Q_{n+1}
0	0	Q_n
0	1	0
1	0	1
1	1	$\bar{Q}_n$

ASYNCHRONOUS ENTRY

Inputs		Outputs	
S_D	C_D	Q	$\bar{Q}$
0	0	1	1
0	1	1	0
1	0	0	1
1	1	No Change	

NOTES:

1. Positive logic: O=L, 1=H is shown.
2. With synchronous entry, output changes occur as clock level changes from High to Low. For operation in accordance with the table, J and K inputs should normally be changed while the clock is low, and maintained while the clock is high.
3. Asynchronous entry overrides synchronous entry, regardless of clock level. If S_D and C_D are both low, then both go high simultaneously, final condition cannot be predicted. For proper operation, the S_D or C_D terminals must be held in the low state for at least 50 nanoseconds.
4. From circuit symmetry, the S_D and C_D pin designations may be interchanged by interchanging the J and K, and also the Q and $\bar{Q}$ pin designations. Thus, the 9093–9094 may be used as a dual flip-flop having C_D terminals available, and the 9097–9099 may be used as a dual flip-flop having separate C_D terminals and a common S_D terminal.
   All rules for MIC 945 apply to MIC 9093 and 9099
   All rules for MIC 948 apply to MIC 9094 and 9097
5. Refer to the MIC 945/948 section of ITT's New Unabridged DTL Design Data Book for typical operating characteristics.

DUAL FLIP-FLOPS

SUMMARY OF MIC 9093/9094 AND 9097/9099 CHARACTERISTICS (25°C)

Network Parameter	Note	FULL TEMPERATURE RANGE Min.	Typ.	Max.	LIMITED TEMPERATURE RANGE Min.	Typ.	Max.	Unit
Operating Supply Voltage	1	4.5	5.0	5.5		5.0		Volts
Network Dissipation	9093/9099 2			70.0			75.0	mW
	9094/9097			81.0			87.5	
Loading D.C. Fanout	9093/9099			10.0			12.0	DTL Unit
	9094/9097			9.0			11.0	Load
Output Logic '1' (High)	9093/9099	2.5			2.5			Volts
	9094/9097	2.5			4.2			
'O' (Low)	9093/9099			0.4			0.45	
	9094/9097			0.4			0.45	
Input Threshold '1' (High)	3	1.9			1.9			Volts
'O' (Low)				1.1			1.1	
Propagation $t_{pd}+$	9093/9099 4	35.0		75.0	35.0		75.0	Nano-
Delay Time	9094/9097	30.0		65.0	30.0		65.0	Second
$t_{pd}-$	9093/9099	30.0		75.0	30.0		75.0	
	9094/9097	30.0		75.0	30.0		75.0	
Noise Immunity		0.35	>0.5		0.35	>0.5		Volts

NOTES: 1. Exact specification limits for operating temperature range may be obtained by reference to the appropriate test.
2. Power supplied from V_{CC}(5V) during "ON" state, Fanout = 0.
3. Input threshold voltage is defined as the minimum (or maximum) voltage at the circuit input to guarantee a low (or high) output.
4. Propagation delay time terms ($t_{pd}+$ and $t_{pd}-$) are described in the t_{pd} test circuit, Page 8.

9093/9094 TEST SEQUENCE

Test No.	Notes	FORCING CONDITIONS AT PINS C_P 1(13)	K 2(12)	J 3(11)	S_D 4(10)	$\overline{Q}$ 5(9)	Q 6(8)	V_{CC} 14	Sense	TEST LIMITS Min.	Max.
1	1,2	GND	GND	GND	GND			V_{MAX}	I_{14}		I_{MAX}
2	1,2				GND			V_{PD}	I_{14}		I_{PDH}
3 (4)	1	V_R		GND				V_R	$I_1(I_{13})$		I_{RCP}
5 (6)	1	V_R	GND		GND			V_R	$I_1(I_{13})$		I_{RCP}
7 (8)	1	GND		V_R		GND		V_{CCH}	$I_3(I_{11})$		I_R
9(10)	1	GND	V_R				GND	V_{CCH}	$I_2(I_{12})$		I_R
11(12)	1	C_{P2}	GND		V_R			V_{CCH}	$I_4(I_{10})$		$2I_R$
13(14)	1				GND		V_{CEX}	V_{CEX}	$I_6(I_8)$		I_{CEX}
15(16)	1	C_{P2}	V_R	GND	V_R	V_{CEX}		V_{CEX}	$I_5(I_9)$		I_{CEX}
17(18)	1	C_{P2}	V_R	GND	V_{IL}		$-I_{OH}$	V_{CCL}	$V_6(V_8)$	V_{OH}	
19(20)	1	C_{P2}	V_R	GND	V_R	$-I_{OH}$		V_{CCL}	$V_5(V_9)$	V_{OH}	
21(22)	1,3	C_{P1}	V_R	GND	V_R		I_{OL1}	V_{CCL}	$V_6(V_8)$		$V_{OL}1$
23(24)	1,3	C_{P1}	V_R	GND	V_R		I_{OL2}	V_{CCH}	$V_6(V_8)$		$V_{OL}2$
25(26)	1,3				GND	I_{OL1}		V_{CCL}	$V_5(V_9)$		$V_{OL}1$
27(28)	1,3				GND	I_{OL2}		V_{CCH}	$V_5(V_9)$		$V_{OL}2$
29(30)	1,3	C_{P4}	V_{IH}	GND	C_{P1}			V_{CCH}	$V_6(V_8)$		$V_{OL}2$
31(32)	1	V_F			V_{IL}			V_{CCH}	$-V_1(V_{13})$		$-I_{FCP1}$
33(34)	1	C_{P3}	V_R	V_F	C_{P1}			V_{CCH}	$-I_3(I_{11})$		$-2/3I_{F1}$
35(36)	1		V_F		GND			V_{CCH}	$-I_2(I_{12})$		$-2/3I_{F1}$
37(38)	1			GND	V_F			V_{CCH}	$I_4(I_{10})$		$-I_{FS1}$
39(40)	1	C_{P2}	V_R	$-V_S$	V_R	GND		V_{CCH}	$-I_5(I_9)$	$-I_{SC}$ (Min.)	$-I_{SC}$ (Max.)
41(42)	1		$-V_S$		GND		GND	V_{CCH}	$-I_6(I_8)$	$-I_{SC}$ (Min.)	$-I_{SC}$ (Max.)
43(44)		TPD+ See Test Figure and Table									
45(46)		TPD− See Test Figure and Table									
47(48)	1,4	V_F			V_{IL}			V_{CCL}	$-V_1(V_{13})$		$-I_{FCP2}$
49(50)	1,4	C_{P3}	V_R	V_F	C_{P1}			V_{CCL}	$-I_3(I_{11})$		$-2/3\ I_{F2}$
51(52)	1,4		V_F		GND			V_{CCL}	$-I_2(I_{12})$		$-2/3\ I_{F2}$
53(54)	1,4			GND	V_F			V_{CCL}	$I_4(I_{10})$		$-I_{FS2}$

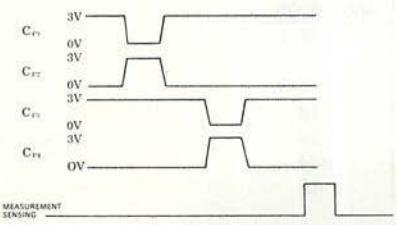
NOTES: 1. Pin 7 is grounded for all tests. 2. Tests 1 and 2 only; forcing conditions applied to both flip-flops simultaneously.
3. Tests 21 through 30 only; ground Q, S_D, and C_P of opposite flip-flop. 4. Tests 47/54 apply to full temperature range only.

9097/9099 TEST SEQUENCE

Test No.	Notes	FORCING CONDITIONS AT PINS								Sense	TEST LIMITS	
		C_P 1	K 2(12)	J 3(11)	S_D 4(10)	$\bar{Q}$ 5(9)	Q 6(8)	C_D 13	V_{CC} 14		Min.	Max.
1	1,2	GND	GND	GND	GND			GND	V_{MAX}	I_{14}		I_{MAX}
2	1,2							GND.	V_{PD}	I_{14}		I_{PDH}
3(4)	1	V_R		GND				GND	V_R	I_1		$2I_{RCP}$
5(6)	1	V_R	GND		GND				V_R	I_1		$2I_{RCP}$
7(8)	1	GND		V_R		GND			V_{CCH}	$I_3(I_{11})$		I_R
9(10)	1	GND	V_R				GND		V_{CCH}	$I_2(I_{12})$		I_R
11(12)	1	C_{P2}	GND		V_R				V_{CCH}	$I_4(I_{10})$		I_R
13	1,2	C_{P2}		GND				V_R	V_{CCH}	I_{13}		$2I_R$
14(15)	1				GND		V_{CEX}	GND	V_{CEX}	$I_6(I_8)$		I_{CEX}
16(17)	1				GND	V_{CEX}		GND	V_{CEX}	$I_5(I_9)$		I_{CEX}
18(19)	1	C_{P2}	V_R	GND	V_{IL}		$-I_{OH}$	V_R	V_{CCL}	$V_6(V_8)$	V_{OH}	
20(21)	1	C_{P2}	GND	V_R	V_R	$-I_{OH}$		V_{IL}	V_{CCL}	$V_5(V_9)$	V_{OH}	
22(23)	1	GND			V_R		I_{OL}	GND	V_{CCL}	$V_6(V_8)$		$V_{OL}1$
24(25)	1	GND			V_R		I_{OL}	GND	V_{CCH}	$V_6(V_8)$		$V_{OL}2$
26(27)	1	GND			GND	I_{OL}		V_R	V_{CCL}	$V_5(V_9)$		$V_{OL}1$
28(29)	1	GND			GND	I_{OL}		V_R	V_{CCH}	$V_5(V_9)$		$V_{OL}2$
30(31)	1	C_{P4}	V_{IH}	GND	C_{P1}			V_R	V_{CCH}	$V_6(V_8)$		$V_{OL}2$
32(33)	1	C_{P4}	GND	V_{IH}	V_R			C_{P1}	V_{CCH}	$V_5(V_9)$		$V_{OL}2$
34(35)	1			V_F				GRD	V_{CCH}	$-I_3(I_{11})$		$-2/3I_{F1}$
36(37)	1		V_F		GND				V_{CCH}	$-I_2(I_{12})$		$-2/3I_{F1}$
38(39)	1	GND			V_F			GND	V_{CCH}	$-I_4(I_{10})$		$-I_{FSI1}$
40	1,2	GND			GND			V_F	V_{CCH}	$-I_{13}$		$-2I_{FSI1}$
41(42)	1			GND	V_F				V_{CCH}	$-I_4(I_{10})$		$-I_{FSI}$
43	1,2		GND					V_F	V_{CCH}	$-I_{13}$		$-2I_{FSI}$
44	1,2	V_F			V_{IL}				V_{CCH}	$-I_1$		$-2I_{FCP1}$
45	1	V_F						V_{IL}	V_{CCH}	$-I_1$		$-2I_{FCP1}$
46(47)	1		$-V_S$		GND		GND	GND	V_{CCH}	$-I_6(I_8)$	$-I_{SC}$ (min.)	$-I_{SC}$ (max.)
48(49)	1			$-V_S$	GND	GND		GND	V_{CCH}	$-I_5(I_9)$	$-I_{SC}$ (min.)	$-I_{SC}$ (max.)
50(51)	TPD+	See Test Figure and Table										
52(53)	TPD−	See Test Figure and Table										
54(55)	1,3			V_F				GRD	V_{CCL}	$-I_3(I_{11})$		$-2/3I_{F2}$
56(57)	1,3		V_F		GND				V_{CCL}	$-I_2(I_{12})$		$-2/3I_{F2}$
58(59)	1,3	GND			V_F			GND	V_{CCL}	$-I_4(I_{10})$		$-I_{FSI2}$
60	1,2,3	GND			GND			V_F	V_{CCL}	$-I_{13}$		$-2I_{FSI2}$
61(62)	1,3			GND	V_F				V_{CCL}	$-I_4(I_{10})$		$-I_{FS2}$
63	1,2,3		GND					V_F	V_{CCL}	$-I_{13}$		$-2I_{FS2}$
64	1,2,3	V_F			V_{IL}				V_{CCL}	$-I_1$		$-2I_{FCP2}$
65	1,2,3	V_F						V_{IL}	V_{CCL}	$-I_1$		$-2I_{FCP}$

NOTES: 1. Pin 7 is grounded for all tests. 2. Tests 1, 2, 13, 40, 43, 44, 60, 63, 64 and 65 only; forcing conditions applied to both flip-flops simultaneously. 3. Tests 54/65 apply to full temperature range only.

PROPAGATION DELAY CONDITIONS AND LIMITS



($T_A = +25°C$)

		TEST CONDITIONS R ohms	C PF	LIMITS Min. nsec.	Max. nsec.
TPD+	9093,9099	2K	30	35.	75
TPD−	9093,9099	330	50	30	75
TPD+	9094,9097	2K	30	30	65
TPD−	9094,9097	330	50	30	75

TEST LIMITS

Parameter	Units	FULL TEMPERATURE RANGE						LIMITED TEMPERATURE RANGE					
		−55°C		+25°C		+125°C		0°C		+25°C		+75°C	
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.
V_{OH} 9093/9099	Volts	2.5		2.5		2.5		2.6		2.6		3.1	
V_{OH} 9094/9097	Volts	2.5		2.5		2.5		4.3		4.3		4.3	
V_{OL}	Volts		0.4		0.4		0.4		0.45		0.45		0.45
$V_{OL}2$ 9093/9099	Volts		0.4		0.4		0.4		0.45		0.45		0.45
$V_{OL}2$ 9094/9097	Volts		0.4		0.4		0.4		0.45		0.45		0.45
I_{MAX} 9093	mA				40						42		
I_{MAX} 9094	mA				43						48		
I_{MAX} 9097	mA				32						35		
I_{MAX} 9099	mA				36						38		
I_{PDH} 9093/9099	mA				28						30		
I_{PDH} 9094/9097	mA				32.4						35		
$-I_{SC}$ 9093/9099	mA	0.7	1.33	0.7	1.33	.625	1.30	.59	1.41	.59	1.41	.55	1.38
$-I_{SC}$ 9094/9097	mA	2.1	3.96	2.1	3.96	1.86	3.54	1.77	4.2	1.77	4.2	1.6	4.0
$-2/3\ I_F$	mA		.98		.98		.92		.95		.95		.90
I_{FSI}	mA		2.93		2.93		2.57		2.8		2.8		2.66
$2I_{FSI}$	mA		5.86		5.86		5.86		5.6		5.6		5.32
I_{FS}	mA		2.2		2.2		1.93		2.1		2.1		2.0
$2I_{FS}$	mA		4.4		4.4		3.86		4.2		4.2		4.0
I_{FCP} 9093	mA		2.93		2.93		2.57		2.8		2.8		2.66
I_{FCP} 9094	mA		2.35		2.35		2.03		2.24		2.24		2.13
$2I_{FCP}$ 9097	mA		4.68		4.68		4.04		4.48		4.48		4.26
$2I_{FCP}$ 9099	mA		5.86		5.86		5.14		5.6		5.6		5.32
I_{CEX}	uA				52						105		
I_{RCP}	uA		10		10		20		20		20		30
$2I_{RCP}$	uA		20		20		40		40		40		60
I_R	uA		2		2		5		5		5		10
$2I_R$	uA		4		4		10		10		10		20
$-2/3\ I_{F2}$	mA		.76		.76		.72						
I_{FSI2}	mA		2.26		2.26		2.20						
$2\ I_{FSI2}$	mA		4.52		4.52		4.40						
I_{FS2}	mA		1.7		1.7		1.5						
$2\ I_{FS2}$	mA		3.4		3.4		3.0						
I_{FCP2} (9093)	mA		2.26		2.26		2.02						
I_{FCP2} (9094)	mA		1.83		1.83		1.59						
$2\ I_{FCP2}$ (9097)	mA		3.66		3.66		3.18						
$2\ I_{FCP2}$ (9099)	mA		4.52		4.52		4.04						

RELIABILITY TESTS

PERFORMED DURING ITT RELIABILITY PROGRAM

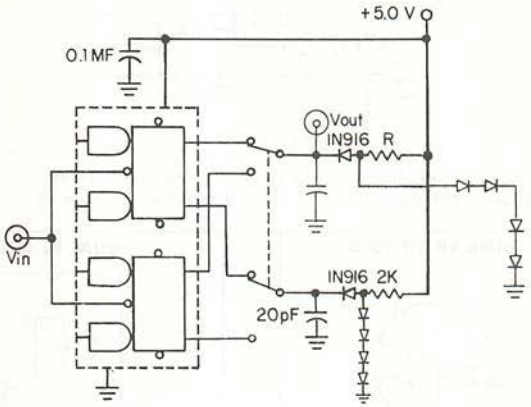
MEASUREMENTS OF THE FOLLOWING PARAMETERS ARE RECORDED:

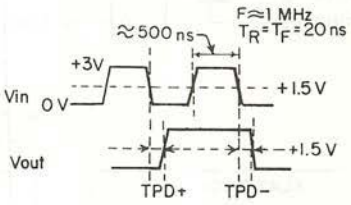
Parameter	Test Sequence Number on Pages 56, 57	
	9093/9094	9097/9099
$2I_{RCP}$	#3	#3(4)
I_{RCP}	#3(4)	
I_R	#7(8)	#7(8)
V_{OH}	#17	#18
V_{OL}	#21	#22
$-2/3I_F$	#33	#34
I_{PDH}	#2	#2

FORCING CONDITIONS

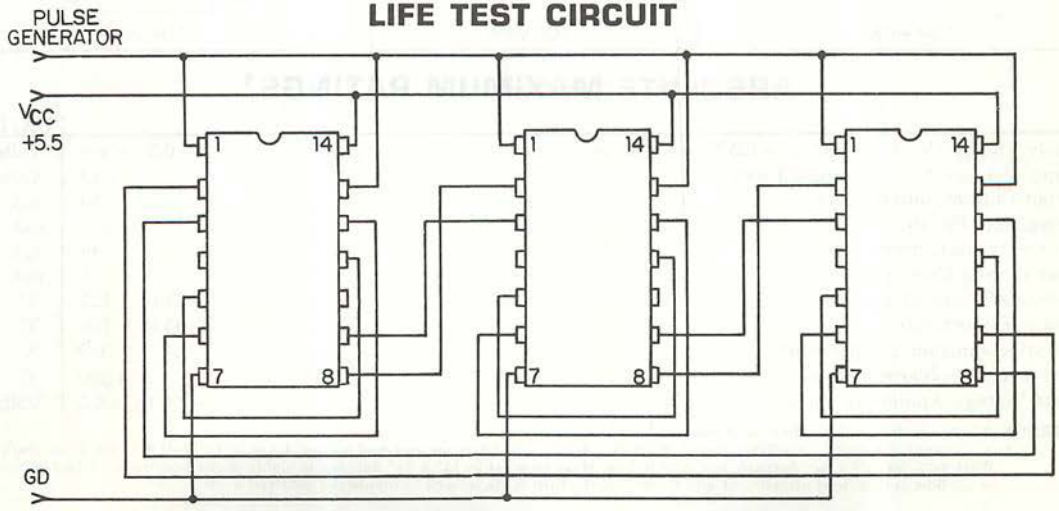
Parameter	Units	−55°C	+25°C	+125°C
V_{CCH}	Volts	5.5	5.5	5.5
V_{CCL}	Volts	4.5	4.5	4.5
V_{CEX}	Volts		4.5	
V_{MAX}	Volts		8.0	
V_{PD}	Volts		5.0	
V_{IH}	Volts	2.1	1.9	1.7
V_{IL}	Volts	1.4	1.1	0.8
V_F	Volts	0.4	0.4	0.4.
V_R	Volts	4.0	4.0	4.0
$-I_{OH}$	uA	115	115	115
I_{OH} 9093/9099	μA	180	180	180
I_{OH} 9094/9097	μA	540	540	540
I_{OL1} 9093/9099	mA	12.0	12.0	12.0
I_{OL2} 9093/9099	mA	15.0	15.0	15.0
I_{OL1} 9094/9097	mA	13.0	13.0	13.0
I_{OL2} 9094/9099	mA	13.6	13.6	13.6

Parameter	Units	0°C	+25°C	+75°C
V_{CCH}	Volts	5.0	5.0	5.0
V_{CCL}	Volts	5.0	5.0	5.0
V_{CEX}	Volts		5.0	
V_{MAX}	Volts		8.0	
V_{PD}	Volts		5.0	
V_{IH}	Volts	2.0	1.9	1.8
V_{IL}	Volts	1.2	1.1	0.95
V_F	Volts	0.45	0.45	0.45
V_R	Volts	4.0	4.0	4.0
$-I_{OH}$	uA	110	110	110
I_{OL} 9093/9099	mA	15.8	15.8	15.1
I_{OL} 9094/9097	mA	14.4	14.4	13.7
$-V_S$	Volts	−1.0	−1.0	−1.0





LIFE TEST CIRCUIT



MONOSTABLE MULTIVIBRATOR MIC 941/951

DESCRIPTION

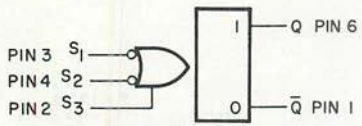
The MIC 941/951 is a monostable multivibrator.

The 941/951 provides a pair of complementary output pulses which are typically 100 nsec wide when it is triggered with an external pulse. The width of the output pulse is adjustable to greater than 100ns by the addition of an external resistor and/or capacitor.

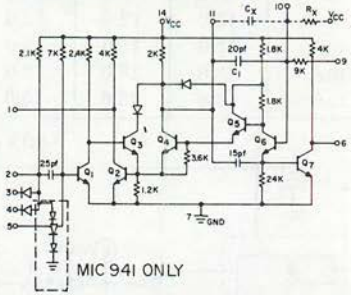
The output pulse width is very stable as either power supply voltage or temperature are varied when an external timing resistor is used instead of the internal diffused resistor.

This circuit is very useful in providing DTL compatible pulses from other sources.

POSTIVE LOGIC SYMBOLS

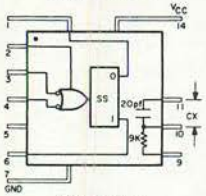


CIRCUIT SCHEMATIC



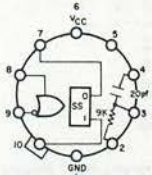
All data in this specification refers to 14-pin package numbers except TO-5 outline and the 10-pin reference numbers in the test sequence on Page 61.

FLAT PACK



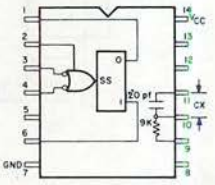
TOP VIEW

SIMILAR TO TO-5



TOP VIEW

DUAL IN-LINE



TOP VIEW

ABSOLUTE MAXIMUM RATINGS[1]

		UNITS
Supply Voltage (V_{CC}), −55°C to +125°C, continuous	−0.5 to +8	Volts
Supply Voltage (V_{CC}), pulsed, <1 sec	+12	Volts
Output Current, into outputs	50	mA
Current into Pin 10	5	mA
Input Forward Current	−10	mA
Input Reverse Current	1	mA
Operating Temperature	−55 to +125	°C
Storage Temperature	−65 to +150	°C
Operating Junction Temperature[2]	+175	°C
Lead Temp. (soldering, 60 sec.)	+300	°C
Input Voltage Applied to Input	−1.5 to +5.5	Volts

NOTES: 1. Above which useful life may be impaired.

2. Allow 200°C/Watt θ_{J-A} for TO-5; 300°C/Watt θ_{J-A} for ¼" x ¼" flatpack and dual in-line. Allow 50°C/Watt θ_{J-C} for TO-5; 180°C/Watt θ_{J-C} for ¼" x ¼" flatpack and dual in-line. Heat removal in ¼" x ¼" flatpack is highly dependent upon contact surfaces or air flow and on lead attachment and thermal paths thru leads, as well as number of soldered leads.

TEST SEQUENCE

Test	Pin no.:	5	1	2	3	4	6	7	9	10	11	14	LIMITS		
No.	TO-5 Pin no.:		7	8	9	—	10	1	2	3	4	6	Sense	Min.	Max.
1				V_F				GND				V_{CCH}	I_2	$-.5I_F$	
2					V_F	V_R		GND				V_{CCH}	I_3	$-.5I_F$	$-2I_{F1}$
3	Note 1				V_R	V_F		GND				V_{CCH}	I_4	$-.5I_F$	$-2I_{F1}$
4	Note 2							GND			V_F	V_{CCH}	I_{11}	$-.5I_F$	
5				GND	V_R			GND				V_{CCH}	I_3		I_R
6	Note 1			GND		V_R		GND				V_{CCH}	I_4		I_R
7			I_{OL1}					GND		GND		V_{CCL}	V_1		V_{OL1}
8		GND	I_{OL1}					GND				V_{CCL}	V_1		V_{OL1}
9							I_{OL1}	GND	V_{CCL}			V_{CCL}	V_6		V_{OL1}
10			$-I_{OH}$	GND				GND	V_{CCL}			V_{CCL}	V_1	V_{OH}	
11							I_{OH}	GND		GND		V_{CCL}	V_6	V_{OH}	
12								GND	V_{CCH}	GND		V_{CCH}	I_9	I_{9K}	I_{9K}
13					GND	GND		GND	V_{PD}			V_{PD}	$I_9 + I_{14}$		I_{PDL}
14					GND	GND		GND				V_{MAX}	I_{14}		I_{MAX}
15								GND	V_{CCH}			V_{CCH}	V_2	V_{2L}	V_{2H}
16	t_{pd}— Pin 1	See Test Circuit Page 59													
17	t_{pd}+ Pin 6	See Test Circuit Page 59													
18	Pulse width Pin 1	See Test Circuit Page 59													
19	Pulse width Pin 6	See Test Circuit Page 59													
20	Note 3		I_{OL2}					GND		GND		V_{CCH}	V_1		V_{OL2}
21	Note 3	GND	I_{OL2}					GND				V_{CCH}	V_1		V_{OL2}
22	Note 3						I_{OL2}	GND	V_{CCH}			V_{CCH}	V_6		V_{OL2}
23	Note 3				V_F	V_R		GND				V_{CCL}	I_3		$-2\ I_{F2}$
24	Note 3				V_R	V_F		GND				V_{CCL}	I_4		$-2\ I_{F2}$

NOTE: 1. These tests do not apply to 10-pin TO-5 packages. 2. Applies to limited temperature range only.
3. Tests 20/24 apply to full temperature range only.

FORCING CONDITIONS

		FULL TEMPERATURE RANGE					LIMITED TEMPERATURE RANGE			
Parameter	Units	−55°C	+25°C	+125°C	Parameter	Units	0°C	+25°C	+75°C
V_{CCH}	Volts	5.5	5.5	5.5	V_{CCH}	Volts	5.0	5.0	5.0
V_{CCL}	Volts	4.5	4.5	4.5	V_{CCL}	Volts	5.0	5.0	5.0
V_{PD}	Volts		5.0		V_{PD}	Volts		5.0	
V_{MAX}	Volts		8.0		V_{MAX}	Volts		8.0	
V_R	Volts	4.0	4.0	4.0	V_R	Volts	4.0	4.0	4.0
V_F	Volts	0.4	0.4	0.4	V_F	Volts	.45	.45	.5
$I_{OL1,2}$	mA	15.0	15.0	15.0	I_{OL}	mA	14.8	14.8	14.0
$-I_{OH}$	mA	.18	.18	.18	$-I_{OH}$	mA	.15	.15	.15

TEST LIMITS

		FULL TEMPERATURE RANGE						LIMITED TEMPERATURE RANGE					
		−55°C		+25°C		+125°C		0°C		+25°C		+75°C	
Parameter	Units	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.
$-.5I_F$	mA	0.8		0.8		0.75		.65		.6		.65	
$-2I_{F1}$	mA		2.93		2.93		2.75		2.6		2.8		2.66
I_R	μA		5.0		5.0		10.0		5.0		5.0		10.0
V_{OL1}	Volts		.4		.4		.4		.5		.45		.5
V_{OH}	Volts	2.5		2.5		2.5		3.2		3.2		3.2	
I_{9K}	mA			.5	.75					.4	.95		
I_{PDL}	mA				9.0						11.8		
I_{MAX}	mA				21.4						23.1		
V_{2L} 941	Volts			1.8	2.5					1.7	2.6		
V_{2H} 951	Volts			5.0						4.5			
V_{OL2}	Volts		.4		.4		.4						
$-2\ I_{F2}$	mA		2.26		2.26		2.22						

MIC 951 SWITCHING TIME TEST CIRCUIT AND WAVEFORMS

TEST LIMITS

	Limited Temp. Range		Full Temp. Range	
	Min. Nano-seconds	Max. Nano-seconds	Min. Nano-seconds	Max. Nano-seconds
$t_{pd}-$		40		40
$t_{pd}+$		40		40
Pin 1	90	330	90	220
Pin 6	70	270	70	160

FIG. 115

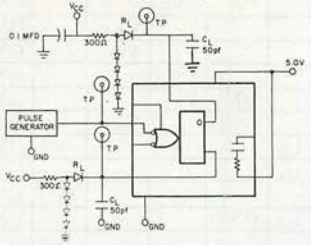
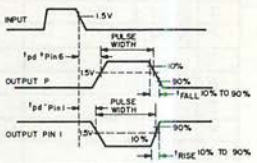


FIG. 116



Suitable precautions must be used when wiring test jig.

TYPICAL DC CHARACTERISTICS

FIG. 117

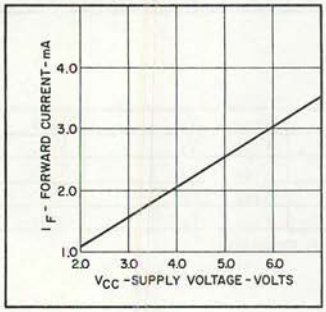


FIG. 118

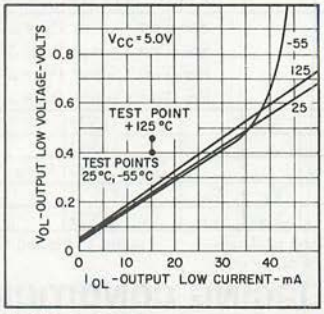
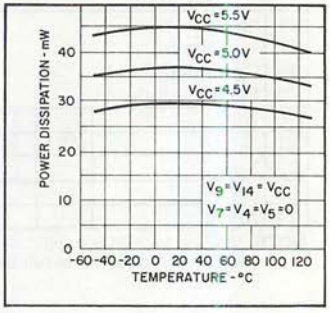


FIG. 119



TIMING CHARACTERISTICS

FIG. 120

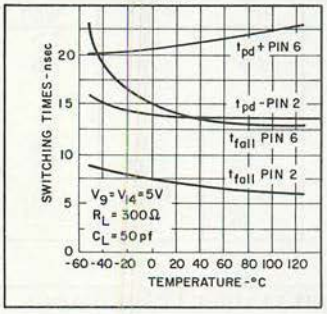


FIG. 121

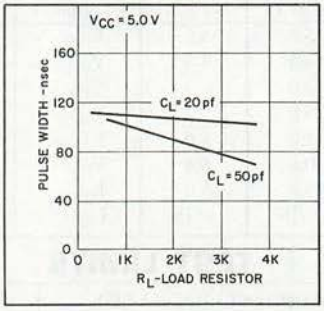


FIG. 122

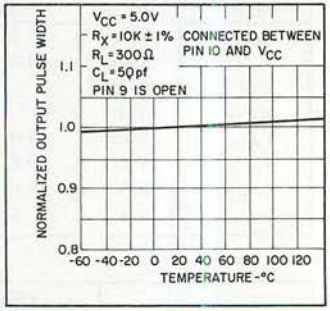


FIG. 123

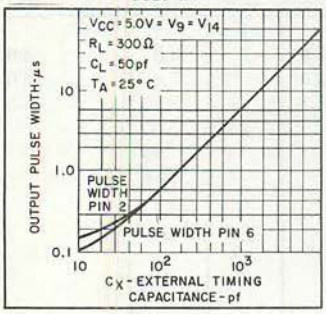


FIG. 124

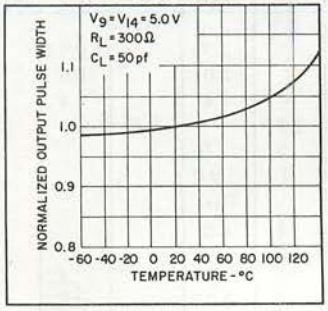
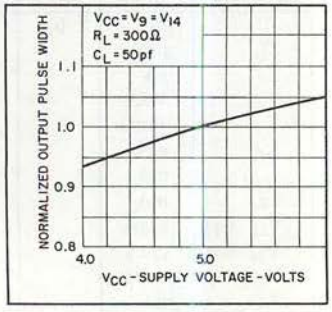


FIG. 125



INPUT-OUTPUT LOAD FACTORS

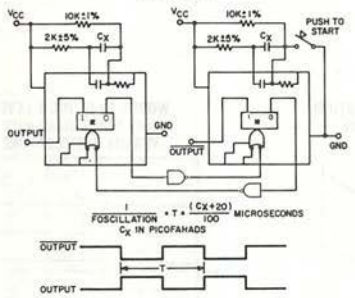
1. Each MIC 951 input should be rated at 2 loads.
2. Each MIC 951 output may drive 10 DTL loads.
3. For input-output load factors of other DTL elements, please refer to the individual DTL element specifications.

APPLICATIONS

RULES FOR USE OF MIC 951

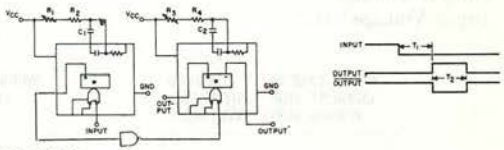
1. With Pin 9 connected to V_{CC} and no external capacitor (C_X), the output pulse width is approximately 100 nsec.
2. With Pin 9 connected to V_{CC} and an external capacitor (C_X) connected between Pins 10 and 11, the output pulse width (T) is: $T \approx 4.5\ (C_X+20)$ with C_X in pf and T in nsec.
3. For improved pulse width control, Pin 9 is left open and a stable external resistor (R_X) of 9 KΩ minimum to 15 KΩ maximum is connected from Pin 10 to V_{CC}. The output pulse width is given by the expression: $T \approx 0.5\ R_X\ (C_X+20)$ with R_X in KΩ, C_X in pf and T in nsec. (See Fig. 126)

FIG. 126



4. The output duty cycle (pulse width/period) should not exceed 40%. It may be increased to 50% by adding a 2-KΩ resistor between Pin 11 and V_{CC}. Higher duty cycles are obtainable but the output pulse width and performance are less predictable.
5. The maximum input fall time to trigger: 25 nsec for a 1.0-volt swing; 50 nsec for a 2.0-volt swing; 100 nsec for a 4.0-volt swing.
6. The AC sensitivity of the inputs may be decreased by connecting a capacitor between Pin 5 and ground.
7. The minimum pulse width at output Pin 1 is approximately 100 nsec. This pulse width may be decreased to 50 nsec by connecting a 10-KΩ resistor between Pin 5 and V_{CC}.

FIG. 127



Explanation

The input 951 determines T_1, the time before the initiation of the output pulse. The second or output 951 determines T_2, the output pulse width.

With R_2 = 10KΩ and R_1 a 5-KΩ potentiometer, T_1 is variable over a range of 2 to 3 and is given by $T_1 \approx 0.5\ (R_1+R_2)\ (C_1+20\ pf)$.

Similarly, with R_4 = 10KΩ and R_3 a 5-KΩ potentiometer, T_2 is $\approx 0.5(R_3+R_4)\ (C_2+20\ pf)$ and T_2 can be controlled by the potentiometer over a range of 2 to 3 since $10K\Omega \leq (R_3+R_4) \leq 15K\Omega$.

A much greater range in T_1 and T_2 is available by varying C_1 and C_2.

RELIABILITY TESTS

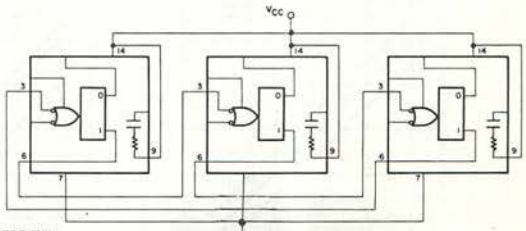
PERFORMED DURING ITT RELIABILITY PROGRAM

MEASUREMENTS OF THE FOLLOWING PARAMETERS ARE RECORDED:

Parameter	Test Sequence Number on Page 57
I_F	#2
I_R	#6
V_{OL}	#8
V_{OH}	#11
I_{MAX}	#14

LIFE TEST CIRCUIT

FIG. 128



NOTE: V_{CC} = 5.5 V, AMBIENT TEMPERATURE = 125°C

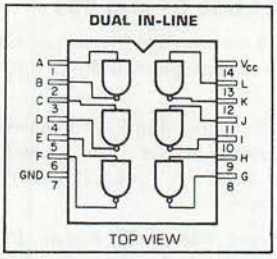
HIGH LEVEL LOGIC

HIGH LEVEL HEX INVERTER 9109, 9110, 9112

The ITT High Level Logic DTL family consists of three high voltage, high threshold hex inverters which offer extremely good D.C. and A.C. noise immunity. These circuits are useful in applications involving a high noise environment or high voltage supply which prohibits the use of current sinking logic.

Interfacing from current sinking logic to HLL is accomplished with the 9112, shifting from HLL to current sinking logic is accomplished with the 9109, and inverting HLL is done with the 9110.

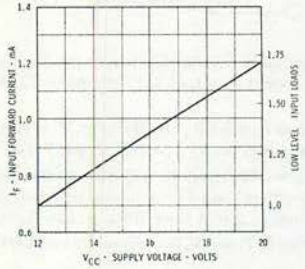
- DTL compatibility
- High Voltage Operation 12 to 20V.
- Fan Out=7 CSL.
- D.C. noise immunity 6.5V
- External input diodes to facilitate high density building block approach.



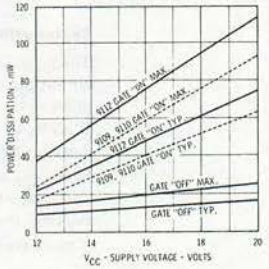
ABSOLUTE MAXIMUM RATINGS[1]

Storage Temperature	−65°C to +150°C
Operating Temperature	0°C to +75°C
V_{CC} Pin Potential to GND Pin	−5V to +25V
Output Current When Output is Low	40mA
Input Current (9109, 9110)	10mA
Output Voltage	25V
Input Voltage (9112)	5.5V

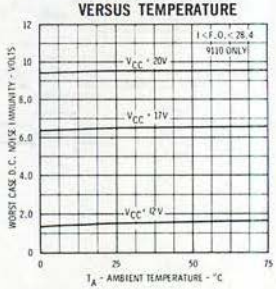
WORST CASE INPUT FORWARD CURRENT AND INPUT LOADS VERSUS SUPPLY VOLTAGE



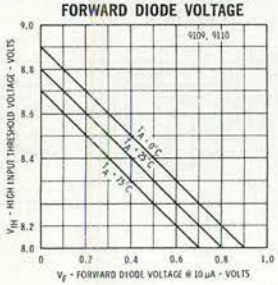
WORST CASE POWER DISSIPATION VERSUS SUPPLY VOLTAGE (PER GATE)



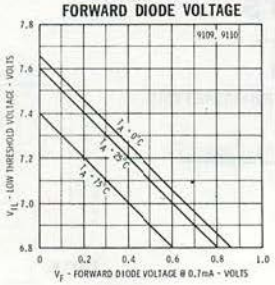
WORST CASE HIGH LEVEL D.C. NOISE IMMUNITY VERSUS TEMPERATURE



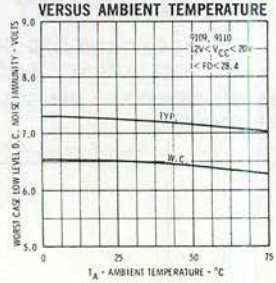
WORST CASE HIGH INPUT THRESHOLD VOLTAGE VERSUS FORWARD DIODE VOLTAGE



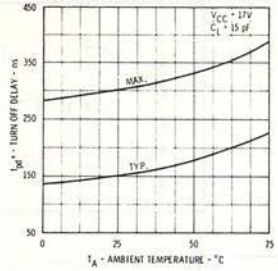
WORST CASE LOW THRESHOLD VOLTAGE VERSUS FORWARD DIODE VOLTAGE



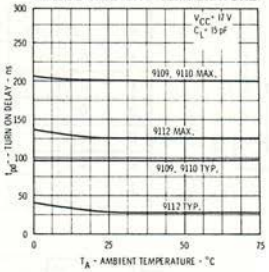
WORST CASE LOW LEVEL D.C. NOISE IMMUNITY VERSUS AMBIENT TEMPERATURE



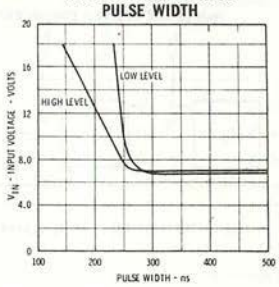
TURN OFF DELAY VERSUS AMBIENT TEMPERATURE



TURN ON DELAY VERSUS AMBIENT TEMPERATURE

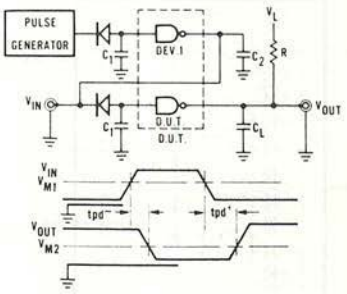


TYPICAL A.C. NOISE IMMUNITY INPUT VOLTAGE VERSUS PULSE WIDTH



SWITCHING TIME TEST CIRCUIT AND WAVEFORMS

$C_1 = 5.0$ pF Includes all probe
$C_2 = 10$ pF and jig capacitance
$C_L = 15$ pF

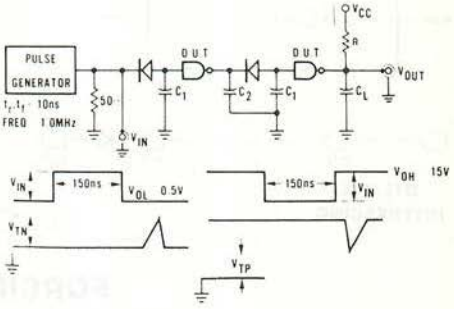


TEST CONDITIONS

D.U.T.	DEV. 1	V_{m1}(V)	V_{m2}(V)	V_L(V)	R_{tpd-}	R_{tpd+}
9109	9110	7.5	1.5	5.0	510 Ω	3.6 k
9110	9110	7.5	7.5	17.0	2.4 k	24 k
9112	932	1.5	7.5	17.0	2.4 k	24 k

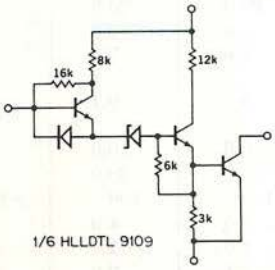
A. C. NOISE IMMUNITY TEST CIRCUIT

$C_1 = 5.0$ pF Includes jig and
$C_2 = 10$ pF all probe capacitance
$C_L = 15$ pF

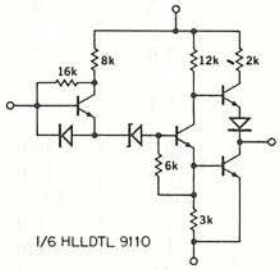


TEST CONDITIONS AND LIMITS						
TEST	LIMIT		V_{CC}	R	T_A	V_{IN}
	MIN.	MAX.	(Volts)	(kΩ)	(°C)	(Volts)
V_{TP}	8.5 V		17	24	25	10
V_{TN}		7.0 V	17	2.4	25	10

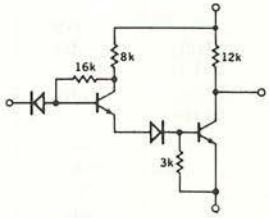
CIRCUIT SCHEMATICS



1/6 HLLDTL 9109



1/6 HLLDTL 9110

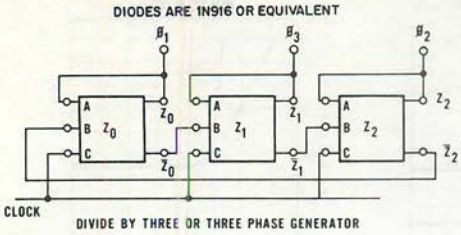


1/6 HLLDTL 9112

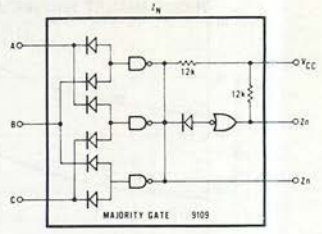
HIGH LEVEL LOGIC

APPLICATIONS

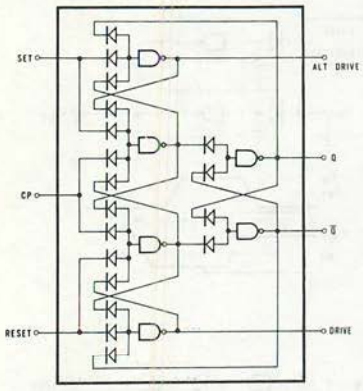
SEQUENTIAL COUNTER

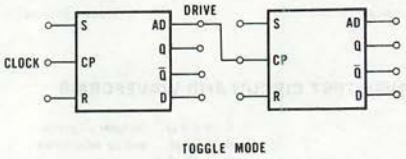


ϕ_1	ϕ_3	ϕ_2	Clock
1	0	0	0
1	0	1	1
0	0	1	0
0	1	1	1
0	1	0	0
1	1	0	1

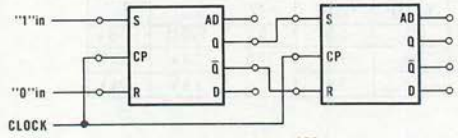


JK FLIP FLOP



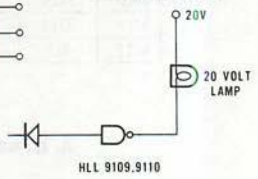


J	K	Qn+1
L	H	L
L	L	Qn
H	H	$\bar{Q}n$
H	L	H

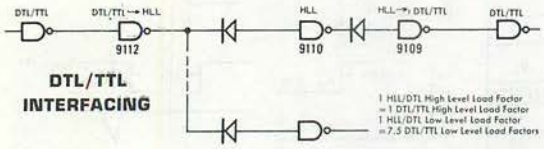


DIODES ARE 1N916 OR EQUIVALENT

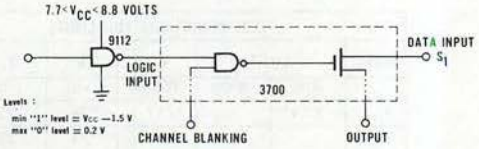
LAMP DRIVER



DTL/TTL INTERFACING



DRIVING MOS3700 MULTIPLEXER OR EQUIVALENT



FORCING CONDITIONS

Parameter	Units	FULL TEMPERATURE RANGE			LIMITED TEMPERATURE RANGE		
		−55°C	+25°C	+125°C	0°C	+25°C	+75°C
V_{MAX}	Volts		20.0			25.0	
V_{CCH}	Volts	16.5	16.5	16.5	20.0	20.0	20.0
V_{CCL}	Volts	13.5	13.5	13.5	12.0	12.0	12.0
V_{CEX}	Volts	16.5	16.5	16.5	20.0	20.0	20.0
V_F	Volts	0.0	0.0	0.0	0.0	0.0	0.0
V_{IL} (9109, 9110)	Volts	7.9	7.6	7.15	7.65	7.6	7.4
V_{IH} (9109, 9110)	Volts	9.3	9.1	8.8	9.2	9.1	9.0
I_{OLI}	mA	10.0	10.0	10.0	10.0	10.0	10.0
I_{OLZ}	mA	12.0	12.0	12.0	20.0	20.0	20.0
I_{OH}	μA	−100	−100	−100	−100	−100	−100
V_R	Volts	4.0	4.0	4.0	4.0	4.0	4.0
V_{IL} (9112)	Volts	1.3	1.0	0.5	1.05	1.0	0.8
V_{IH} (9112)	Volts	2.1	2.0	1.4	2.1	2.0	1.9
V_{OH} (9109)	Volts	16.5	16.5	16.5	18.0	18.0	18.0

TEST SEQUENCE* 9109

Test No.	Notes	FORCING CONDITIONS AT PINS							Sense	TEST LIMITS	
		Pin A (L)	Pin B (K)	Pin C (J)	Pin D (I)	Pin E (H)	Pin F (G)	V_{CC}		Min.	Max.
1								V_{CCH}	I_{VCC}		I_{PDH}
2	1	GND	V_{MAX}	GND	V_{MAX}	GND	V_{MAX}	V_{MAX}	I_{VCC}		I_{MAX}
3, (4)		V_{IL}	V_{OH}	GND		GND		V_{CCH}	$I_B(I_K)$		I_{OH}
5, (6)		GND		V_{IL}	V_{OH}	GND		V_{CCH}	$I_D(I_I)$		I_{OH}
7, (8)		GND		GND		V_{IL}	V_{OH}	V_{CCH}	$I_F(I_G)$		I_{OH}
9, (10)		V_F		GND		GND		V_{CCH}	$I_A(I_L)$		$-I_F$
11, (12)		GND		V_F		GND		V_{CCH}	$I_C(I_J)$		$-I_F$
13, (14)		GND		GND		V_F		V_{CCH}	$(I_E)(I_H)$		$-I_F$
15, (16)		V_{IH}	I_{OL1}	GND		GND		V_{CCL}	$V_B(V_K)$		V_{OL1}
17, (18)		GND		V_{IH}	I_{OL1}	GND		V_{CCL}	$V_D(V_I)$		V_{OL1}
19, (20)		GND		GND		V_{IH}	I_{OL1}	V_{CCL}	$V_F(V_G)$		V_{OL1}
21, (22)		V_{IH}	I_{OL2}	GND		GND		V_{CCH}	$V_B(V_K)$		V_{OL2}
23, (24)		GND		V_{IH}	I_{OL2}	GND		V_{CCH}	$V_D(V_I)$		V_{OL2}
25, (26)		GND		GND		V_{IH}	I_{OL2}	V_{CCH}	$V_F(V_G)$		V_{OL2}

*Ground Pin is grounded for all tests. Inputs of all unused gates are grounded.
Note 1. Test all gates simultaneously.

TEST SEQUENCE* 9110

Test No.	Notes	FORCING CONDITIONS AT PINS							Sense	TEST LIMITS	
		Pin A (L)	Pin B (K)	Pin C (J)	Pin D (I)	Pin E (H)	Pin F (G)	V_{CC}		Min.	Max.
1								V_{CCH}	I_{VCC}		I_{PDH}
2	1	GND	V_{MAX}	GND	V_{MAX}	GND	V_{MAX}	V_{MAX}	I_{GND}		I_{MAX}
3, (4)		V_{IL}	I_{OH}	GND		GND		V_{CCL}	$V_B(V_K)$	V_{OH}	
5, (6)		GND		V_{IL}	I_{OH}	GND		V_{CCL}	$V_D(V_F)$	V_{OH}	
7, (8)		GND		GND		V_{IL}	I_{OH}	V_{CCL}	$V_F(V_G)$	V_{OH}	
9, (10)		V_F		GND		GND		V_{CCH}	$I_A(I_L)$		$-I_F$
11, (12)		GND		V_F		GND		V_{CCH}	$I_C(I_J)$		$-I_F$
13, (14)		GND		GND		V_F		V_{CCH}	$I_E(I_H)$		$-I_F$
15, (16)		GND	V_{CEX}	GND		GND		V_{CEX}	$I_B(I_K)$		I_{CEX}
17, (18)		GND		GND	V_{CEX}	GND		V_{CEX}	$I_D(I_I)$		I_{CEX}
19, (20)		GND		GND		GND	V_{CEX}	V_{CEX}	$I_F(I_C)$		I_{CEX}
21, (22)		V_{IH}	I_{OL1}	GND		GND		V_{CCL}	$V_B(V_K)$		V_{OL1}
23, (24)		GND		V_{IH}	I_{OL1}	GND		V_{CCL}	$V_D(V_I)$		V_{OL1}
25, (26)		GND		GND		V_{IH}	I_{OL1}	V_{CCL}	$V_F(V_G)$		V_{OL1}
27, (28)		V_{IH}	I_{OL2}	GND		GND		V_{CCH}	$V_B(V_K)$		V_{OL2}
29, (30)		GND		V_{IH}	I_{OL2}	GND		V_{CCH}	$V_D(V_J)$		V_{OL2}
31, (32)		GND		GND		V_{IH}	I_{OL2}	V_{CCH}	$V_F(V_G)$		V_{OL2}
33, (34)		GND	GND	GND		GND		V_{CCH}	$I_B(I_K)$	I_{SC}	I_{SC}
35, (36)		GND		GND	GND	GND		V_{CCH}	$I_D(I_I)$	I_{SC}	I_{SC}
37, (38)		GND		GND		GND	GND	V_{CCH}	$I_F(I_G)$	I_{SC}	I_{SC}

HIGH LEVEL LOGIC

TEST SEQUENCE* 9112

Test No.	Notes	FORCING CONDITIONS AT PINS							Sense	TEST LIMITS	
		Pin A (L)	Pin B (K)	Pin C (J)	Pin D (I)	Pin E (H)	Pin F (G)	V_{CC}		Min.	Max.
1								V_{CCL}	I_{VCC}		I_{PDH}
2	1	GND	V_{MAX}	GND	V_{MAX}	GND	V_{MAX}	V_{MAX}	I_{CND}		I_{MAX}
3, (4)		V_R		GND		GND		V_{CCH}	$I_A(I_L)$		I_R
5, (6)		GND		V_R		GND		V_{CCH}	$I_C(I_J)$		I_R
7, (8)		GND		GND		V_R		V_{CCH}	$I_E(I_H)$		I_R
9, (10)		GND	V_{CEX}	GND		GND		V_{CCH}	$I_B(I_K)$		I_{CEX}
11, (12)		GND		GND	V_{CEX}	GND		V_{CCH}	$I_O(I_I)$		I_{CEX}
13, (14)		GND		GND		GND	V_{CEX}	V_{CCH}	$I_F(I_G)$		I_{CEX}
15, (16)		V_F		GND		GND		V_{CCH}	$I_A(I_L)$		$-I_F$
17, (18)		GND		V_F		GND		V_{CCH}	$I_C(I_J)$		$-I_F$
19, (20)		GND		GND		V_F		V_{CCH}	$I_E(I_H)$		$-I_F$
21, (22)		V_{IH}	I_{OL1}	GND		GND		V_{CCL}	$V_B(V_K)$		V_{OL1}
23, (24)		GND		V_{IH}	I_{OL1}	GND		V_{CCL}	$V_N(V_I)$		V_{OL1}
25, (26)		GND		GND		V_{IH}	I_{OL1}	V_{CCL}	$V_F(V_G)$		V_{OL1}
27, (28)		V_{IH}	I_{OL2}	GND		GND		V_{CCH}	$V_B(V_K)$		V_{OL2}
29, (30)		GND		V_{IH}	I_{OL2}	GND		V_{CCH}	$V_D(V_I)$		V_{OL2}
31, (32)		GND		GND		V_{IH}	I_{OL2}	V_{CCH}	$V_F(V_G)$		V_{OL2}
33, (34)		V_{IL}	I_{OH}	GND		GND		V_{CCH}	$V_B(V_K)$	V_{OH}	
35, (36)		GND		V_{IL}	I_{OH}	GND		V_{CCH}	$V_O(V_I)$	V_{OH}	
37, (38)		GND		GND		V_{IL}	I_{OH}	V_{CCH}	$V_F(V_G)$	V_{OH}	
39, (40)		GND	GND	GND		GND		V_{CCH}	$I_B(I_K)$	$-I_{SC}$	$-I_{SC}$
41, (42)		GND		GND	GND	GND		V_{CCH}	$I_O(I_I)$	$-I_{SC}$	$-I_{SC}$
43, (44)		GND		GND		GND	GND	V_{CCH}	$I_F(I_G)$	$-I_{SC}$	$-I_{SC}$

TEST LIMITS

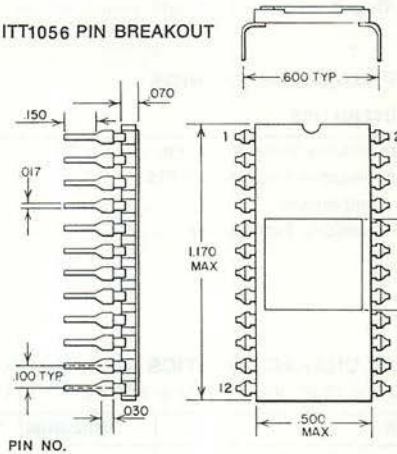
Parameter	Units	FULL TEMPERATURE RANGE						LIMITED TEMPERATURE RANGE					
		−55°C		+25°C		+125°C		0°C		+25°C		+75°C	
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.
I_{POH} (9109, 9110)	mA										28.0		
I_{POH} (9112)	mA										34.0		
I_{MAX}	mA				10						15.0		
I_{ON} (9109)	μA		75.0		75.0		75.0		75.0		75.0		75.0
$-I_F$ (9109, 9110)	mA		0.860		0.860		0.810		1.31		1.31		1.25
$-I_F$ (9112)	mA		0.825		0.825		0.800		1.15		1.15		1.10
V_{OL1}	Volts		0.5		0.5		0.5		0.5		0.5		0.5
V_{OL2}	Volts		1.0		1.0		1.0		1.0		1.0		1.0
V_{OH} (9110, 9112)	Volts	14.5		14.5		14.5		18.0		18.0		18.0	
I_R	μA		2.0		2.0		5.0		5.0		5.0		10.0
I_{CEX}	μA		50.0		50.0		50.0		75.0		75.0		75.0
I_{SC} (9110)	mA		−12.0	5.2	11.0		−11.0		−17.0	5.0	16.3		15.6
I_{SC} (9112)	mA		−1.90	1.1	1.83		−1.83		−2.4	−1.25	−2.3		−2.3

MOS COUNTER DECODER DRIVER

- **Direct drive for low voltage seven segment display tubes***
- **Counts up or down**
- **Sample and hold capability**
- **Operation to 1 MHz**
- **Dot storage and drive**
- **Packaged in a 24 pin metalized ceramic DIP**

DIMENSIONS

ITT1056 PIN BREAKOUT



PIN NO.

1 — Ground	13 — Storage Entry Command
2 — Count Disable Command	14 — Dot Output
3 — Clock Input	15 — Bar E Output
4 — Preset Command	16 — Bar F Output
5 — P1 Input (2^0)	17 — Bar C Output
6 — P2 Input (2^1)	18 — Bar D Output
7 — P3 Input (2^2)	19 — Bar G Output
8 — P4 Input (2^3)	20 — Bar B Output
9 — Count Zero Output	21 — Bar A Output
10 — Blanking Input	22 — V_{GG}
11 — Carry Propagate Output	23 — V_{DD}
12 — Dot Input	24 — Count Up/Down Command

General — The ITT 1056 MOS circuit performs the functions of up/down decade counting, binary storage, binary to decimal decoding, decimal to seven segment decoding and direct drive for low voltage seven segment display tubes.* The 1056 and the display tube share the same −27v supply.

Up/Down Count Control — The ITT 1056 counts up when a logic "0" (negative logic convention is employed here making logic zero the high voltage level) is applied to the count up/down command input (pin 24). Conversely, a logic "1" on pin 24 causes the ITT1056 to count down.

Preset Count Control — The counter is preset to any predetermined number by applying the BCD equivalent of the number on the preset inputs (pins 5, 6, 7 and 8) and a logic "1" on the preset command input (pin 4).

Count Disable Control — Accumulation of input clock pulses by the decade counter is interrupted by a logic "1" on the count disable pin 2.

Clock Input — The decade counter advances by one count for each low to high voltage transition (logic "1" to logic "0") of the clock input (pin 3) when the count disable control is in the logic "0" state.

Storage Entry Command — A logic "1" on the storage entry command pin 13 causes the BCD numbers in the decade counter to enter an intermediate storage. A logic "0" on pin 13 prevents data entering this buffer. Only BCD data currently in the buffer is converted to the seven segment display drive. Data displayed by the 1056 then corresponds to the count present in the decade counter when the storage entry pin logic level was last changed from a "1" to "0". The blanking and dot inputs are also stored in this buffer.

Blanking Input — All output drivers are turned off by a logic "1" on the blanking input pin 10 and when a logic "1" is placed on the storage entry input. This control is provided for blanking out any digit not required for display. Blanking of leading zeros is one application utilizing this input.

Dot Input Control — The dot output driver at pin 14 is controlled by the input on the dot input pin 12. A logic "1" on pin 12 and a logic "1" on the storage input pin 13 switches on the dot driver and stores it until pin 13 is again brought to a "1" level.

Forbidden Count Display — The 1056 BCD to seven segment decode circuitry detects forbidden BCD counts (10 to 15) which could inadvertently appear in the decade counter and excites the corresponding outputs to display the character "F" on the display tube.

Carry Propagate Output — The carry propagate output on pin 11 provides the necessary signal to cascade the 1056 for high frequency synchronous counting. A logic "0" appears at the carry propagate output on the nine count when counting up and on the zero count when counting down. For synchronous counting, the carry propagate signal from the nth digit must be fed to the count disable control pin 2 of the (n+1)st digit as illustrated in Figure 1. With this arrangement, the logic "0" carry propagate signal from the nth digit permits the (n+1)st digit

*Tung-Sol DT1705D and G.E. Y1938

to advance or decrease only once for every ten clock pulses input to the nth digit. Connected as shown in Figure 2, the 1107C will count asynchronously up or down.

Count Zero Output — The count zero output on pin 9 also provides a signal to cascade 1107C units. A logic "0" appears at the count zero output when there is a decimal zero in the counter counting up or down. This output connected as shown in Figure 3 will give asynchronous up counting only.

ABSOLUTE MAXIMUM RATINGS

CHARACTERISTICS		UNITS
Maximum Positive Voltage Any Pin	+0.3	Volts
Maximum Negative Voltage Any Pin	−30.0	Volts
Storage Temperature	−55 to 150	°C
Ambient Operating Temperature	−55 to 85	°C

ELECTRICAL CHARACTERISTICS — Standard Conditions (unless otherwise specified)

Load = 1.0 MΩ and 25 pF, V_{GG} = −27 V ± 1 V, V_{DD} = −13 V ± 1 V, T_A = −55°C to +85°C, V_{SS} = Ground

PARAMETER		MINIMUM	TYPICAL	MAXIMUM	UNITS	CONDITIONS
INPUTS (Any)	Logic "0"	—	—	−2.0	Volts	
	Logic "1"	−10	—	—	Volts	
	Capacitance	—	2.0	5.0	pF	
	Leakage	—	—	5.0	uA	V_{in} = −25 Volts
Pulse Duration at Logic "0" or Logic "1" Clock (i_{pw1})		0.5	—	Continuous	uS	See Figure 5
Other inputs		1.0	—	Continuous	uS	See Figure 5
Clock Rise (t_r) and Fall Times (t_f)		—	—	20	uS	See Figure 5
Clock Frequency		dc	—	1.0	MHz	
LOGIC OUTPUTS	Impedance	—	2.0	3.5	KΩ	I_{out} less than 0.3 mA
	Logic "0"	—	−0.5	−1.0	Volt	I_{out} less than 0.3 mA
	Logic "1"	−11	−12	V_{DD}	Volts	I_{out} less than 0.3 mA
Propagation Delay Plus Rise (t_{dr}) or Fall Time (t_{df})		—	0.7	1.0	uS	
Display Drive Outputs Output On		—	−1.3	−2.0	Volts	1.0 mA to a negative supply
Output Off		—	0.01	5.0	uA	−26 Volts on Output Terminal
Propagation Delay Plus Rise or Fall Time to (TD)		—	2.5	4.0	uS	
Supply Current Drain	I_{GG}	—	4.0	7.5	mA	T_A = 25°C
	I_{DD}	—	4.0	7.5	mA	T_A = 25°C, Excluding external load current

FIGURE 1 — SYNCHRONOUS COUNTING

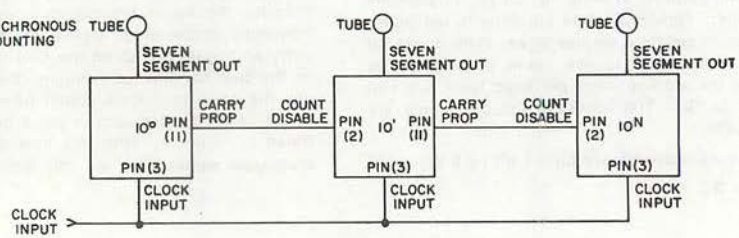


FIGURE 2 —— ASYCHRONOUS COUNTING

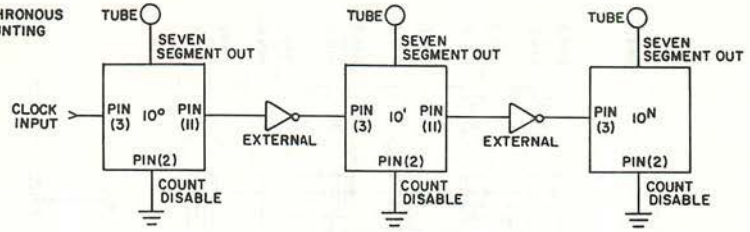


FIGURE 3 —— ASYCHRONOUS COUNTING (UP ONLY)

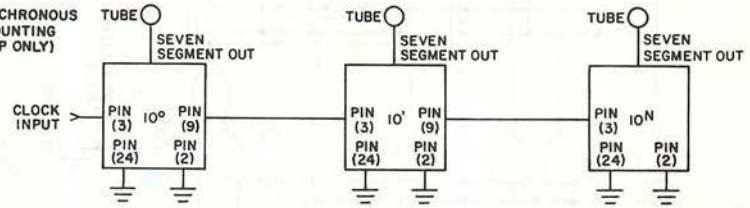


FIGURE 4 —— BLOCK DIAGRAM OF ITT1056

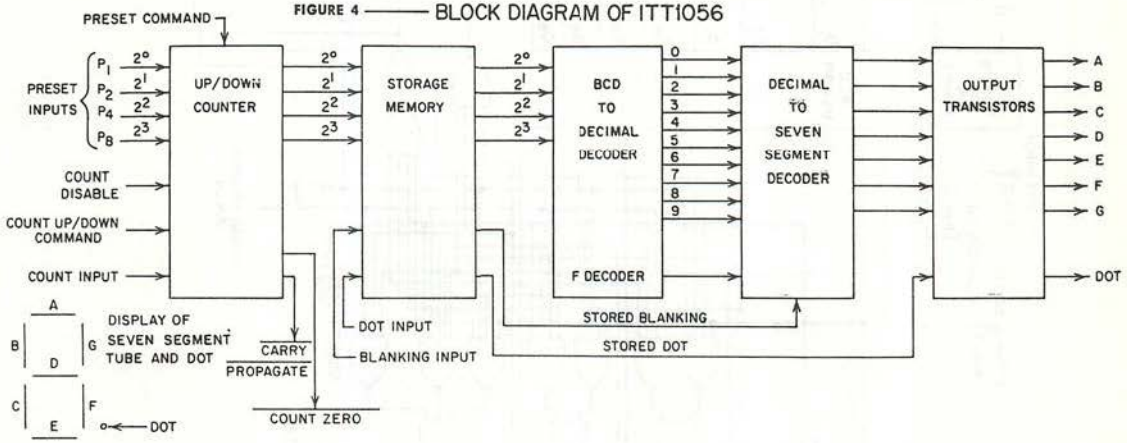
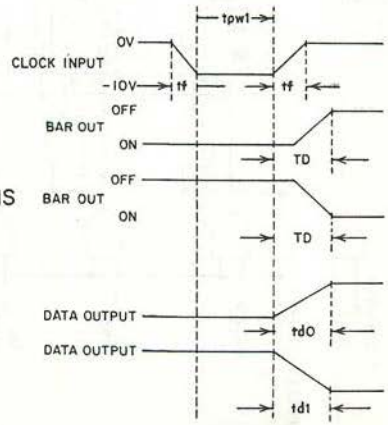


FIGURE 5 —— BAR AND DATA WAVEFORMS



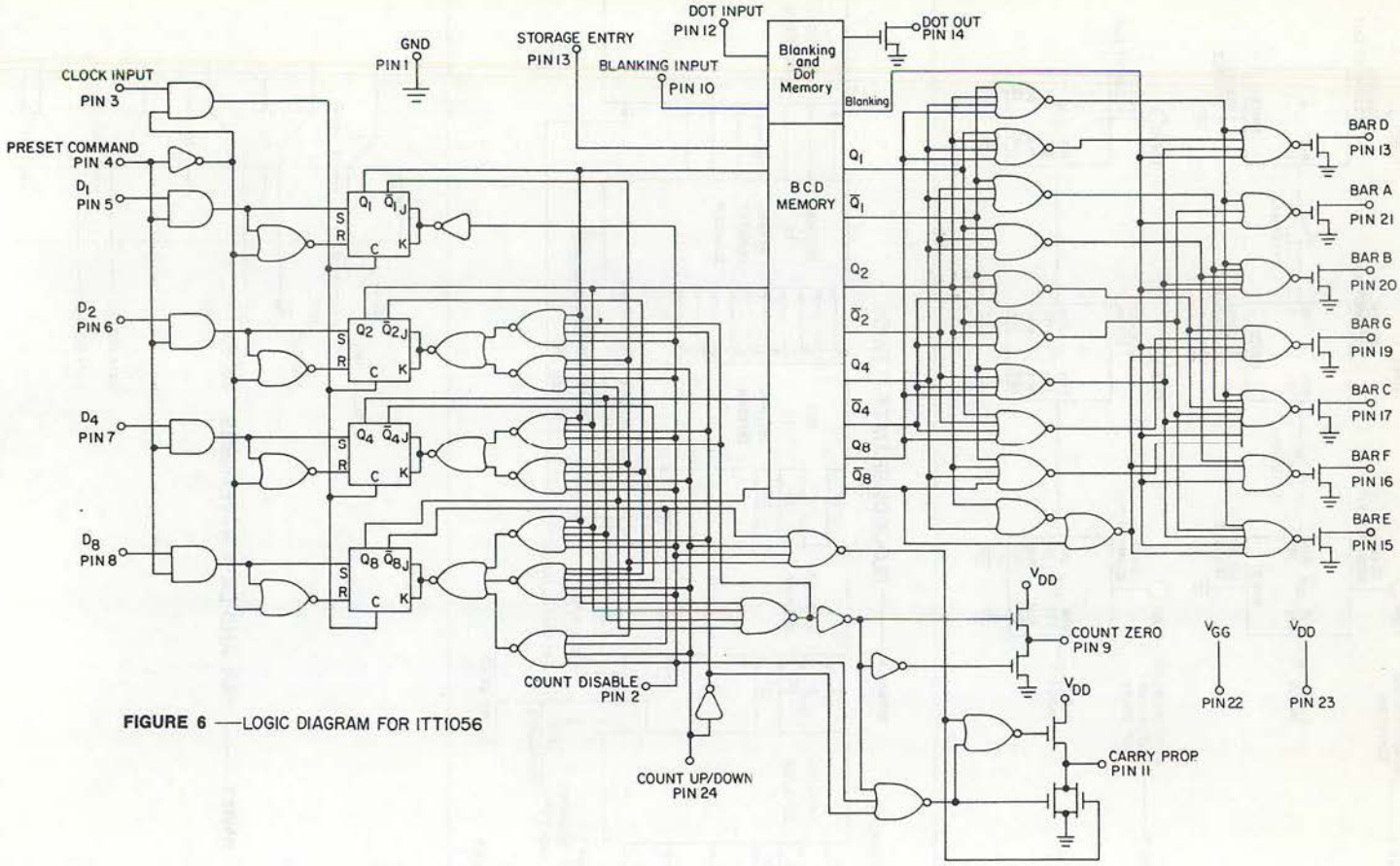


FIGURE 6 —LOGIC DIAGRAM FOR ITT1056

SILICON GATE MOS STATIC SHIFT REGISTER

- Direct Bipolar Compatibility
- 3MHz Operation Guaranteed (Typically 5MHz,-55 c to +125 c)
- 22pF Clockline Capacitance (Max.)
- 1.0mW/Bit Power Dissipation (Max.) including Internal clock Generator
- Input Overvoltage Protection
- 10 Lead TO-100 Package
- Length Selectable to 144,138 or 125 Bits

The ITT1144 is a single selectable 125,138 or 144 bit single-phase static shift register. It is a monolithic integrated circuit utilizing P-channel enhancement mode SILICON GATE MOS technology. The output buffer is capable of driving both low level MOS and bipolar loads directly.

FUNCTIONAL DESCRIPTION – The 1144 is a straight "pipe line" single phase static shift register. Data is accepted at the input when the clock is negative and data is available at the output after the positive going clock transition. The output stage is push-pull, and can sink one TTL load to VDD (1.6mA at 0.4V). Bipolar compatible operation is achieved by connecting VSS to +5.0V, VDD to 0V, and VGG to -12V. Register length of 144, 138, or 125 BITS is determined by the state of control inputs S1 and S2, as defined by the following truth table.

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

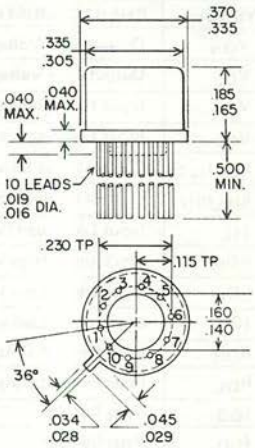
CHARACTERISTICS	UNITS
All inputs including Ø,S1 and S2 (Note 2) . . . −24V to +0.3	V
V_{GG} (Note 2) . . . . . −20V to +0.3	V
V_{DD} and Output (Note 2) . . . . . −7.0V to +0.3	V
Output Current when Output is low (Note 1) 10	mA
Storage Temperature . . . . . −55 C to +150	°C
Operating Temperature . . . . . −55 to +125	°C

Note 1: Low logic level is most negative level and high logic level is most positive level.
Note 2: All voltages with respect to V_{SS}.

TRUTH TABLE

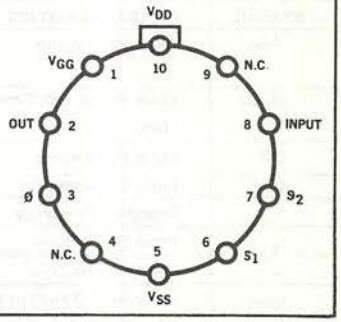
REGISTER LENGTH	S_1	S_2
144	V_{SS}	V_{GG}
138	V_{GG}	V_{GG}
125	V_{SS} or V_{GG}	V_{SS}

PHYSICAL DIMENSIONS

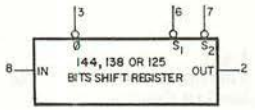


NOTES: LEADS ARE GOLD-PLATED KOVAR
PACKAGE WEIGHT IS 1.32 GRAMS

CONNECTION DIAGRAM
(TOP VIEW)



LOGIC SYMBOL



ORDERING CODE:
ITT1144–5C 0 to 70°C
ITT1144–1C −55 to 125°C

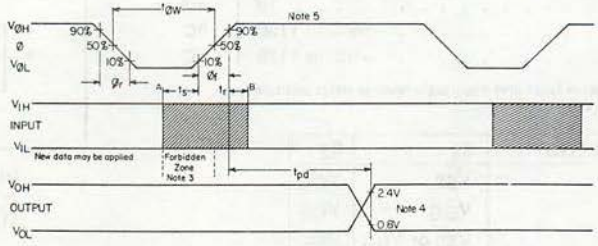
D.C. CHARACTERISTICS (T_A = −55°C to 125°C, V_{SS} = 5.0V±10%, V_{DD}=0V, V_{GG} = −12V±10%)

SYMBOL	CHARACTERISTICS	MIN.	TYP.	MAX.	UNITS	TEST CONDITIONS
V_{OH}	Output High Voltage	V_{SS}−.5		V_{SS}	Volts	I_{OH} = −200uA
V_{OL}	Output Low Voltage			0.4	Volts	I_{OL} = 1.6mA note 1
V_{1H}	Input High Voltage	V_{SS}−1.0		V_{SS}+0.3	Volts	
V_{1L}	Input Low Voltage	V_{GG}		0.80	Volts	
I_{IL6},I_{IL7}	Control Input Low Current			10	uA	V_{6L},V_{7L}=V_{GG},T_A=25°C
I_{IH6},I_{IH7}	Control Input High Current		50	100	uA	V_{6H},V_{7H}=V_{SS},T_A=25°C
I_{1L}	Input Low Load Current			10	uA	V_1=−15.0V,T_A=25°C
$V\emptyset_H$	Clock Input High Voltage	V_{SS}−1.0		V_{SS}+0.3	Volts	
$V\emptyset_L$	Clock Input Low Voltage	−15.0		−10.0	Volts	
$I\emptyset_L$	Clock Input Leakage			10	uA	V$\emptyset$= −15V, T_A=25°C
R_{OH}	Impedance of Output High		1.0	2.5	kohms	I_{out} =200uA
R_{OL}	Impedance of Output Low		180	250	ohms	I_{out}= −1.6mA
I_{GG}	V_{GG} Current		−3.0	−4.5	mA	V_{SS}=5.5V,V_{GG}=−13.2V
I_{DD}	V_{DD} Current		−9	−11.5	mA	$V\emptyset_L$=−13.2
I_{SS}	V_{SS} Current		12	15	mA	T_A=25°C
P_D	Power Dissipation		110	150	mW	Clock Duty Cycle=30%

A.C. CHARACTERISTICS (T_A=−55°C to 125°C,V_{SS}=5.0V ± 10%,V_{DD}=0V,V_{GG}=−12V ± 10%) (See Fig. 1)

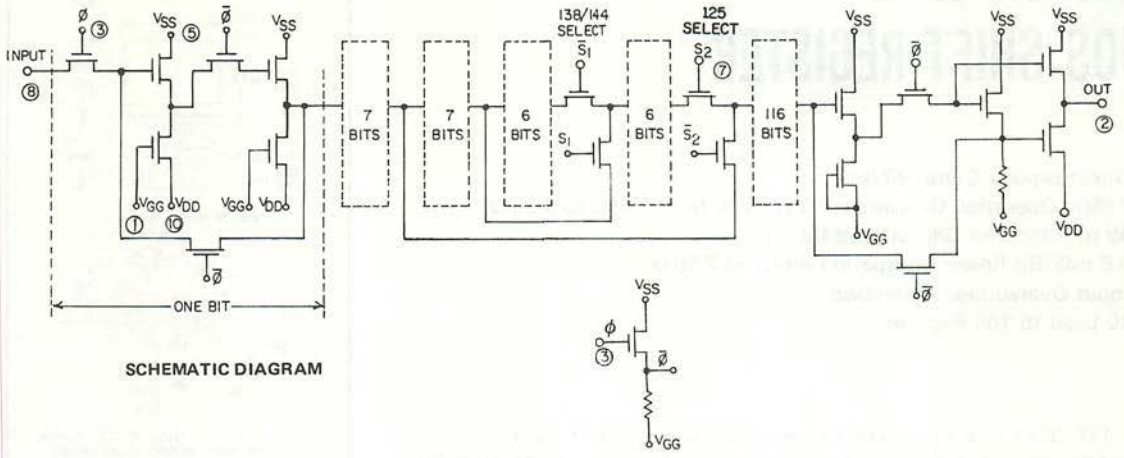
SYMBOL	CHARACTERISTICS	MIN.	TYP.	MAX.	UNITS	TEST CONDITIONS
$t_{\emptyset W}$	Clock Pulse Width	0.1		20	uS	T_A = 70°C
				2	uS	70°C<T_A ≤125°C
$\emptyset_r$,$\emptyset_f$	Clock Rise & Fall Times (10% − 90%)			1.0	uS	
C$\emptyset$	Clock Capacitance		16	22	pF	V_{IN},V$\emptyset$=V_{SS} f=1.0 MHz
CIN	Input Capacitance		4	5		
f	Operating Frequency	D.C.		3.0	MHz	
t_s	Input Set Up Time			50	ns	
t_r	Input Release Time	0			ns	
t_{pd+}	Delay from Ø High to High Level at Output (V_{OH} = 2.4V)			150	ns	C_L = 10pF, Load = 1 DTL Input
t_{pd-}	Delay from Ø High to Low Level at Output (V_{OL} = .8V)			150	ns	C_L = 10pF, Load = 1 DTL Input

Fig. 1
TIMING DIAGRAM
See Test Circut.



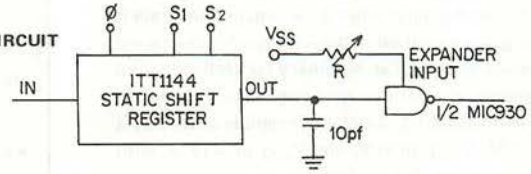
Note 3: A and B define a window during which the input to the shift register is setting up. If the input data changes during this window, the change may or may not be detected. To avoid this ambiguous operation, the input data must remain good between A and B.

Note 4: The outputs remain good until a new output appears.
Note 5: Data is stored indefinitely only when Ø is high.



SCHEMATIC DIAGRAM

PROPAGATION DELAY TEST CIRCUIT



V_{SS} = +4.5V
V_{GG} = −10.8V
V_{DD} = 0V

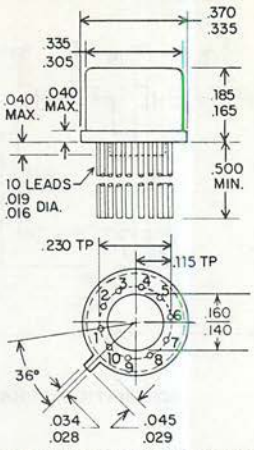
Propagation delay is measured with register output loaded with one DTL gate and a discrete 10pf capacitor. The DTL gate input current is adjusted to 1.6mA by means of a resistor tied between V_{SS} and the gate expander terminal.

ITT3329
512 BIT DYNAMIC SHIFT REGISTER

SILICON GATE MOS SHIFT REGISTER

- **Direct Bipolar Compatibility**
- **2 MHz Operation Guaranteed (Typically from 1 kHz to 4 MHz)**
- **45 pF Clockline Capacitance (Max.)**
- **0.5 mW/Bit Power Dissipation (Max) at 2 MHz**
- **Input Overvoltage Protection**
- **10 Lead to-100 Package**

PHYSICAL DIMENSIONS

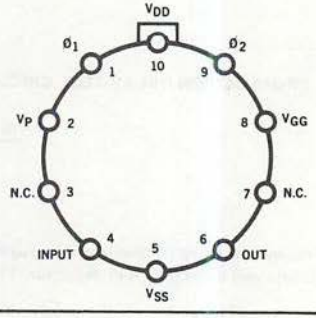


NOTES: LEADS ARE GOLD-PLATED KOVAR
PACKAGE WEIGHT IS 1.32 GRAMS

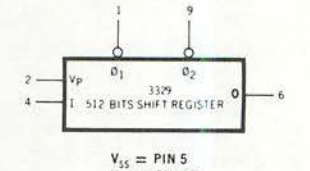
The ITT 3329 is a single 512 bit, two-phase dynamic shift register. It is a monolithic integrated circuit utilizing P-channel enhancement mode SILICON GATE MOS technology. An on-chip input resistor allows direct bipolar compatibility by tying the V_P pin to V_{DD}. The output buffer is capable of driving both low level MOS and bipolar loads directly without addition of an external resistor.

FUNCTIONAL DESCRIPTION – The 3329 is a straight "pipe line" two phase dynamic shift register. The functions ϕ_1 and ϕ_2 are non-overlapping and negative as illustrated in Figure 1. Data is accepted at the input when ϕ_1 is negative and data is available at the output after negative going transition of ϕ_2. The input is connected by a MOS transistor to V_{SS}; this transistor acts as an externally controlled pull-up resistor allowing complete TTL compatibility. The output stage is push-pull, and can sink one TTL load to V_{DD} (1.6 mA at 0.4 V). Bipolar compatible operation is achieved by connecting V_{SS} to +5.0 V, V_{DD} to 0 V, and V_{GG} to −12 V, with V_P, the control pin to the input pull-up resistor tied to V_{DD}.

CONNECTION DIAGRAM
(TOP VIEW)



LOGIC SYMBOL



V_{SS} = PIN 5
V_{DD} = PIN 10
V_{GG} = PIN 8

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

CHARACTERISTICS		UNITS
All Inputs including ϕ_1, ϕ_2 and V_P (Notes 1 & 3)	−24 V to +0.3	V
V_{GG} (Note 3)	−24 V to +0.3	V
V_{DD} and Output (Note 3)	−7.0 V to +0.3	V
Output Current when Output is low (Note 2)	10	mA
Storage Temperature	−55°C to +150	°C
Operating Temperature	0°C to +70	°C

Note 1: V_P must be tied to V_{SS} if data input is between −7 V and −24 V.
Note 2: Low logic level is most negative level and high logic level is most positive level.
Note 3: All voltages with respect to V_{SS}.

ORDERING CODE: ITT3329-5C

D.C. CHARACTERISTICS ($T_A = 0°C$ to $+70°C$, $V_{SS} = 5.0\ V \pm 10\%$, $V_{DD} = 0\ V$, $V_{GG} = -12\ V \pm 10\%$)

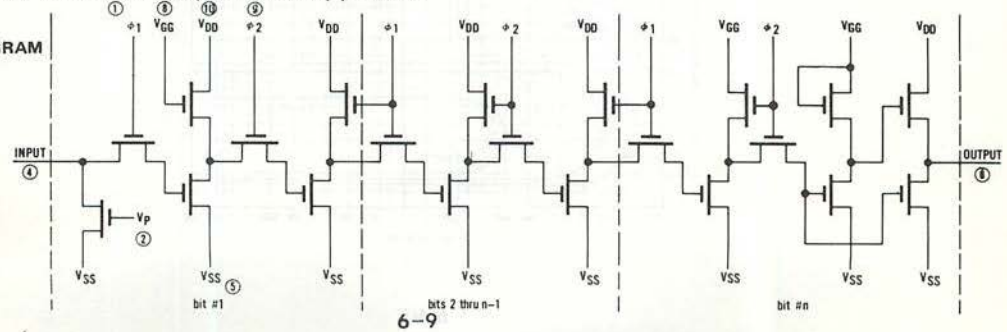
SYMBOL	CHARACTERISTICS	MIN.	TYP.	MAX.	UNITS	TEST CONDITIONS
V_{OH}	Output High Voltage	$V_{SS}-0.6$		V_{SS}	Volts	$I_{OH} = -0.5$ mA
V_{OL}	Output Low Voltage	0	0.24	0.4	Volts	$I_{OL} = 1.6$ mA
V_{IH}	Input High Voltage	$V_{SS}-1.0$			Volts	
V_{IL}	Input Low Voltage	V_{GG}		0.85	Volts	$V_P = V_{SS}$ if V_1 is negative
I_{IH}	Input High Load Current	0.17			mA	$V_1 = V_{SS}-1$, $V_P = V_{DD}$
I_{IL}	Input Low Load Current		1.0	1.60	mA	$V_1 = 0.4\ V$, $V_P = V_{DD}$
I_{IL}	Input Low Load Current			1.0	μA	$V_1 = -5.0\ V$, $V_P = V_{SS}$, $T_A = 25°C$
$V\phi_H$	Clock Input High Voltage	$V_{SS}-1.0$		V_{SS}	Volts	
$V\phi_L$	Clock Input Low Voltage	−6.5		−4.5	Volts	
$I\phi_L$	Clock Input Leakage			1.0	μA	$V\phi = -10\ V$, $T_A = 25°C$
R_{OH}	Impedance of Output High		0.7	1.0	kohms	$V_{OUT} = V_{SS}-0.5\ V$
R_{OL}	Impedance of Output Low		150	250	ohms	$V_{OUT} = V_{OL}$
I_{GG}	V_{GG} Current		−2.4	−3.0	mA	$V_{SS} = 5.5\ V$, $V_{GG} = -13.2\ V$
I_{DD}	V_{DD} Current		−28	−35	mA	$V\phi_L = -6.5\ V$, $T_A = 25°C$, f = 2.0 MHz, $t\phi_w = 200$ ns
I_{SS}	V_{SS} Current		30.4	38	mA	
P_D	Power Dissipation		200	250	mW	

A.C. CHARACTERISTICS ($T_A = 0°C$ to $+70°C$, $V_{SS} = 5.0\ V \pm 10\%$, $V_{DD} = 0\ V$, $V_{GG} = -12\ V \pm 10\%$) (See Fig. 1)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNITS	TEST CONDITIONS
$t\phi_w$	Clock Pulse Width	0.2		100	μs	Note 4
$t\phi_d$	Time Between Clocks	0		100	μs	Note 4
ϕ_r, ϕ_f	Clock Rise & Fall Times (10% - 90%)			1.0	μs	
$C\phi$	Clock Capacitance (Each clockline)			45	pF	$V\phi = V_{SS}$, f = 1.0 MHz
f	Operating Frequency	0.01		2.0	MHz	
t_s	Input Set Up Time			100	ns	
t_r	Input Release Time	0			ns	
t_{pd+}	Delay from ϕ_2 to High Level at Output			150	ns	$C_L = 10$ pF, Load = 1 TTL Input
t_{pd-}	Delay from ϕ_2 to Low Level at Output			150	ns	$C_L = 10$ pF, Load = 1 TTL Input

Note 4: Maximum cycle time $(t\phi_{w1} + t\phi_{d1,2} + t\phi_{w2} + t\phi_{d2,1}) = 100\ \mu s$.

SCHEMATIC DIAGRAM



○ = Pin Number

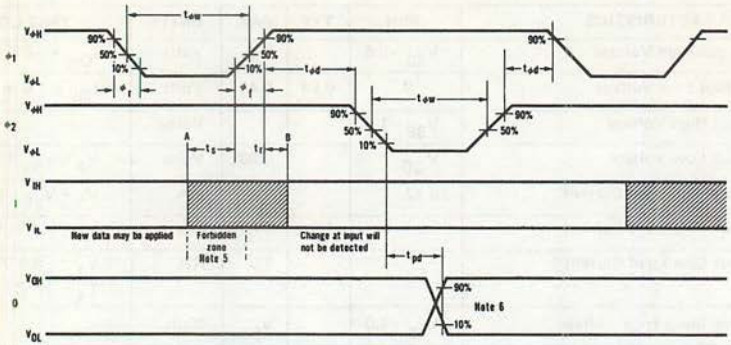


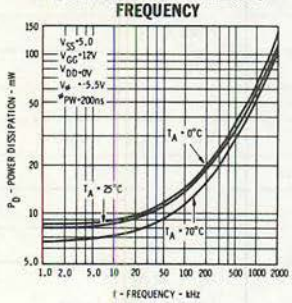
Fig. 1- TIMING DIAGRAM

Note 5: A and B define a window during which the input to the shift register is setting up. If the input data changes during this window, the change may or may not be detected. To avoid this ambiguous operation, the input data must remain good between A and B.

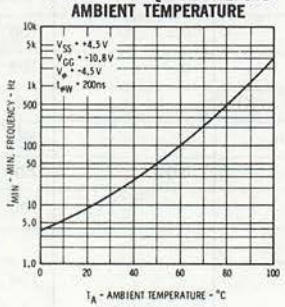
Note 6: The outputs remain good until a new output appears.

TYPICAL ELECTRICAL CHARACTERISTICS

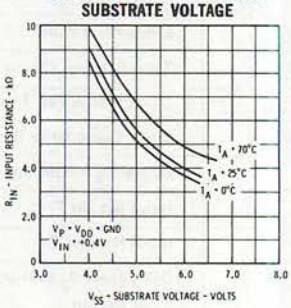
POWER DISSIPATION VERSUS FREQUENCY



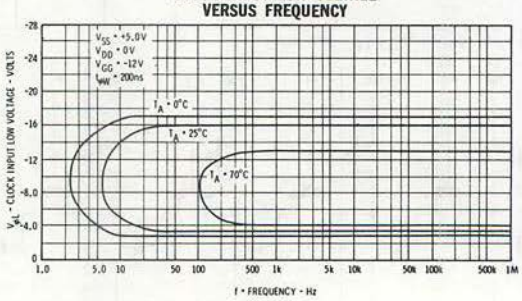
MINIMUM FREQUENCY VERSUS AMBIENT TEMPERATURE



INPUT RESISTANCE VERSUS SUBSTRATE VOLTAGE



CLOCK INPUT LOW VOLTAGE VERSUS FREQUENCY



APPLICATIONS

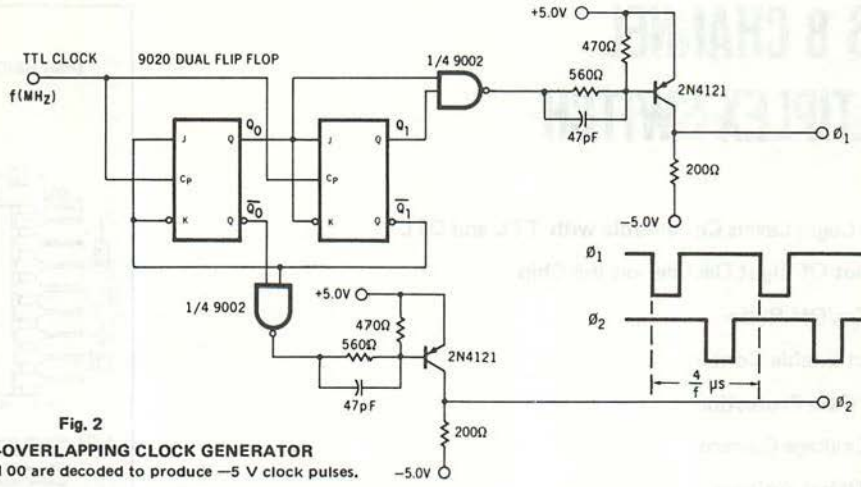


Fig. 2

TWO-PHASE NON-OVERLAPPING CLOCK GENERATOR

The counter states 11 and 00 are decoded to produce −5 V clock pulses.

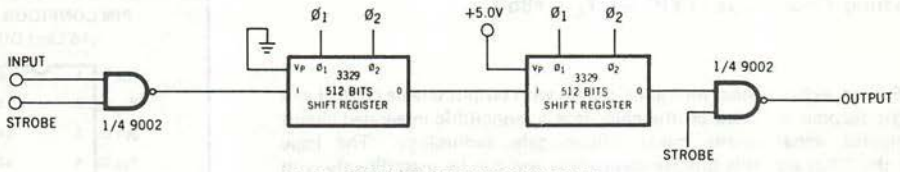


Fig. 3 – SHIFT REGISTER INTERFACE

The shift register inputs may be connected directly to a TTL or DTL output if V_P is tied to ground. If the input is to be driven by a MOS output, V_P is tied to V_{SS}. The output can drive TTL or DTL directly. No external components are required.

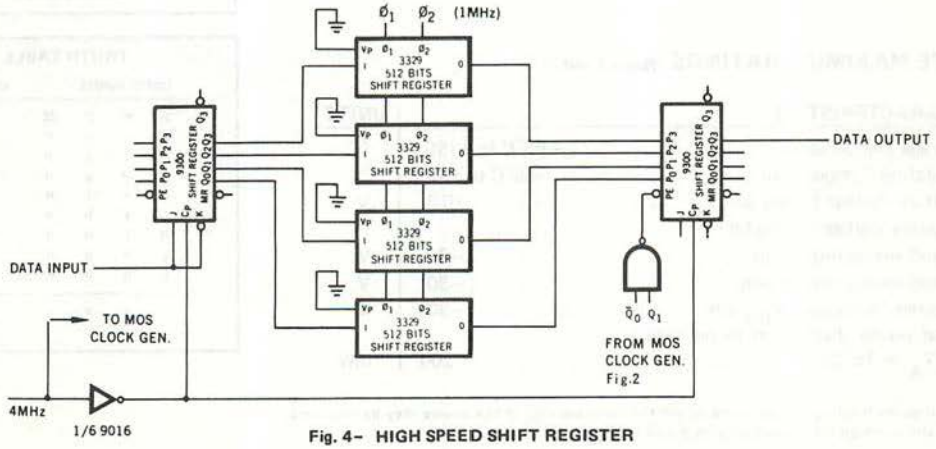


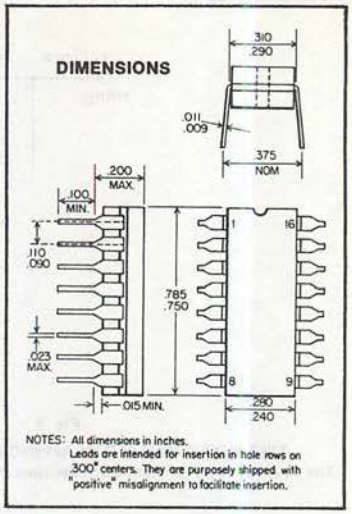
Fig. 4 – HIGH SPEED SHIFT REGISTER

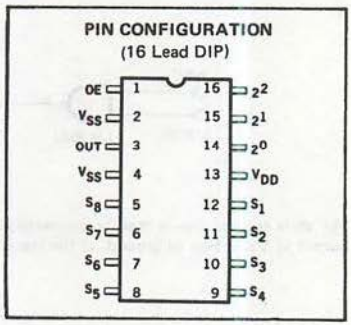
Four shift registers may be connected as shown in the figure above to simulate one long high speed shift register. The 9300 MSI shift register on the left is used as a serial to parallel converter. Data is clocked into the 9300 at four times the clock rate of the silicon-gate shift registers. When four bits have been clocked in, they are loaded into the four long shift registers. At the output of the silicon-gate registers, another 9300 is used to re-serialize the data at the higher clock rate. Because the 9300's add several bits of delay, the system illustrated looks like a high speed 4x512+5 bit register.

Note that the clock period of the 9300's must be greater than the input set up time on the silicon-gate registers.

MOS 8 CHANNEL MULTIPLEX SWITCH

- **Input Logic Levels Compatible with TTL and DTL**
- **One-Out-Of-Eight Decoder on the Chip**
- **High On/Off Ratio**
- **Output Enable Control**
- **Input Gate Protection**
- **Low Leakage Current**
- **Zero Offset Voltage**
- **Fast Switching Time 0.8 μs (TYP) AT T_A = +85°C**





The ITT 3708 is an eight-channel multiplex switch with output enable control and one-out-of-eight decoder included on the chip. It is a monolithic integrated circuit utilizing P-channel enhancement mode silicon gate technology. The logic input lines of the 3708 are NPN bipolar compatible and can be used directly with TTL and DTL 5.0 volt logic levels with no level-shifting interface required. This device is intended for use in A/D converters, multiplexing in analog or digital data transmission systems, and other airborne or ground instrumentation signal routing applications.

ABSOLUTE MAXIMUM RATINGS (Notes 1 and 2)

CHARACTERISTICS		UNITS
Storage Temperature	−65°C to +150	°C
Operating Temperature	−55°C to +85	°C
Positive Voltage on any pin	+0.3	V
Negative Voltage on digital and analog input pins	−30	V
and analog output pins	−30	V
Negative Voltage on V_{DD} pin	−30	V
Total power dissipation in package (T_A = 25°C)	200	mW

NOTES:

(1) These ratings are limiting values above which the serviceability of the device may be impaired.
(2) Voltage ratings are all referenced to pins 2 and 4 (V_{SS}).

TRUTH TABLE

LOGIC INPUTS				CHANNEL
2^0	2^1	2^2	OE	'ON'
L	L	L	H	S_1
H	L	L	H	S_2
L	H	L	H	S_3
H	H	L	H	S_4
L	L	H	H	S_5
H	L	H	H	S_6
L	H	H	H	S_7
H	H	H	H	S_8
X	X	X	L	OFF

ELECTRICAL CHARACTERISTICS

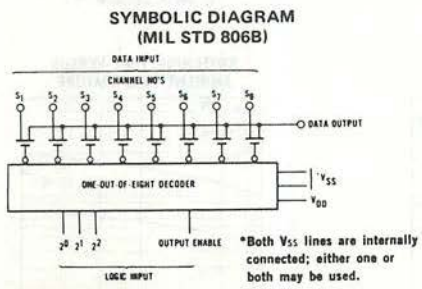
For ITT3708-2D2 $-5.0V<V_{OUT}<+5.0V$, $T_A = 25°C$, $-18\ V<V_{DD}<-20\ V$, $5.0\ V<V_{SS}<6.0\ V$ unless otherwise specified

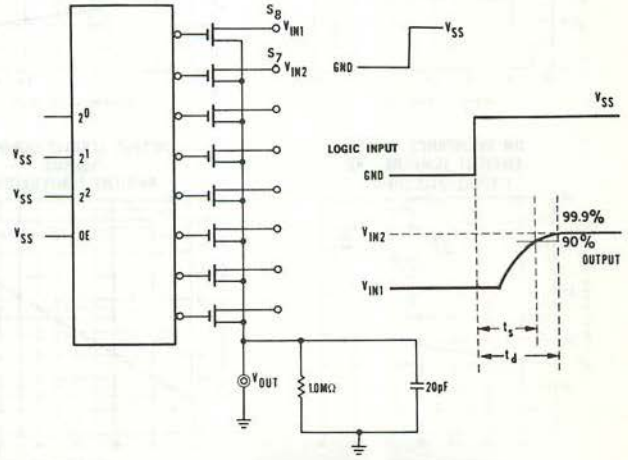
For ITT3708-2D3 $0\ V<V_{OUT}<+5.0\ V$, $T_A = 25°C$, $-18\ V<V_{DD}<-20\ V$, $5.0\ V<V_{SS}<6.0\ V$ unless otherwise specified

SYMBOL	CHARACTERISTICS	MIN.	TYP.	MAX.	UNITS	TEST CONDITIONS
R_{ON}	Data Channel "ON" Resistance					
	2D2		250	400	Ω	$V_{OUT} = -5.0\ V$, $I_{OUT} = -100\ \mu A$
	2D3		190	350	Ω	$V_{OUT} = 0\ V$, $I_{OUT} = -100\ \mu A$
R_{ON}	Data Channel "ON" Resistance		125		Ω	$V_{DD} = -20\ V$, $V_{SS} = +5.0\ V$, $I_{OUT} = -100\ \mu A$
R_{OFF}	Data Channel "OFF" Resistance	1.5	5.0		GΩ	$V_{SS}-V_{OUT} = 15\ V$
I_{LO}	Output Leakage Current		2.0	10	nA	$V_{SS}-V_{OUT} = 15\ V$
I_{LO} (85°)	Output Leakage Current		100	500	nA	$V_{SS}-V_{OUT} = 15\ V$
I_{LDI}	Data Input Leakage Current					
	2D2			3.0	nA	$V_{SS}-V_{IN} = 15\ V$
	2D3			2.0	nA	$V_{SS}-V_{IN} = 10\ V$
I_{LI}	Logic Input Leakage Current			1.0	μA	$V_{SS}-V_{LOGIC\text{-}IN} = 15\ V$
*V_{IL}	Logic Gate Input "Low" Level	V_{DD}		+0.2	V	
*V_{IH}	Logic Gate Input "High" Level	$V_{SS}-1.5$		V_{SS}	V	
t_s	Channel Switching Time (See Fig. 1)		0.45		μs	
t_s (85°C)	Channel Switching Time (See Fig. 1)		0.8	1.5	μs	
t_d	Channel Switching Time (See Fig. 1)		1.0	2.5	μs	
C_{db}	Output Capacitance		25		pF	$V_{SS}-V_{OUT} = 0\ V$, f = 1.0 MHz
C_{is}	Data Input Capacitance		4.5		pF	$V_{SS}-V_{IN} = 0\ V$, f = 1.0 MHz
C_{ig}	Logic Input Capacitance		3.0	175	pF	$V_{SS}-V_{LOGIC\text{-}IN} = 0\ V$, f = 1.0 MHz
P_D	Power Dissipation		130		mW	$V_{DD} = -26\ V$, $V_{SS} = 0\ V$

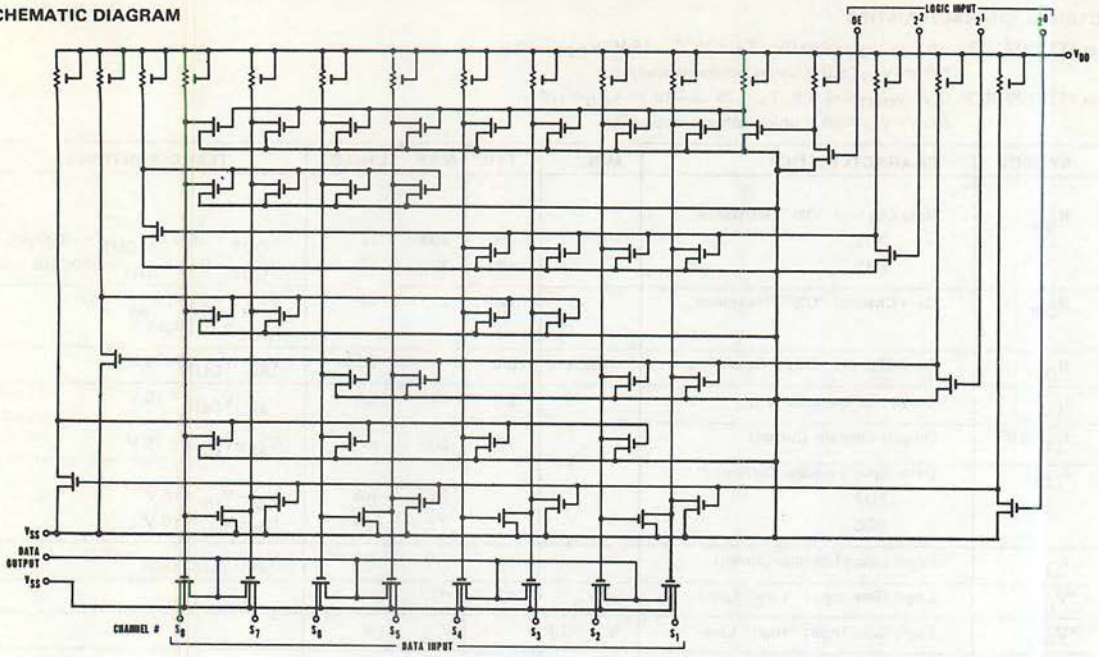
*When driven by DTL and TTL elements, avoid excessive D.C. loading of DTL and TTL elements to insure 3708 logic levels under maximum fan-out conditions. Analog input signal swing should not exceed V_{SS} (= V_{CC}).

Fig. 1— SWITCHING TIME TEST CIRCUIT



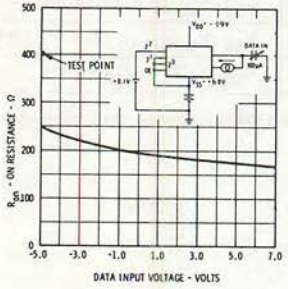


SCHEMATIC DIAGRAM

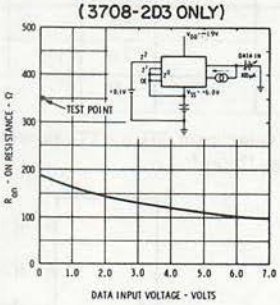


TYPICAL DEVICE CHARACTERISTICS

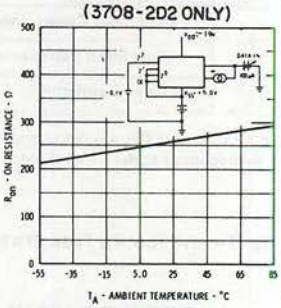
ON RESISTANCE VERSUS DATA INPUT VOLTAGE (3708-2D2 ONLY)



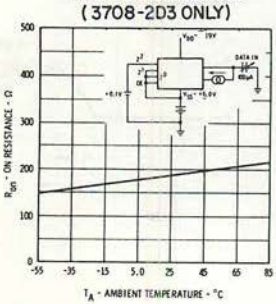
ON RESISTANCE VERSUS DATA INPUT VOLTAGE (3708-2D3 ONLY)



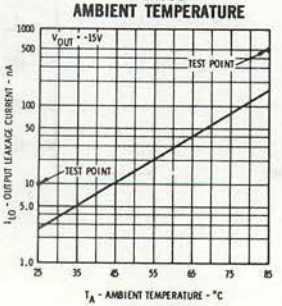
ON RESISTANCE VERSUS AMBIENT TEMPERATURE (3708-2D2 ONLY)



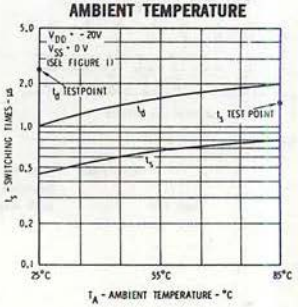
ON RESISTANCE VERSUS AMBIENT TEMPERATURE (3708-2D3 ONLY)

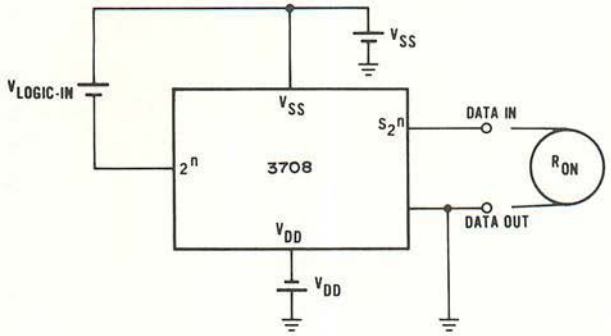


OUTPUT LEAKAGE CURRENT VERSUS AMBIENT TEMPERATURE



SWITCHING TIME VERSUS AMBIENT TEMPERATURE

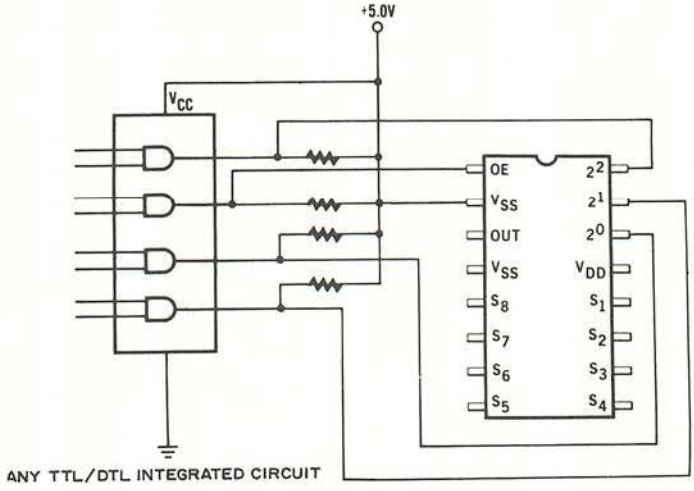




The following sets of power supplies are equivalent:

	CONDITION 1	CONDITION 2
DATA IN	+5.0 V	0 V
V_{SS}	+6.0 V	+1.0 V
V_{DD}	−18 V	−23 V
LOGIC IN		
"Low" Level	+0.2 V	−4.8 V
"High" Level	+5.5 V	+0.5 V

Voltage levels between semiconductor electrodes are normally referenced to one of the electrodes. In MOS, this electrode is the substrate (body or V_{SS}). The voltages can be translated to an equivalent level and referenced to another electrode. In order to measure the 'ON' resistance of the data channel accurately, the data output is at ground potential and all other terminals are changed correspondingly to test worst case conditions.



SPECIAL ORDERING CODE

3708-2D2
Temp. Range: -55°C to +85°C
Input Signal: -5.0to +5.0 Volts

3708-2D3
Temp. Range: -55°C to +85°C
Input Signal: 0 to +5 Volts

3708-5D2
Temp. Range: 0°C to +70°C
Input Signal: -5.0to +5.0 Volts

3708-5D3
Temp. Range: 0°C to +70°C
Input Signal: 0 to +5.0 Volts

ENTERTAINMENT TYPE SELENIUM RECTIFIERS

- Low Cost
- Small Size
- Easy Mounting
- Long Life
- High Voltage

The ITT selenium rectifiers in this catalog cover a wide range of applications. High voltage types lend themselves to compact power supply designs for mobile equipment. The "off-the-line" types are ideal for low-cost half wave and voltage doubler applications in a variety of equipment. Low power applications are especially appropriate for the clip-in types and miniature diodes.

ITT selenium rectifiers are available in several mounting and terminal styles. Miniature diodes and tubular type rectifiers are provided with tinned wire leads and are self-supporting. Open type rectifiers are available in stud and eyelet mounting styles, many can be supplied with clip-in mountings. These rectifiers can be supplied with conventional solder terminals, printed wiring board terminals or plug-in terminals.

ITT's vacuum disposition technique produces selenium rectifiers with extremely long life and minimum change in initial characteristics.

APPLICATIONS

- Horizontal phase discriminator
- Diode matrix assemblies
- Oscilloscopes
- Gate circuits
- Wave shaping networks
- Modulators and demodulators
- Power supplies
- Hi-fi equipment
- DC motor control
- Electric appliances

CLIP TYPE 6H65F
(actual size)

CARTRIDGE TYPE 676H100BCIT
(half size)

OPEN PLATE TYPE 1263B
(actual size)

MINIATURE TYPE 1215
(actual size)

MINIATURE TYPE K1615C
(actual size)

HIGH VOLTAGE CARTRIDGE TYPE SELENIUM RECTIFIERS

CHARACTERISTICS

PIV	Rating (mA)	DIMENSIONS (inches)					ITT Part No.
		Rectifier Dim.		Cell Dia.	Lead Dim.(1)		
		Dia.	Length		Dia.	Length	
4650	2	7/32	3-9/32	1/8	.031 (2)	1½	665H100ABI
4650	2	7/32	2-1/8	1/8	.031 (2)	1½	665H100ABIT
4650	4	9/32	3-9/32	3/16	.031 (2)	1½	676H100ABI
4650	4	9/32	2-1/8	3/16	.031 (2)	1½	676H100ABIT
4650	6.5	13/32	3-9/32	9/32	.040(2)	1½	647H100ABI
4650	6.5	13/32	2-1/8	9/32	.040(2)	1½	647H100ABIT
4650	2	15/64	3-1/2	1/8	.031	1½	665H100BCI
4650	2	15/64	2-11/32	1/8	.031	1½	665H100BCIT
4650	4	19/64	3-1/2	3/16	.031	1½	676H100BCI
4650	4	19/64	2-11/32	3/16	.031	1½	676H100BCIT
4650	6.5	3/8	3-1/2	9/32	.031	1½	647H100BCI
4650	6.5	3/8	2-11/32	9/32	.031	1½	647H100BCIT
4650	15	39/64	3-23/32	1/2	.031	1½	629H100BCI
4650	15	39/64	2-9/16	1/2	.031	1½	629H100BCI
4650	25	15/16	3-23/32	3/4	.031	1½	630H100BCI
4650	25	15/16	2-9/16	3/4	.031	1½	630H100BCIT

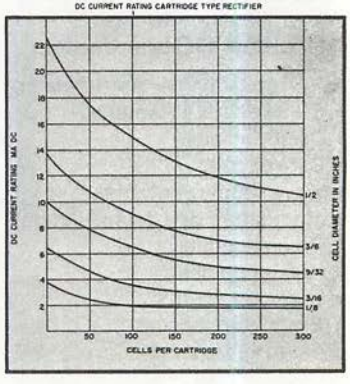
NOTES: 1. Solder type terminals or radial leads also available.
2. Silver plated metal end ferrules.

HOW TO ORDER HIGHER VOLTAGE TYPES

Voltage ratings are available in 46.5 volt increments up to many thousands of volts. Contact ITT Semiconductors for applications assistance.

HOW TO CALCULATE CURRENT RATINGS

Current rating depends upon cell area and the number of cells in series. The curves at the right give the necessary information. The AB series of rectifiers in the characteristics table above have a maximum current rating of 10 mA in a half wave circuit. The BC series has a maximum current rating of 45 mA in a half wave circuit.



OFF-THE-LINE HALF WAVE SELENIUM RECTIFIERS

SPECIFICATIONS

Rated Input Voltage ..... 117 Volts RMS
Maximum Input Voltage ..... 130 Volts RMS
Maximum Inverse Voltage ..... 380 Volts Peak
Maximum Output Current ..... As Listed
Maximum RMS Current ..... 2.7 Times DC Rating
Maximum Peak Current ..... 10 Times DC Rating
Minimum Series Resistance ..... As Listed
Maximum Cell Operating Temperature ..... 85°C

DIMENSIONS

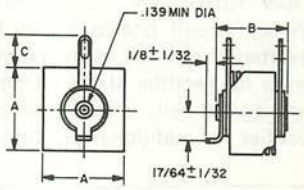


FIGURE 1

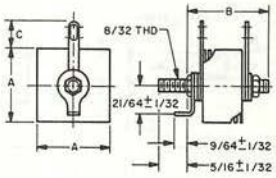


FIGURE 2

CHARACTERISTICS

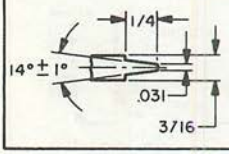
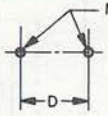
Max. Output (mA) DC	Dimensions (inches) Fig. No.	Cell Size (A)	Mtg Dim. (B) Max.	Term. Hgt (C) Max.	Series Resist. (Min.)	ITT Part No.
10		3/8 Dia. x 11/16 long, with axial wire leads 1-5/16 long			47	1158
15		3/8 Dia. x 11/16 long, with axial wire leads 1-5/16 long			47	5152
20		1/2 Dia. x 11/16 long, with axial wire leads 1-5/16 long			47	1159
30		1/2 Dia. x 11/16 long, with axial wire leads 1-5/16 long			47	5153
65	1	1	9/16	21/64	22	1002A
	1	1	9/16	13/32	22	1444(1)
	1	11/16	23/32	31/64	22	1263A
	1	11/16	21/32	9/16	22	1526(1)
	—	11/16	BKT MTD	31/64	22	1263B
75	1	1	3/4	21/64	22	1003A
	1	1	3/4	13/32	22	1445(1)
	1	11/16	21/32	31/64	22	6H75AE
100	1	1-1/4	3/4	25/64	22	1004A
	1	1	1-1/8	21/64	22	1101A
	1	1	1-1/8	13/32	22	1504(1)
	1	1	3/4	21/64	7.5	6H100AE
150	1	1-1/4	1	25/64	15	1005A
	1	1	1-1/8	21/64	7.5	6H150AE
200	1	1-1/2	1	31/64	4.7	1006A
	2	1	2	21/64	4.7	6H200A
250	1	1-1/2	1-1/8	31/64	4.7	1028A
	1	1-1/4	1-1/4	25/64	4.7	6H250AE
300	2	1-1/2	2-7/32	19/32	4.7	1090A
	1	1-1/4	1-13/32	25/64	4.7	6H300AE
350	2	1-3/4	2-7/32	19/32	4.7	1023A
	2	1-5/8	2-7/32	17/32	4.7	1356A
	2	1-1/4	2	25/64	4.7	6H350A
400	2	1-3/4	2-1/4	19/32	4.7	1277A
	1	1-1/2	1-1/2	31/64	4.7	6H400AE
450	2	2	2-7/32	15/32	4.7	1021A
	2	1-1/2	2-7/32	31/64	3.3	6H450A
500	2	2	2-7/32	15/32	4.7	1179A
	2	1-3/4	1-13/16	19/32	3.3	6H500A
600	2	2	2-1/2	15/32	4.7	1289A
	2	1-3/4	2	19/32	3.3	6H600A
750	2	2	2	15/32	3.3	6H750A

NOTE: Rectifier terminals designed for mounting in a printed circuit board. The "B" dimension listed here is the overall length; see page 4 for mounting information.

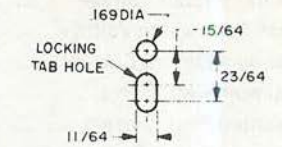
OFF-THE-LINE HALF WAVE SELENIUM RECTIFIERS, continued

MOUNTING DETAILS

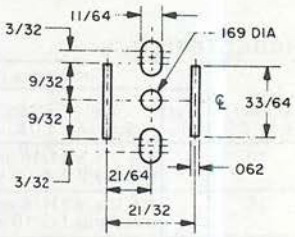
Taper Tip Design . . . for maximum ease of insertion in heavy-gauge printed circuit boards up to ⅛" thick. The tapered terminal may be inserted into round, diamond-shaped, or rectangular holes. Taper design keeps the rectifier plates off the board. As a result, the flow of cooling air through the cells is improved, and extra board area is freed beneath the rectifier for additional printing.

Mounting Detail	Terminal Detail	Rectifier Code No.	Dimension "D"
		1444	5/16
		1445	15/32
		1504	7/8
		1526	13/32

MOUNTING HOLES

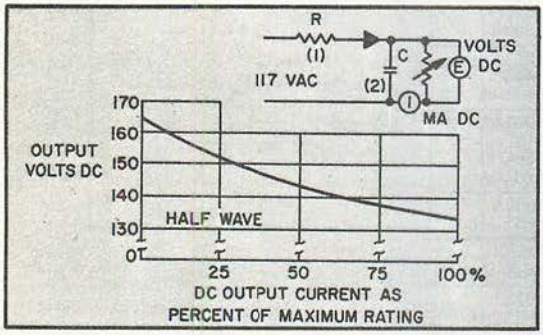


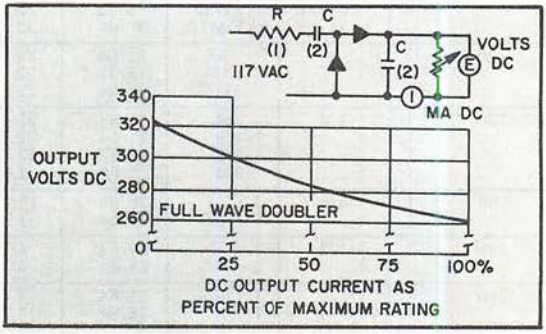
Mounting hole layout for stud and eyelet rectifiers.

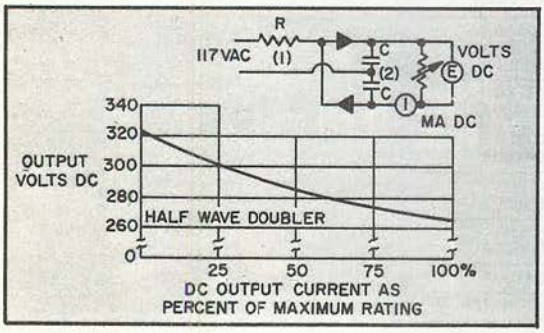


Mounting hole layout for clip mounted rectifiers; will also permit mounting of stud type rectifiers.

CIRCUIT DIAGRAMS and TYPICAL VOLTAGE REGULATION CURVES







NOTES:

1. Minimum series resistance specified in characteristics table.
2. Minimum filter capacitance in MFD to be ½ rectifier rating in milliamperes.

CLIP TYPE SELENIUM RECTIFIERS

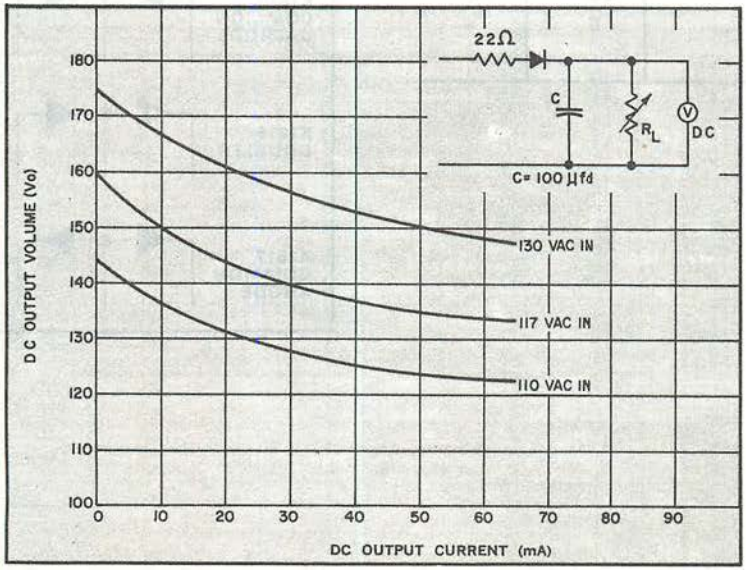
CHARACTERISTICS FOR CAPACITIVE LOAD

Nominal RMS Input Voltage	117
Maximum RMS Input Voltage	130
Maximum Peak Reverse Voltage	380
Maximum Peak Current (mA)	650
Maximum RMS Current (mA)	175
Maximum DC Output Current (mA)	65
Minimum Recommended Series Resistance (Ohms)	22
Maximum Cell Operating Temperature (°C)	85
Maximum Forward Voltage Drop (dc)	10
Dielectric Strength (Volts for 1 Min.)	900
Output Voltage with 117 Volts Input and 100 μf Capacitor and 65 mA dc (Volts)	130

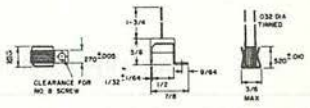
ENVIRONMENTAL CHARACTERISTICS

Humidity—Withstands 120 hours in 95% +RH at 65°C.

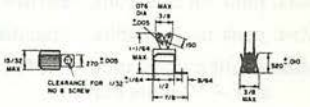
Vibration—Withstands 10 to 55 cps., .060″ displacement for 2 hours in each plane.



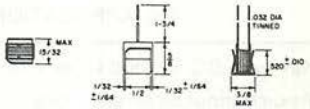
DIMENSIONS



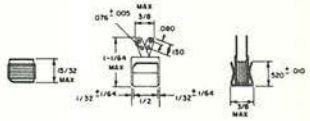
6H65HW



6H65F



6H65FW



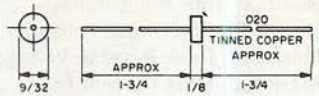
6H65H

MINIATURE SELENIUM DIODES

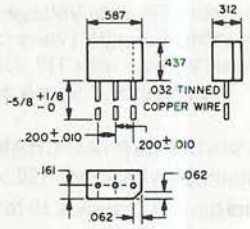
CHARACTERISTICS

AC APPLICATIONS	ITT Part No. 1215	ITT Part No. K1615AC K1616AC K1617AC
Max. DC forward current (mA)	.25	—
Max. peak forward current (mA)	2.5	—
Max. RMS input volts, resistive load	40	—
Max. peak reverse volts, resistive load	56	—
Max. peak reverse volts, capacitive load	68	—
*Max. shunt capacitance in $\mu\mu$f at 1 kc and —10 volts bias	—	50
Max. shunt capacitance unbalance ($\mu\mu$f)	—	5
Max. shunt capacitance in $\mu\mu$f at 200 kc	22	—
Max. ambient temperature	55°C	85°C
DC APPLICATIONS		
Max pure DC forward current (mA)	.37	.15
Max. continuous reverse volts	30	20
Max. reverse current at 40 volts (μA)	6	—
Max. reverse current at 20 volts (μA)	—	4

DIMENSIONS

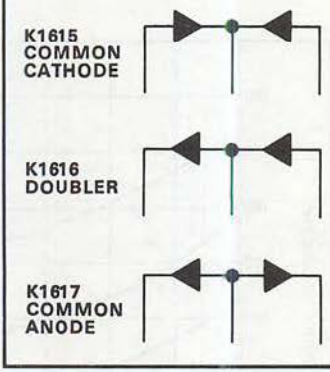


ITT Part Nos.
K1615AC, K1616AC, K1617AC



ITT Part No. 1215

ELECTRICAL CONNECTIONS



SELENIUM CONTACT PROTECTOR RECTIFIERS

- AC or DC Applications
- Low Cost
- Easy to Install
- Small Size
- Rugged Construction

These ITT selenium cells have been specifically processed for contact protector applications. Their long life, low leakage current and reliable operation provide a low-cost solution to arcing problems in switched inductive devices.

These circuit protectors prevent arcing by effectively suppressing the voltage surges which normally occur during switching. This eliminates the undesirable by-products of arcing, such as contact pitting and erosion, undesirable electrical noise, false triggering of adjacent control circuits or possible insulation breakdown.

ITT selenium cells may be used in a back-to-back arrangement on devices breaking either AC or DC circuits. In AC applications, each arm normally contains the same number of cells; for DC use, a different number of cells is generally specified for each arm.

TYPICAL APPLICATIONS

- Relays
- Stepping Switches
- Electromagnets
- Solenoids
- Small Motors
- Electric Clutches
- Telephone Switching Equipment
- Automobile Clocks & Horns
- Telemetering Equipment
- Magnetic Chucks
- Thermostats
- Electric Brakes
- Solenoid Valves
- Computers

ORDERING INFORMATION

Explanation of part number codes

8A4 P S 1

- 1 — No. of cells in position "A"
- S — "S" indicates DC suppressor
- A — "A" indicates AC suppressor
- P — "P" indicates paper tube
- H — "H" indicates hermetic seal

102 S 2 E X 1

- 1 — No. of cells in position "B"
- X — Finish
- E — No. of cells in position "A"
- S — "S" indicates DC suppressor
- A — "A" indicates AC suppressor

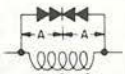


FIG. A

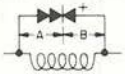


FIG. B

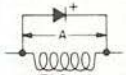


FIG. C

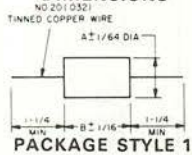
A=BLOCKING SECTION
B=SUPPRESSOR SECTION

Special finishes

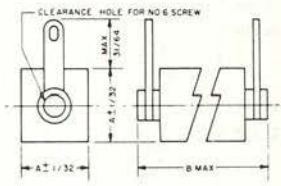
Package style 1 is supplied in a paper tube or in a hermetically sealed can which meets MIL specifications for environmental exposure. Package styles 2, 3 and 4 are supplied with a commercial protective finish. To order special finishes replace the **"X"** in the part number with letters as follows:

"Y" for humidity and salt spray protection
"W" for heavy duty industrial protection
"YF" for humidity, salt spray and fungus protection

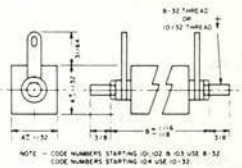
DIMENSIONS

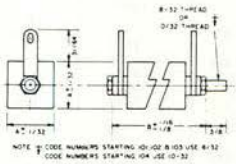


PACKAGE STYLE 1



PACKAGE STYLE 2


PACKAGE STYLE 3


PACKAGE STYLE 4

CHARACTERISTICS

DC APPLICATIONS — 10 BREAKS / SECOND MAX

DC Voltage Range	Max. DC Coil Current mA	Coil Current For 300V Max. Rise mA	ITT Part No.	Package Style	Dimensions A	Dimensions B	ITT Part No.	Package Style	Dimensions A	Dimensions B
0-30	500		8A1PS0	1	25/64	5/8	8A1HS0*	1	1/2	29/32
	1000		15A1PS0	1	1/2	5/8	15A1HS0*	1	9/16	29/32
0-22	1750		101S1EX0	2	11/16	3/8	101S1AX0	4	11/16	9/16
	4700		102S1EX0	2	1	3/8	102S1AX0	4	1	9/16
	9000		103S1EX0	2	1-1/4	11/32	103S1AX0	4	1-1/4	5/8
	14000		104S1EX0	2	1-17/32	11/32	104S1AX0	4	1-17/32	11/16
31-60	500		8A2PS0	1	25/64	5/8	8A2HS0*	1	1/2	29/32
	1000		15A2PS0	1	1/2	5/8	15A2HS0*	1	9/16	29/32
23-44	1750		101S2EX0	2	11/16	1/2	101S2AX0	4	11/16	11/16
	4700		102S2EX0	2	1	1/2	102S2AX0	4	1	11/16
	9000		103S2EX0	2	1-1/4	1/2	103S2AX0	4	1-1/4	11/16
	14000		104S2EX0	2	1-17/32	1/2	104S2AX0	4	1-17/32	13/16
61-90	500		8A3PS0	1	25/64	5/8	8A3HS0*	1	1/2	29/32
	1000		15A3PS0	1	1/2	5/8	15A3HS0*	1	9/16	29/32
45-66	1750		101S3EX0	2	11/16	9/16	101S3AX0	4	11/16	11/16
	4700		102S3EX0	2	1	5/8	102S3AX0	4	1	27/32
	9000		103S3EX0	2	1-1/4	5/8	103S3AX0	4	1-1/4	13/16
	14000		104S3EX0	2	1-17/32	5/8	104S3AX0	4	1-17/32	31/32
91-120	500		8A4PS0	1	25/64	3/4	8A4HS0*	1	1/2	1-1/32
	1000		15A4PS0	1	1/2	3/4	15A4HS0*	1	9/16	1-1/32
67-88	1750		101S4EX0	2	11/16	5/8	101S4AX0	4	11/16	13/16
	4700		102S4EX0	2	1	11/16	102S4AX0	4	1	7/8
	9000		103S4EX0	2	1-1/4	3/4	103S4AX0	4	1-1/4	15/16
	14000		104S4EX0	2	1-17/32	23/32	104S4AX0	4	1-17/32	1
121-150	500		8A5PS0	1	25/64	3/4	8A5HS0*	1	1/2	1-1/32
	1000		15A5PS0	1	1/2	5/8	15A5HS0*	1	9/16	1-1/32
89-110	1750		101S5EX0	2	11/16	3/4	101S5AX0	4	11/16	1
	4700		102S5EX0	2	1	7/8	102S5AX0	4	1	1-1/16
	9000		103S5EX0	2	1-1/4	1	103S5AX0	4	1-1/4	13/32
	14000		104S5EX0	2	1-17/32	1	104S5AX0	4	1-17/32	1-3/16
151-180	500		8A6PS0	1	25/64	3/4	8A6HS0*	1	1/2	1-1/32
	1000		15A6PS0	1	1/2	15/16	15A6HS0*	1	9/16	1-1/32
111-132	1750		101S6EX0	2	11/16	1	101S6AX0	4	11/16	1-1/16
	4700		102S6EX0	2	1	1	102S6AX0	4	1	1-1/8
	9000		103S6EX0	2	1-1/4	1	103S6AX0	4	1-1/4	1-1/4
	14000		104S6EX0	2	1-17/32	1-1/8	103S6AX0	4	1-17/32	1-5/16
181-210	500		8A7PS0	1	25/64	15/16	8A7HS0*	1	1/2	1-7/32
	1000		15A7PS0	1	1/2	13/16	15A7HS0*	1	9/16	1-7/32
133-154	1750		101S7EX0	2	11/16	1	101S7AX0	4	11/16	1-1/8
	4700		102S7EX0	2	1	1	102S7AX0	4	1	1-1/4
	9000		103S7EX0	2	1-1/4	1-1/2	103S7AX0	4	1-1/4	1-3/8
	14000		104S7EX0	2	1-17/32	1-1/8	104S7AX0	4	1-17/32	1-7/16
211-240	500		8A8PS0	1	25/64	13/16	8A8HS0*	1	1/2	1-7/32
	1000		15A8PS0	1	1/2	13/16	15A8HS0*	1	9/16	1-7/32
155-176	1750		101S8EX0	2	11/16	1-1/8	101S8AX0	4	11/16	1-3/16
	4700		102S8EX0	2	1	1-5/32	102S8AX0	4	1	1-5/16
	9000		103S8EX0	2	1-1/4	1-1/4	103S8AX0	4	1-1/4	1-7/16
	14000		104S8EX0	2	1-17/32	1-1/4	104S8AX0	4	1-17/32	1-1/2
241-270	500		8A9PS0	1	25/64	15/16	8A9HS0*	1	1/2	1-7/32
	1000		15A9PS0	1	1/2	15/16	15A9HS0*	1	9/16	1-7/32
177-198	1750		101S9EX0	2	11/16	1-1/8	101S9AX0	4	11/16	1-1/4
	4700		102S9EX0	2	1	1-1/4	102S9AX0	4	1	1-15/32
	9000		103S9EX0	2	1-1/4	1-3/8	103S9AX0	4	1-1/4	1-9/16
	14000		104S9EX0	2	1-17/32	1-3/8	103S9AX0	4	1-17/32	1-3/8
271-300	500	375	8A10PS0	1	25/64	15/16	8A10HS0*	1	1/2	1-7/32
	1000	750	15A10PS0	1	1/2	15/16	15A10HS0*	1	9/16	1-7/32
199-220	1750	1300	101S10EX0	2	11/16	1-1/4	101S10AX0	4	11/16	1-5/16
	4700	3500	102S10EX0	2	1	1-3/8	102S10AX0	4	1	1-1/2
	9000	6750	103S10EX0	2	1-1/4	1-1/2	103S10AX0	4	1-1/4	1-5/8
	14000	11000	104S10EX0	2	1-17/32	1-1/2	104S10AX0	4	1-17/32	1-11/16
301-330	500	275	8A11PS0	1	25/64	1-1/8	8A11HS0*	1	1/2	1-13/32
	1000	550	15A11PS0	1	1/2	1-1/8	15A11HS0* *	1	9/16	1-13/32
221-242	1750	950					101S11AX0	3	11/16	1-5/8
	4700	2600					102S11AX0	3	1	1-13/16
	9000	5000					103S11AX0	3	1-1/4	2
	14000	7750					104S11AX0	3	1-17/32	2-1/16
331-360	500	125	8A12PS0	1	25/64	1-1/8	8A12HS0*	1	1/2	1-13/32
	1000	250	15A12PS0	1	1/2	1-1/8	16A12HS0*	1	9/16	1-13/32
243-264	1750	450					101S12AX0	3	11/16	1-9/16
	4700	1200					102S12AX0	3	1	1-13/16
	9000	2250					103S12AX0	4	1-1/4	2
	14000	3500					104S12AX0	3	1-17/32	2-1/16

mA FOR 300 VOLT RISE EXCEEDS MAX. CURRENT RATING

NOTE: Hermetically sealed tubular construction to meet MIL specifications for environmental exposure.

DC APPLICATIONS — 40 BREAKS / SECOND MAX

DC Voltage Range	Max. DC Coil Current mA	Coil Current For 300V Max. Rise mA	ITT Part No.	Package Style	Dimensions A	Dimensions B	ITT Part No.	Package Style	Dimensions A	Dimensions B
0-30	250	mA FOR 300 VOLT RISE EXCEEDS MAX. CURRENT RATING	8A1PS1	1	25/64	5/8	8A1HS1*	1	1/2	29/32
	600		15A1PS1	1	1/2	5/8	15A1HS1*	1	9/16	29/32
0-22	850		101S1EX1	2	11/16	15/32	101S1AX1	4	11/16	5/8
0-22	2250		102S1EX1	2	1	15/32	102S1AX1	4	1	25/32
	4300		103S1EX1	2	1-1/4	17/32	103S1AX1	4	1-1/4	3/4
	6600		104S1EX1	2	1-17/32	17/32	104S1AX1	4	1-17/32	13/16
31-60	250		8A2PS1	1	25/64	5/8	8A2HS1*	1	1/2	29/32
	600		15A2PS1	1	1/2	5/8	15A2HS1*	1	9/16	29/32
23-44	850		101S2EX1	2	11/16	9/16	101S2AX1	4	11/16	1-3/16
	2250		102S2EX1	2	1	9/16	102S2AX1	4	1	29/32
	4300		103S2EX1	2	1-1/4	17/32	103S2AX1	4	1-1/4	3/4
	6600		104S2EX1	2	1-17/32	19/32	104S2AX1	4	1-17/32	7/8
61-90	250		8A3PS1	1	25/64	3/4	8A3HS1*	1	1/2	1-1/32
	600		15A3PS1	1	1/2	3/4	15A3HS1*	1	9/16	1-1/32
45-66	850		101S3EX1	2	11/16	17/32	101S3AX1	4	11/16	1
	2250		102S3EX1	2	1	9/16	102S3AX1	4	1	1-1/32
	4300		103S3EX1	2	1-1/4	23/32	103S3AX1	4	1-1/4	25/32
	6600		104S3EX1	2	1-17/32	23/32	104S3AX1	4	1-17/32	1
91-120	250		8A4PS1	1	25/64	3/4	8A4HS1*	1	1/2	1-1/32
	600		15A4PS1	1	1/2	3/4	15A4HS1*	1	9/16	1-1/32
67-88	850		101S4EX1	2	11/16	21/32	101S4AX1	4	11/16	1
	2250		102S4EX1	2	1	1	102S4AX1	4	1	1
	4300		103S4EX1	2	1-1/4	1	103S4AX1	4	1-1/4	1-1/16
	6600		104S4EX1	2	1-17/32	3/4	104S4AX1	4	1-17/32	1-1/8
121-150	250		8A5PS1	1	25/64	3/4	8A5HS1*	1	1/2	1-1/32
	600		15A5PS1	1	1/2	3/4	15A5HS1*	1	9/16	1-1/32
89-110	850		101S5EX1	2	11/16	13/16	101S5AX1	4	11/16	1-1/16
	2250		102S5EX1	2	1	7/8	102S5AX1	4	1	1-1/8
	4300		103S5EX1	2	1-1/4	1-1/8	103S5AX1	4	1-1/4	1-1/4
	6600		104S5EX1	2	1-17/32	1-1/8	104S5AX1	4	1-17/32	1-3/8
151-180	250		8A6PS1	1	25/64	15/16	8A6HS1*	1	1/2	1-7/32
	600		15A6PS1	1	1/2	15/16	15A6HS1*	1	9/16	1-7/32
111-132	850		101S6EX1	2	11/16	1	101S6AX1	4	11/16	1-1/8
	2250		102S6EX1	2	1	1	102S6AX1	4	1	1-1/4
	4300		103S6EX1	2	1-1/4	1-1/8	103S6AX1	4	1-1/4	1-3/8
	6600		104S6EX1	2	1-17/32	1-1/8	104S6AX1	4	1-17/32	1-7/16

DC Voltage Range	Max. DC Coil Current mA	Coil Current For 300V Max. Rise mA	ITT Part No.	Package Style	Dimensions A	Dimensions B	ITT Part No.	Package Style	Dimensions A	Dimensions B
181-210	250	mA FOR 300 VOLT RISE EXCEEDS MAX. CURRENT RATING	8A7PS1	1	25/64	15/16	8A7HS1*	1	1/2	1-7/32
	600		15A7PS1	1	1/2	15/16	15A7HS1*	1	9/16	1-7/32
133-154	850		101S7EX1	2	11/16	1-1/8	101S7AX1	4	11/16	1-3/16
	2250		102S7EX1	2	1	31/32	102S7AX1	4	1	1-5/16
	4300		103S7EX1	2	1-1/4	1-1/4	103S7AX1	4	1-1/4	1-7/16
	6600		104S7EX1	2	1-17/32	1-1/4	104S7AX1	4	1-17/32	1-9/16
211-240	250	250	8A8PS1	1	25/64	15/16	8A8HS1*	1	1/2	1-7/32
	600	600	15A8PS1	1	1/2	15/16	15A8HS1*	1	9/16	1-7/32
155-176	850	850	101S8EX1	2	11/16	1-1/8	101S8AX1	4	11/16	1-1/4
	2250	2250	102S8EX1	2	1	1-1/4	102S8AX1	4	1	1-7/16
	4300	4300	103S8EX1	2	1-1/4	1-3/8	103S8AX1	4	1-1/4	1-9/16
	6600	6600	104S8EX1	2	1-17/32	1-1/4	104S8AX1	4	1-17/32	1-5/8
241-270	250	120	8A9PS1	1	25/64	15/16	8A9HS1*	1	1/2	1-7/32
	600	300	15A9PS1	1	1/2	15/16	15A9HS1*	1	9/16	1-7/32
177-198	850	500	101S9EX1	2	11/16	1-1/4	101S9AX1	4	11/16	1-15/16
	2250	1350	102S9EX1	2	1	1-3/8	102S9AX1	4	1	1-1/2
	4300	2600	103S9EX1	2	1-1/4	1-1/2	103S9AX1	4	1-1/4	1-5/8
	6600	4000	104S9EX1	2	1-17/32	1-1/2	104S9AX1	4	1-17/32	1-3/4
271-300	250	100	8A10PS1	1	25/64	1-1/8	8A10HS1*	1	1/2	1-13/32
	600	250	15A10PS1	1	1/2	1-1/8	15A10HS1*	1	9/16	1-13/32
199-220	850	450					101S10AX1	3	11/16	1-5/8
	2250	1125					102S10AX1	3	1	1-13/16
	4300	4150					103S10AX1	3	1-1/4	1-7/8
	6600	3300					104S10AX1	3	1-17/32	2-1/16
301-330	250	50	8A11PS1	1	25/64	1-1/8	8A11HS1*	1	1/2	1-13/32
	600	125	15A11PS1	1	1/2	1-1/8	15A11HS1*	1	9/16	1-13/32
221-242	850	210					101S11AX1	3	11/16	1-5/8
	2250	560					102S11AX1	3	1	1-7/8
	4300	1100					103S11AX1	3	1-1/4	2
	6600	1650					104S11AX1	3	1-17/32	2-1/16
331-360	250	10	8A12PS1	1	25/64	1-1/8	8A12HSA*	1	1/2	1-13/32
	600	25	15A12PS1	1	1/2	1-1/16	15A12HS1*	1	9/16	1-13/32
243-264	850	45					101S12AX1	3	11/16	1-5/8
	2250	110					102S12AX1	3	1	1-7/8
	4300	215					103S12AX1	3	1-1/4	2-1/16
	6600	330					104S12AX1	3	1-17/32	2-3/16

AC APPLICATIONS

DC Voltage Range	Max. DC Coil Current mA	Coil Current For 300V Max. Rise mA	ITT Part No.	Package Style	Dimensions A	Dimensions B	ITT Part No.	Package Style	Dimensions A	Dimensions B
0-26	200	mA FOR 300 VOLT RISE EXCEEDS MAX. CURRENT RATING	8A1PA1	1	25/64	5/8	8A1HA1*	1	1/2	29/32
	400		15A1PA1	1	1/2	5/8	15A1HA1*	1	9/16	29/32
	600		101A1EX1	2	11/16	15/32	101A1AX1	4	11/16	11/16
	1600		102A1EX1	2	1	15/32	102A1AX1	4	1	25/32
	3000		103A1EX1	2	1-1/4	1/2	103A1AX1	4	1-1/4	3/4
	4700		104A1EX1	2	1-17/32	17/32	104A1AX1	4	1-17/32	13/16
27-52	200	200	8A2PA2	1	25/64	5/8	8A2HA2*	1	1/2	1-1/32
	400	400	15A2PA2	1	1/2	3/4	15A2HA2*	1	9/16	1-1/32
	600	600	101A2EX2	2	11/16	1/2	101A2AX2	4	11/16	23/32
	1600	1600	102A2EX2	2	1	11/16	102A2AX2	4	1	1-1/32
	3000	3000	103A2EX2	2	1-1/4	11/16	103A2AX2	4	1-1/4	7/8
	4700	4700	104A2EX2	2	1-17/32	23/32	104A2AX2	4	1-17/32	1
53-78	200	60	8A3PA3	1	25/64	3/4	8A3HA3*	1	1/2	1-1/32
	400	140	15A3PA3	1	1/2	3/4	15A3HA3*	1	9/16	1-1/32
	600	250	101A3EX3	2	11/16	13/16	101A3AX3	4	11/16	27/32
	1600	650	102A3EX3	2	1	7/8	102A3AX3	3	1	1-7/16
	3000	1200	103A3EX3	2	1-1/4	1-3/16	103A3AX3	4	1-1/4	1-1/4
	4700	2000	104A3EX3	2	1-17/32	1	104A3AX3	4	1-17/32	1-5/16

DC Voltage Range	Max. DC Coil Current mA	Coil Current For 300V Max. Rise mA	ITT Part No.	Package Style	Dimensions A	Dimensions B	ITT Part No.	Package Style	Dimensions A	Dimensions B
79-104	200	15	8A4PA4	1	25/64	15/16	8A4HA4*	1	1/2	1-7/32
	400	35	15A4PA4	1	1/2	15/16	15A4HA4*	1	9/16	1-7/32
	600	60	101A4EX4	2	11/16	29/32	101A4AX4	3	11/16	1-3/16
	1600	160	102A4EX4	2	1	31/32	102A4AX4	4	1	29/32
	3000	300	103A4EX4	2	1-1/4	1-5/32	103A4AX4	4	1-1/4	1-1/4
	4700	470	104A4EX4	2	1-17/32	1-5/32	104A4AX4	4	1-17/32	1-1/2
105-130	200	10	8A5PA5	1	25/64	15/16	8A5HA5*	1	1/2	1-7/32
	400	20	15A5PA5	1	1/2	15/16	15A5HA5*	1	9/16	1-7/32
	600	30	101A5EX5	2	11/16	1-1/8	101A5AX5	4	11/16	1-1/8
	1600	80	102A5EX5	2	1	1-11/32	102A5AX5	3	1	1-5/8
	3000	150	103A5EX5	2	1-1/4	1-1/4	103A5AX5	4	1-1/4	1-7/16
	4700	250	104A5EX5	2	1-17/32	1-13/32	104A5AX5	3	1-17/32	1-7/8

NOTE: Hermetically sealed tubular construction to meet MIL specifications for environmental exposure.

CAUSE OF CONTACT ARCING

Consider the circuit shown in **Figure 1.** Close the circuit contacts S_1 and the current flow as indicated by the ammeter M_1 builds up to 400 mA. The flow of current has set up a magnetic field through the core. Electrical energy has been stored in the magnetic field by the current, analogous to the mechanical energy stored in a spring by compression.

Now open the contacts S_1 thus breaking the steady flow of current. Just as the compressed spring will start to release its stored mechanical energy, the magnetic field starts to collapse, releasing its stored energy. While the magnetic field is collapsing it induces a voltage in the coil that acts to maintain the current through the coil in the same direction as the original current which built up the field. The magnitude of this induced voltage is equal to the product of the coil current, and the coil and circuit resistance; and it can attain very high values since the circuit resistance approaches infinity with the switch contacts open.

Theoretically, when the flow of current is suddenly stopped by the opening of S_1, the voltage that appears across the coil could go up to infinity. Approximately 300 volts is required to produce arcing across contacts in free air. Since air is not a perfect insulator, the instant that S_1 is opened and the high induced voltage appears across the contacts, an arc occurs. In typical applications, air breakdown across the contacts will limit the voltage rise to the region of 300 to 1,000 volts in an average 24-volt coil circuit. **See Figure 2.**

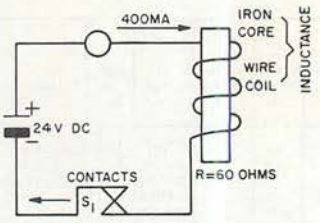


FIG. 1

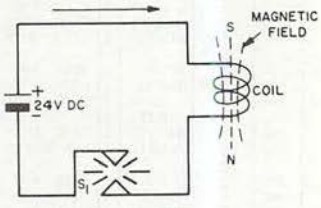


FIG. 2

HOW ITT SELENIUM CONTACT PROTECTORS WORK

Half-wave configuration for DC applications

Consider the circuit of **Figure 3,** showing contact protector cell A connected across the coil terminals. While contacts S_1 are held closed a current of 400 milliamperes flows through the coil, but no part of the coil current flows through the contact protector. When S_1 is opened coil current flows in the low-resistance direction of the contact protector, thus dissipating the energy stored in the coil through the resistance of the coil and contact protector. As the resistance of the contact protector is very low, usually a fraction of the coil resistance, the voltage across the contacts rises only slightly, to a few volts above battery voltage.

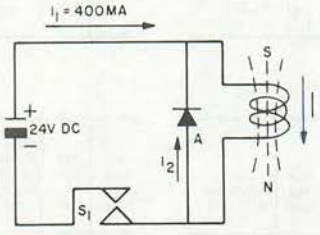


FIG. 3

Half-wave configuration, continued

In the circuit shown in **Figure 4,** cell B has been added in such a direction as to oppose the discharge current I_2. A semiconductor cell has the unique characteristic of exhibiting decreasing resistance with increasing voltage in the blocking direction.

At the instant switch S_1 is opened, the induced voltage rises to approximately 150 volts, due to the blocking action of cell B. This induced voltage is indicated in **Figure 4** and appears as a reverse voltage across cell B, i.e., the high-resistance direction.

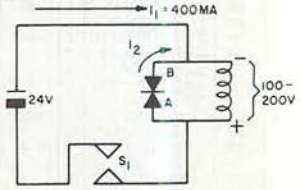


FIG. 4

Figure 5 shows the change in reverse resistance with application of reverse voltage to a typical semiconductor contact-protector cell. At the working voltage of 24 volts, the reverse resistance is approximately 1 megohm. When S_1 is opened, the voltage across the coil builds up to approximately −200 volts. At this voltage the reverse resistance of cell B will be less than 500 ohms. Much of the stored energy is dissipated in this low-resistance region of the cell characteristic.

As the energy is dissipated and the current decreases, the induced voltage also decreases. The remainder of the stored energy is dissipated in a higher-resistance region than initially. For example, as the induced voltage decays to −25 volts, the cell resistance rises to approximately one megohm.

Thus the effect of the nonlinear resistance of cell B is to provide, at the instant of switching, a path of relatively low resistance to prevent the induced voltage from rising to a value which will cause arcing. As the stored energy is dissipated the low resistance increases, due to the nature of the cell characteristics, and provides a damping effect on the discharge current. The result is to reduce the coil release time as compared to the action of the half-wave-type contact protector.

Figure 6. Oscillograph trace voltage across a set of contacts breaking the circuit of a 48-volt telephone relay, without contact protection. Sparking begins at 300 volts (see oscillations), continues as contacts are separated and rises to a voltage peak at 500 volts. Voltage decay is exponential.

Figure 7. Oscillograph trace of voltage across same set of contacts, protected by ITT half-wave semiconductor contact protector.

Figure 8. Oscillograph trace of voltage across same set of contacts, protected by ITT back-to-back semiconductor contact protector.

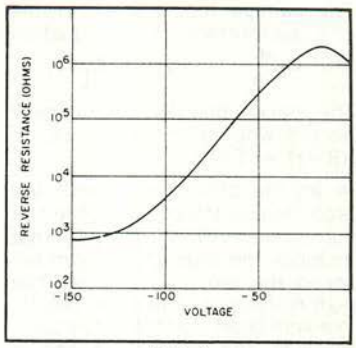


FIG. 5

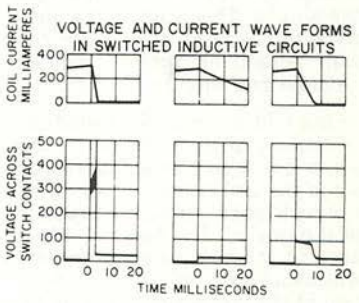


FIG. 6 FIG. 7 FIG. 8

Back-to-back configuration for AC applications

The back-to-back configuration is readily adapted to use in AC circuits by providing the same number of cells in each arm of the device. The number of cells in series per arm will depend on the applied AC voltage. The requirement for the same number of cells in each arm arises from the fact that both arms alternately are required to block the input voltage. This arrangement differs from the DC back-to-back configuration in which one arm has sufficient cells to block the battery voltage and the other has only one or two cells to provide the surge suppression.

Factors relating to the opening of inductive circuits

It can be shown mathematically that the time required for the coil current to drop to zero, after the switch contacts have opened, is inversely proportional to the sum of the coil resistance and protector resistance. Also, the magnitude of the voltage induced in the coil at the instant of switching is directly proportional to the sum of these resistances.

When the circuit energizing an inductance is opened the polarity of the voltage across the coil is reversed and is indicated by the equation $E = -L\frac{di}{dt}$

After the circuit opens, and assuming no arcing occurs, the time for the current to fall to a percentage of its initial value is given by the following equation:

$$t = \frac{-L}{R_L + r} \frac{\log i}{\overline{EI}}$$

When R = Coil resistance
r = Forward resistance of rectifier
L = Inductance of coil
t = Time for current to decrease to i
i = Current at time t
I = Steady-state current through the coil
E = Supply voltage

The voltage induced across the coil is expressed by the equation

$$V = -L\frac{di}{dt} = (R_L + r)\, I_\varepsilon - \frac{R_L + r}{L}t$$

The maximum value of voltage V occurs when $t = 0$ V max. $= I(R+r) = E + Ir$

In an inductive circuit with unprotected switch contacts, the coil current decays through a path that includes the widening air gap between the moving contacts. The high resistance of this gap results in a very short current decay time. However, the voltage induced in the coil at the instant of switching must reach a value high enough to force the current across the air gap. This leads to the electrical breakdown of the air gap with attendant arcing, contact damage and electrical noise.

In the half-wave configuration the resistance of the protector is low when it is acting as a suppressor, since the coil current flows in the low-resistance forward direction of the device. The forward resistance of the half-wave suppressor will usually be only a small fraction of the coil resistance and, for practical purposes, may be regarded as a short circuit around the coil. The low value of protector resistance prevents the induced voltage from rising more than a volt or two over the battery voltage, and increases the current decay time compared to the decay time of a coil with unprotected contacts.

In the back-to-back configuration the reverse resistance of the protector is inversely proportional to the induced voltage. This resistance will be the smallest at the instant of switching and will increase in value as the current decreases. This nonlinear resistance characteristic causes the induced voltage to rise to a value higher than it would reach in a circuit using the half-wave configuration, but it prevents the induced voltage from attaining the contact-damaging values existing in a circuit with unprotected contacts. Although the current decay time is increased somewhat compared to the decay time of a coil with unprotected contacts, it is very appreciably shorter than the decay time of a circuit using the half-wave configuration.

APPLICATION NOTES

Voltage Range

The words "voltage range" are used because the maximum voltage rating increases in discrete steps, according to the number of blocking cells in series. Each protector has a maximum permissible voltage rating which is the low-voltage end of the range for the next higher voltage group.

Max. Coil Current – mA

The maximum permissible coil current is based on the thermal dissipation characteristics of the contact protector when operated at maximum coil voltage and repetition rate.

Coil Current for 300-V Max. Rise – mA

At the instant of switching, the current through the protector is the same as the coil current, and the induced voltage at the coil terminals will rise to the value required to drive this current through the protector. This voltage will add to the supply voltage and appear across the contacts. Sparking at the contacts will be minimized if the sum of these two voltages does not exceed 300 volts, and this requirement is met if the induced voltage is no greater than the difference between 300 and the supply voltage. This condition is achieved by reducing, for a given cell size, the permissible coil current as the supply voltage increases. Thus, it will be observed that the coil current for 300-volt rise will be less than the maximum coil current for many of the higher-voltage units. Conversely, the coil current for 300-volt rise is so great that it exceeds the maximum coil current for the low-voltage units. These protectors carry the note in the rating table "MA for 300-Volt Rise Exceeds Max. Current Rating"; this means that operation at the listed maximum coil current will give a voltage rise of less than 300 volts at the contacts.

The current values listed in the column "Coil Current for 300-V Max. Rise" are representative values, based on the observation of typical relays and solenoids. The specific value of current that will limit the voltage at the contacts to 300 volts is a function of the coil design, the size of the coil, the number of turns of wire, etc., and it is possible for a contact protector to furnish adequate spark suppression when used with coils carrying currents greater than those listed; but the maximum current rating should not be exceeded. For this reason, it is wise to observe the action and efficiency of the protector before freezing a design. Samples and engineering assistance are available upon written request to the Engineering Department.

In selecting a suitable Contact Protector from the list in this data sheet, it should be noted:

Ratings are based upon operation in typical inductive circuits at temperatures of 50°C or lower. Current ratings given in the column headed "Coil Steady State Current for 300 volt max. rise" represent the rating of the protector to limit the voltage rise across the contacts to approximately 300 volts. This rating may be exceeded if a rise in excess of 300 volts is permissible, but the maximum peak current rating should not be exceeded. The voltage rating should not be exceeded under any circumstances.

Fast Contact Action

Rate of operation of contacts in the range 10 to 40 breaks per second. The back-to-back arrangement of the ITT Contact Protector provides adequate arc suppression with a negligible effect upon the release time of the relay. The protectors are fated for applications where the rate of operation of the contacts is in the range of 10 to 40 breaks per second. ITT should be consulted for recommendations if the rate of operation exceeds 40 breaks per second.

TRANSIENT VOLTAGE SUPPRESSOR RECTIFIERS

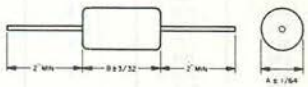
- **AC Input or DC Applications**
- **Improve Equipment Reliability**
- **Reduce Equipment Cost**

ITT transient voltage suppressors eliminate one of the major causes of failure of semiconductor rectifiers by instantaneously short-circuiting transient voltages in excess of the ratings of the rectifiers. They permit the circuit designer to use rectifiers with lower PIV ratings, thereby reducing equipment cost. These specially processed selenium cells have very sharp "zener" breakdown characteristics when operated in the reverse direction. Since the reverse characteristic is used instead of the forward characteristic, aging has very little effect on the resistance and suppressing voltage level of the protector. The small effects of aging and temperature variations have been taken into consideration in the volt-ampere curves and tabulated characteristics.

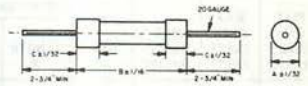
In inductive circuits using mechanical switches, these suppressors can be used to eliminate pitting of the switch contacts by absorbing the high peak voltages generated when the switch is opened. ITT contact protector selenium rectifiers can also be used in this application.

Transient voltage suppressors can be mounted by eyelets or studs in stack types and by clips or pigtail leads in tubular types. Stack types are supplied with a standard industrial finish or with a moisture resistant finish for protection against salt spray and humidity.

DIMENSIONS



PAPER TUBE TYPE



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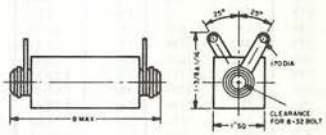
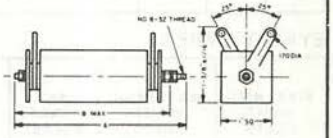


EYELET TYPE



STUD TYPE

RATINGS

CHARACTERISTICS	8A SERIES	25A SERIES	102 SERIES	UNITS
Steady State RMS Volts/Cell	30	30	25	Volts
Peak Volts/Cell	42.4	42.4	35	Volts
DC Volts/Cell	20	20	20	Volts
Stack RMS Volts	30-600	36-600	25-500	Volts
Stack DC Volts	20-400	20-400	20-320	Volts
Steady State Leakage Current (max.)	0.8	1.2	12	mA
Single Pulse Current (4 milliseconds) (max.)	0.75	2	8	Amps
Recurrent Pulse Current (1 millisecond @ 60 cps) (max.)	0.25	0.75	3	Amps
Ambient Temperature	—20 to +100	—20 to +100	—20 to +100	°C
Cell Operating Temperature (max.)	130	130	130	°C
Construction	Tubular	Tubular	Stud or Eyelet	

ELECTRICAL AND MECHANICAL CHARACTERISTICS – AC INPUT TYPES

PAPER TUBE TYPES

MAX. RMS INPUT VOLTS	MAX. PEAK INPUT VOLTS	MAX. ZENER VOLTS[1]	DIMENSIONS DIA. (A)	DIMENSIONS LENGTH (B)	ITT PART NO.
30	42	104	3/8	27/32	8A1PG1
60	85	208	3/8	27/32	8A2PG2
90	127	312	3/8	27/32	8A3PG3
120	170	416	3/8	27/32	8A4PG4
150	212	519	3/8	27/32	8A5PG5
180	254	623	3/8	1 3/32	8A6PG6
210	297	727	3/8	1 3/32	8A7PG7
240	339	831	3/8	1 3/32	8A8PG8
270	382	934	3/8	1 3/32	8A9PG9
300	424	1039	3/8	1 3/32	8A10PG10
330	467	1143	3/8	1 21/64	8A11PG11
360	509	1247	3/8	1 21/64	8A12PG12
390	551	1350	3/8	1 21/64	8A13PG13
420	594	1454	3/8	1 21/64	8A14PG14
450	636	1558	3/8	1 21/64	8A15PG15
480	679	1663	3/8	1 37/64	8A16PG16
510	721	1766	3/8	1 37/64	8A17PG17
540	764	1870	3/8	1 37/64	8A18PG18
570	806	1974	3/8	1 37/64	8A19PG19
600	848	2078	3/8	1 37/64	8A20PG20

MAX. RMS INPUT VOLTS	MAX. PEAK INPUT VOLTS	MAX. ZENER VOLTS[2]	DIMENSIONS DIA. (A)	DIMENSIONS LENGTH (B)	ITT PART NO.
30	42	87	37/64	1 1/64	25A1PG1
60	85	177	37/64	1 1/64	25A2PG2
90	127	266	37/64	1 1/64	25A3PG3
120	170	354	37/64	1 1/64	25A4PG4
150	212	443	37/64	1 1/64	25A5PG5
180	254	532	37/64	1 1/4	25A6PG6
210	297	620	37/54	1 1/4	25A7PG7
240	339	709	37/64	1 1/4	25A8PG8
270	382	798	37/64	1 1/4	25A9PG9
300	424	886	37/64	1 1/4	25A10PG10
330	467	975	37/64	1 1/2	25A11PG11
360	509	1063	37/64	1 1/2	25A12PG12
390	551	1152	37/64	1 1/2	25A13PG13
420	594	1241	37/64	1 1/2	25A14PG14
450	636	1329	37/64	1 1/2	25A15PG15
480	679	1417	37/64	1 3/4	25A16PG16
510	721	1507	37/64	1 3/4	25A17PG17
540	764	1595	37/64	1 3/4	25A18PG18
570	806	1684	37/64	1 3/4	25A19PG19
600	848	1772	37/64	1 3/4	25A20PG20

PHENOLIC TUBE TYPES

MAX. RMS INPUT VOLTS	MAX. PEAK INPUT VOLTS	MAX. ZENER VOLTS[1]	DIMENSIONS DIA. (A)	DIMENSIONS LENGTH (B)	DIMENSIONS FERRULE LENGTH (C)	ITT PART NO. FERRULE	ITT PART NO. WIRE LEAD
30	42	104	15/32	31/32	3/8	8A1QBG1	8A1ABG1
60	85	208	15/32	31/32	3/8	8A2QBG2	8A2ABG2
90	127	312	15/32	31/32	3/8	8A3QBG3	8A3ABG3
120	170	416	15/32	31/32	3/8	8A4QBG4	8A4ABG4
150	212	519	15/32	31/32	3/8	8A5QBG5	8A5ABG5
180	254	623	15/32	31/32	3/8	8A6QBG6	8A6ABG6
210	297	727	15/32	31/32	3/8	8A7QBG7	8A7ABG7
240	339	831	15/32	31/32	3/8	8A8QBG8	8A8ABG8
270	382	934	15/32	31/32	3/8	8A9QBG9	8A9ABG9
300	424	1039	15/32	31/32	3/8	8A10QBG10	8A10ABG10
330	467	1143	15/32	1 17/64	3/8	8A11QBG11	8A11ABG11
360	509	1247	15/32	1 17/64	3/8	8A12QBG12	8A12ABG12
390	551	1350	15/32	1 17/64	3/8	8A13QBG13	8A13ABG13
420	594	1454	15/32	1 17/64	3/8	8A14QBG14	8A14ABG14
450	636	1558	15/32	1 17/64	3/8	8A15QBG15	8A15ABG15
480	679	1662	15/32	1 1/2	3/8	8A16QBG16	8A16ABG16
510	721	1766	15/32	1 1/2	3/8	8A17QBG17	8A17ABG17
540	764	1870	15/32	1 1/2	3/8	8A18QBG18	8A18ABG18
570	806	1974	15/32	1 1/2	3/8	8A19QBG19	8A19ABG19
600	848	2078	15/32	1 1/2	3/8	8A20QBG20	8A20ABG20

MAX. RMS INPUT VOLTS	MAX. PEAK INPUT VOLTS	MAX. ZENER VOLTS[2]	DIMENSIONS DIA. (A)	DIMENSIONS LENGTH (B)	DIMENSIONS FERRULE LENGTH (C)	ITT PART NO. FERRULE	ITT PART NO. WIRE LEAD
30	42	104	31/32	1 1/32	13/32	25A1QBG1	25A1ABG1
60	85	208	31/32	1 1/32	13/32	25A2QBG2	25A2ABG2
90	127	312	31/32	1 1/32	13/32	25A3QBG3	25A3ABG3
120	170	416	31/32	1 1/32	13/32	25A4QBG4	25A4ABG4
150	212	519	31/32	1 1/32	13/32	25A5QBG5	25A5ABG5
180	254	623	31/32	1 1/32	13/32	25A6QBG6	25A6ABG6
210	297	727	31/32	1 1/32	13/32	25A7QBG7	25A7ABG7
240	339	831	31/32	1 1/32	13/32	25A8QBG8	25A8ABG8
270	382	934	31/32	1 1/32	13/32	25A9QBG9	25A9ABG9
300	424	1039	31/32	1 1/32	13/32	25A10QBG10	25A10ABG10
330	467	1143	31/32	1 29/64	13/32	25A11QBG11	25A11ABG11
360	509	1247	31/32	1 29/64	13/32	25A12QBG12	25A12ABG12
390	551	1350	31/32	1 29/64	13/32	25A13QBG13	25A13ABG13
420	594	1454	31/32	1 29/64	13/32	25A14QBG14	25A14ABG14
450	636	1558	31/32	1 29/64	13/32	25A15QBG15	25A15ABG15
480	679	1662	31/32	1 11/16	13/32	25A16QBG16	25A16ABG16
510	721	1766	31/32	1 11/16	13/32	25A17QBG17	25A17ABG17
540	764	1870	31/32	1 11/16	13/32	25A18QBG18	25A18ABG18
570	806	1974	31/32	1 11/16	13/32	25A19QBG19	25A19ABG19
600	848	2078	31/32	1 11/16	13/32	25A20QBG20	25A20ABG20

EYELET TYPES

MAX. RMS INPUT VOLTS	MAX. PEAK INPUT VOLTS	MAX. ZENER VOLTS[3]	DIMENSIONS LENGTH (B)	ITT PART NO.
25	35	80	47/64	102G1EX1
50	70	159	13/16	102G2EX2
75	105	239	57/64	102G3EX3
100	140	319	31/32	102G4EX4
125	175	398	1 3/64	102G5EX5
150	210	478	1 1/8	102G6EX6
175	245	558	1 13/64	102G7EX7
200	280	637	1 19/64	102G8EX8

STUD TYPES

MAX. RMS INPUT VOLTS	MAX. PEAK INPUT VOLTS	MAX. ZENER VOLTS[3]	DIMENSIONS STUD LENGTH (A)	DIMENSIONS STACK LENGTH (B)	ITT PART NO.
25	35	80	1 7/16	15/16	102G1BX1
50	70	159	1 1/2	1	102G2BX2
75	105	239	1 5/8	1 1/8	102G3BX3
100	140	319	1 11/16	1 3/16	102G4BX4
125	175	398	1 3/4	1 1/4	102G5BX5
150	210	478	1 7/8	1 3/8	102G6BX6
175	245	558	1 15/16	1 7/16	102G7BX7
200	280	637	2	1 1/2	102G8BX8
225	315	717	2 1/16	1 9/16	102G9BX9
250	350	797	2 3/16	1 11/16	102G10BX10
275	385	876	2 1/4	1 3/4	102G11BX11
300	420	956	2 5/16	1 13/16	102G12BX12
325	455	1035	2 3/8	1 7/8	102G13BX13
350	490	1115	2 1/2	2	102G14BX14
375	525	1195	2 9/16	2 1/16	102G15BX15
400	560	1274	2 5/8	2 1/8	102G16BX16
425	595	1354	2 3/4	2 1/4	102G17BX17
450	630	1434	2 13/16	2 5/16	102G18BX18
475	665	1513	2 7/8	2 3/8	102G19BX19
500	700	1593	2 15/16	2 7/16	102G20BX20
600	840	1913	3 5/16	2 13/16	102G24BX24

NOTES: 1. At 4 millisecond pulse current = 0.75 Amperes
2. At 4 millisecond pulse current = 2 Amperes
3. At 4 millisecond pulse current = 8 Amperes

ELECTRICAL AND MECHANICAL CHARACTERISTICS – DC INPUT TYPES

PAPER TUBE TYPES

MAX. RMS INPUT VOLTS	MAX. PEAK INPUT VOLTS	MAX. ZENER VOLTS	DIMENSIONS DIA. (A)	DIMENSIONS LENGTH (B)	ITT PART NO.
20	31	104	3/8	27/32	8A1PG0
40	63	208	3/8	27/32	8A2PG0
60	93	312	3/8	27/32	8A3PG0
80	126	416	3/8	27/32	8A4PG0
100	157	519	3/8	27/32	8A5PG0
120	188	623	3/8	27/32	8A6PG0
140	220	727	3/8	27/32	8A7PG0
160	251	831	3/8	27/32	8A8PG0
180	282	934	3/8	27/32	8A9PG0
200	314	1039	3/8	27/32	8A10PG0
220	345	1143	3/8	1 3/32	8A11PG0
240	377	1247	3/8	1 3/32	8A12PG0
260	409	1350	3/8	1 3/32	8A13PG0
280	440	1454	3/8	1 3/32	8A14PG0
300	472	1558	3/8	1 3/32	8A15PG0
320	502	1662	3/8	1 3/32	8A16PG0
340	534	1766	3/8	1 3/32	8A17PG0
360	566	1870	3/8	1 3/32	8A18PG0
380	597	1974	3/8	1 3/32	8A19PG0
400	628	2078	3/8	1 3/32	8A20PG0

MAX. RMS INPUT VOLTS	MAX. PEAK INPUT VOLTS	MAX. ZENER VOLTS[2]	DIMENSIONS DIA. (A)	DIMENSIONS LENGTH (B)	ITT PART NO.
20	31	87	37/64	1 1/64	25A1PG0
40	63	177	37/64	1 1/64	25A2PG0
60	93	266	37/64	1 1/64	25A3PG0
80	126	354	37/64	1 1/64	25A4PG0
100	157	443	37/64	1 1/64	25A5PG0
120	188	532	37/64	1 1/64	25A6PG0
140	220	620	37/64	1 1/64	25A7PG0
160	251	709	37/64	1 1/64	25A8PG0
180	282	798	37/64	1 1/64	25A9PG0
200	314	886	37/64	1 1/64	25A10PG0
220	345	975	37/64	1 1/4	25A11PG0
240	377	1063	37/64	1 1/4	25A12PG0
260	409	1152	37/64	1 1/4	25A13PG0
280	440	1241	37/64	1 1/4	25A14PG0
300	472	1329	37/64	1 1/4	25A15PG0
320	502	1417	37/64	1 1/4	25A16PG0
340	534	1507	37/64	1 1/4	25A17PG0
360	566	1595	37/64	1 1/4	25A18PG0
380	597	1684	37/64	1 1/4	25A19PG0
400	628	1772	37/64	1 1/4	25A20PG0

PHENOLIC TUBE TYPES

MAX. RMS INPUT VOLTS	MAX. PEAK INPUT VOLTS	MAX. ZENER VOLTS[1]	DIMENSIONS DIA. (A)	DIMENSIONS LENGTH (B)	DIMENSIONS FERRULE LENGTH (C)	ITT PART NO. FERRULE	ITT PART NO. WIRE LEAD
20	31	104	15/32	31/32	3/8	8A1QBG0	8A1ABG0
40	63	208	15/32	31/32	3/8	8A2QBG0	8A2ABG0
60	93	312	15/32	31/32	3/8	8A3QBG0	8A3ABG0
80	126	416	15/32	31/32	3/8	8A4QBG0	8A4ABG0
100	157	519	15/32	31/32	3/8	8A5QBG0	8A5ABG0
120	188	623	15/32	31/32	3/8	8A6QBG0	8A6ABG0
140	120	727	15/32	31/32	3/8	8A7QBG0	8A7ABG0
160	251	831	15/32	31/32	3/8	8A8QBG0	8A8ABG0
180	282	934	15/32	31/32	3/8	8A9QBG0	8A9ABG0
200	314	1039	15/32	31/32	3/8	8A10QBG0	8A10ABG0
220	345	1143	15/32	31/32	3/8	8A11QBG0	8A11ABG0
240	377	1247	15/32	31/32	3/8	8A12QBG0	8A12ABG0
260	409	1350	15/32	31/32	3/8	8A13QBG0	8A13ABG0
280	440	1454	15/32	31/32	3/8	8A14QBG0	8A14ABG0
300	472	1558	15/32	31/32	3/8	8A15QBG0	8A15ABG0
320	502	1662	15/32	31/32	3/8	8A16QBG0	8A16ABG0
340	534	1766	15/32	31/32	3/8	8A17QBG0	8A17ABG0
360	566	1870	15/32	31/32	3/8	8A18QBG0	8A18ABG0
380	597	1974	15/32	31/32	3/8	8A19QBG0	8A19ABG0
400	628	2078	15/32	31/32	3/8	8A20QBG0	8A20ABG0

MAX. RMS INPUT VOLTS	MAX. PEAK INPUT VOLTS	MAX. ZENER VOLTS[2]	DIMENSIONS DIA. (A)	DIMENSIONS LENGTH (B)	DIMENSIONS FERRULE LENGTH (C)	ITT PART NO. FERRULE	ITT PART NO. WIRE LEAD
20	31	104	31/32	1 1/32	13/32	25A1QBG0	25A1ABG0
40	63	208	31/32	1 1/32	13/32	25A2QBG0	25A2ABG0
60	93	312	31/32	1 1/32	13/32	25A3QBG0	25A3ABG0
80	126	416	31/32	1 1/32	13/32	25A4QBG0	25A4ABG0
100	157	519	31/32	1 1/32	13/32	25A5QBG0	25A5ABG0
120	188	623	31/32	1 1/32	13/32	25A6QBG0	25A6ABG0
140	220	727	31/32	1 1/32	13/32	25A7QBG0	25A7ABG0
160	251	831	31/32	1 1/32	13/32	25A8QBG0	25A8ABG0
180	282	934	31/32	1 1/32	13/32	25A9QBG0	25A9ABG0
200	314	1039	31/32	1 1/32	13/32	25A10QBG0	25A10ABG0
220	345	1143	31/32	1 1/32	13/32	25A11QBG0	25A11ABG0
240	377	1247	31/32	1 1/32	13/32	25A12QBG0	25A12ABG0
260	409	1350	31/32	1 1/32	13/32	25A13QBG0	25A13ABG0
280	440	1454	31/32	1 1/32	13/32	25A14QBG0	25A14ABG0
300	472	1558	31/32	1 1/32	13/32	25A15QBG0	25A15ABG0
320	502	1662	31/32	1 1/32	13/32	25A16QBG0	25A16ABG0
340	534	1766	31/32	1 1/32	13/32	25A17QBG0	25A17ABG0
360	566	1870	31/32	1 1/32	13/32	25A18QBG0	25A18ABG0
380	597	1974	31/32	1 1/32	13/32	25A19QBG0	25A19ABG0
400	628	2078	31/32	1 1/32	13/32	25A20QBG0	25A20ABG0

EYELET TYPES

MAX. RMS INPUT VOLTS	MAX. PEAK INPUT VOLTS	MAX. ZENER VOLTS[1]	DIMENSIONS LENGTH (B)	ITT PART NO.
20	31	80	27/32	102G1EX0
40	63	159	7/8	102G2EX0
60	93	239	29/32	102G3EX0
80	126	319	15/16	102G4EX0
100	157	398	1	102G5EX0
120	188	478	1 1/32	102G6EX0
140	220	558	1 1/16	102G7EX0
160	251	637	1 1/8	102G8EX0
180	282	717	1 5/32	102G9EX0
200	314	795	1 3/16	102G10EX0
220	345	876	1 1/4	102G11EX0
240	377	956	1 9/32	102G12EX0
260	409	1035	1 5/16	102G13EX0
280	440	1115	1 11/32	102G14EX0
300	472	1195	1 3/8	102G15EX0
320	502	1274	1 7/16	102G16EX0

STUD TYPES

MAX. RMS INPUT VOLTS	MAX. PEAK INPUT VOLTS	MAX. ZENER VOLTS[3]	DIMENSIONS STUD LENGTH (A)	DIMENSIONS STACK LENGTH (B)	ITT PART NO.
20	31	80	1 5/16	13/16	102G1BX0
40	63	159	1 3/8	27/32	102G2BX0
60	93	239	1 3/8	7/8	102G3BX0
80	126	319	1 7/16	29/32	102G4BX0
100	157	398	1 1/2	15/16	102G5BX0
120	188	478	1 5/8	1 3/32	102G6BX0
140	220	558	1 5/8	1 1/8	102G7BX0
160	251	637	1 11/16	1 3/16	102G8BX0
180	282	717	1 3/4	1 7/32	102G9BX0
200	314	797	1 3/4	1 1/4	102G10BX0
220	345	876	1 13/16	1 9/32	102G11BX0
240	377	956	1 7/8	1 11/32	102G12BX0
260	409	1035	1 15/16	1 3/8	102G13BX0
280	440	1115	1 15/16	1 13/32	102G14BX0
300	472	1195	1 15/16	1 15/32	102G15BX0
320	502	1274	2	1 1/2	102G16BX0

NOTES: 1. At 4 millisecond pulse current=0.75 Amperes
2. At 4 millisecond pulse current=2 Amperes
3. At 4 millisecond pulse current=8 Amperes

HOW TO SELECT THE PROPER RECTIFIER

Determination of Current Rating

Although the peak value and duration of a transient current cannot always be determined, certain valid assumptions can be made to determine the ITT suppressor rectifier current rating for the application.

For circuits in which a transformer is the power source, usually the greatest transient currents have been observed when the circuit is interrupted with no load on the transformer. The transient current is the magnetizing current of the transformer. If the actual transient current is not known, a valid assumption can be made by the use of the magnetizing current versus voltage on page 4. If the transient results from opening a circuit containing an inductance, the transient current will be the current through the inductance at the instant of interruption. To select the proper ITT suppressor series, assume a single pulse width of 4 milliseconds and refer to the pulse current versus time curve on page 4. The same curve can be used to select the appropriate ITT series when a single pulse width other than 4 milliseconds is known or assumed.

Voltage Rating

After the required current rating has been established, determine the maximum steady-state voltage which will appear across the suppressor rectifier and select the appropriate type number from the tables on pages 2 and 3. Note that both RMS and peak voltage ratings are tabulated for AC types and DC ratings for DC types. Use the RMS value for sinusoidal voltages; otherwise, use the peak value of the input voltage to select the proper rectifier.

Zener Voltage

The Zener voltages shown in the characteristics tables are the maximum instantaneous voltages that will appear across the rectifier if the 4 millisecond current rating is not exceeded. Any ITT suppressor rectifier can safely discharge higher currents than this rating, where the pulse width is less than 4 milliseconds.

For other values of peak current, however, the indicated Zener voltage will be as shown in the curves on page 4. To obtain the expected protection, rectifiers should be used within their rated currents. For optimum protection, the maximum Zener voltage should be below the PIV rating of the semiconductor devices being protected.

The maximum Zener voltages shown in the characteristics tables have been derived from the curves on page 4 which represent the conservative ratings placed on suppressor rectifiers. These volt-ampere curves apply to a single cell. To determine the Zener voltage for a particular rectifier, multiply the peak voltage values that are shown by the number of cells per arm for AC rectifiers, or by the total number of cells for DC rectifiers. The final step is to be sure that the silicon or germanium rectifier or silicon controlled rectifier to be protected has a PIV rating higher than the Zener voltage of the ITT protector rectifier. The volt-ampere curves are also valid for DC applications in determining the proper rectifier for a given peak transient voltage.

Similar protection is also provided to transformers, capacitors, resistors, switches, relays, or any electrical component subject to damage from transient over-voltage.

Example

Assume a single phase full-wave bridge rectifier application with a transformer rated at 8.5KVA, 115V. The rectifier to be protected is across the transformer secondary.

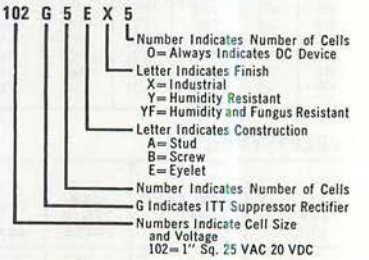
1. Assume a 4 millisecond pulse width.
2. From the curve on page 4, determine the per cent of magnetizing current. Using the "maximum" plot line, 8.5KVA ≈5.2% of full load current.

Full load current $\frac{VA}{V} \approx \frac{8500}{115} \approx 74A$

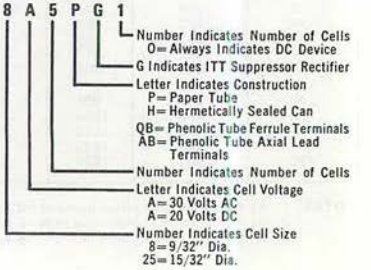
$74A \times 5.2\% \approx 3.85A$ peak.

3. From the RATINGS table on page 1, select a rectifier series which will withstand 3.85A peak @ 4 millisecond pulse width. The 102 series, either stud mounting or eyelet mounting may be used. Assume a stud type is preferred for this application.
4. Select the appropriate ITT part number from the stud mounting table on page 2 by finding a type with a RMS input voltage rating equal to or above 115V. 102G5BX5 meets this requirement.
5. Determine the PIV rating required for the rectifier to be protected. Use the 102 series curve on page 4 to determine the voltage corresponding to 3.85A. The maximum voltage is 73 volts per cell. The number of cells in each rectifier is indicated by the first number after the first letter in the part number. In this case the 102G5BX5 has five cells. The maximum voltage is $73 \times 5 = 365V$. The PIV rating required for the protected rectifier is 365V.

CODING SYSTEM FOR EYELET AND STUD TYPE ITT SELENIUM VOLTAGE SUPPRESSOR RECTIFIERS

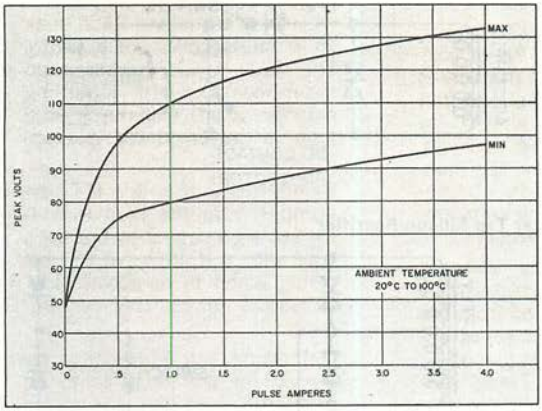


CODING SYSTEM FOR TUBULAR TYPE ITT SELENIUM VOLTAGE SUPPRESSOR RECTIFIERS

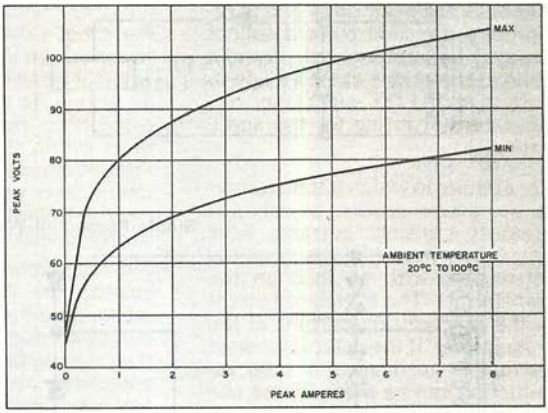


CHARACTERISTIC CURVES

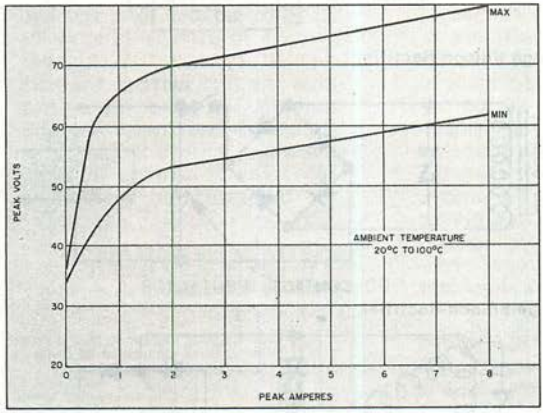
8A1 SERIES PEAK VOLTAGE VS CURRENT



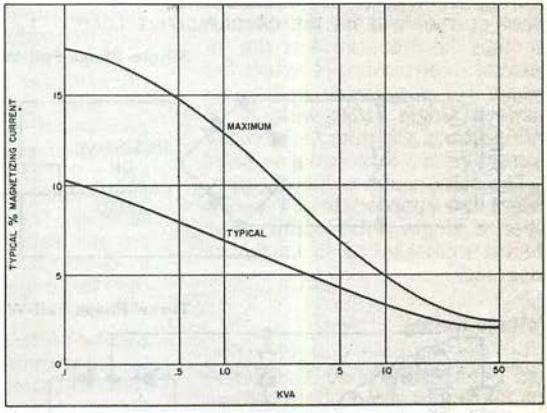
25A1 SERIES PEAK VOLTAGE VS CURRENT



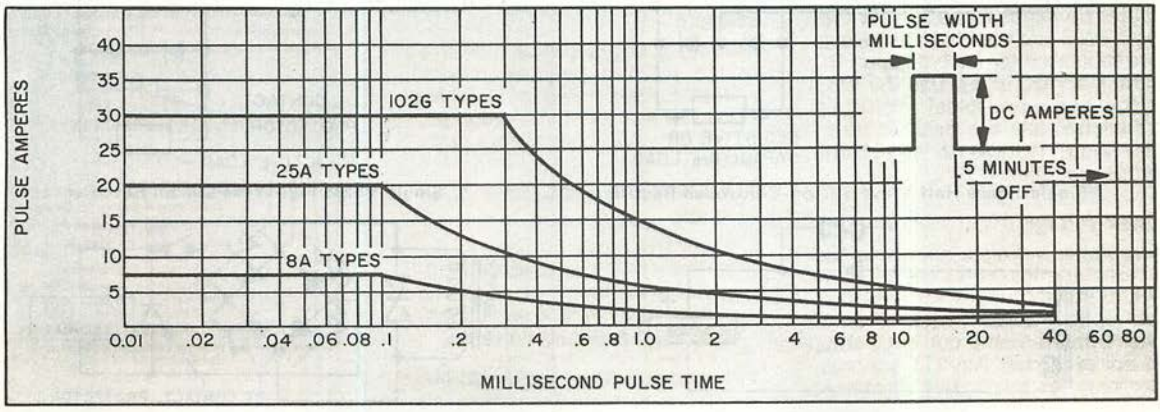
102 SERIES PEAK VOLTAGE VS CURRENT



MAGNETIZING CURRENT VS VOLTAGE

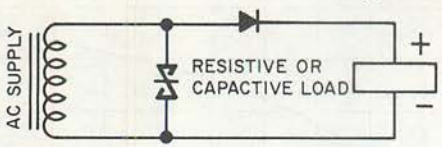


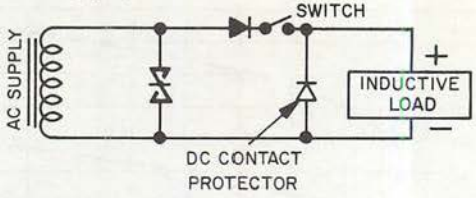
PULSE CURRENT VS TIME



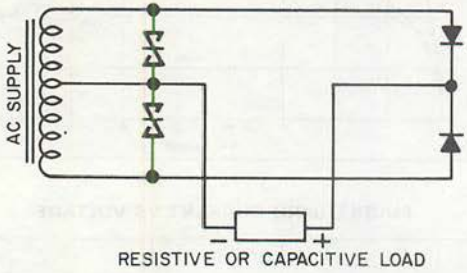
TYPICAL APPLICATIONS

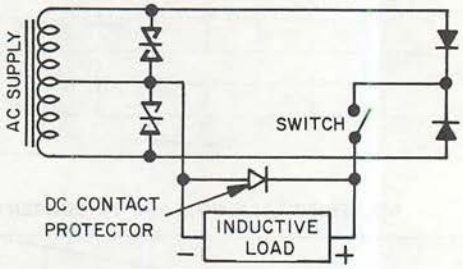
Single-Phase Half-Wave Silicon Rectifier



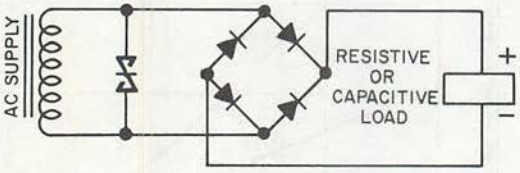


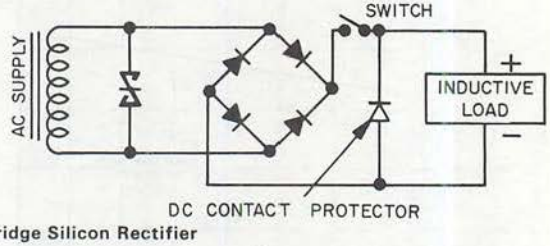
Single-Phase Full-Wave Center Tap Silicon Rectifier



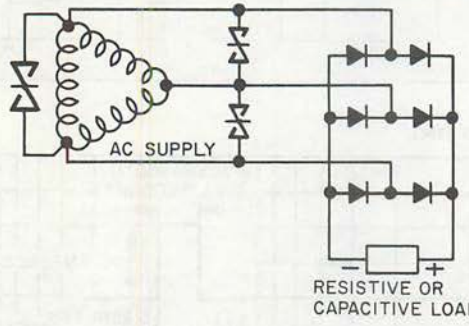


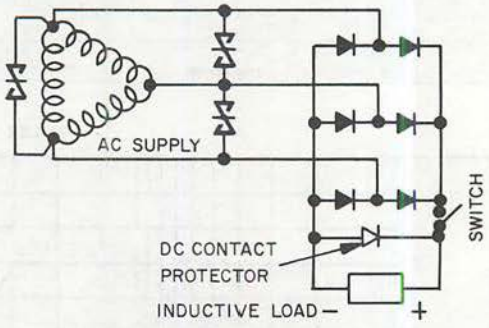
Single-Phase Full-Wave Bridge Silicon Rectifier



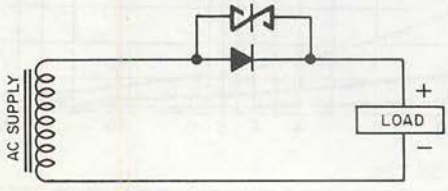


Three-Phase Full-Wave Bridge Silicon Rectifier

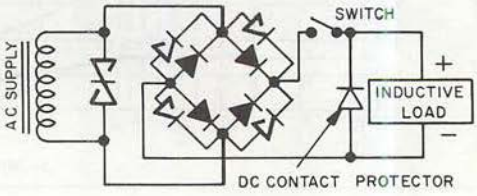




Single-Phase Half-Wave Silicon-Controlled Rectifier



Single-Phase Full-Wave Silicon Rectifier



Package: DO-7

DIFFUSED SILICON GENERAL-PURPOSE DIODES

ABSOLUTE MAXIMUM RATINGS at 25°C free-air temperature (unless otherwise noted)

Symbol	Characteristics	1N645	1N646	1N647	1N648	1N649	Unit
$V_{RM(wkg)}$	Working Peak Reverse Voltage over Operating Free-Air Temperature Range	225	300	400	500	600	V
I_O	Average Rectified Forward Current at (or below) 25°C Free-Air Temperature (See Note 1)	400					mA
I_O	Average Rectified Forward Current at 150°C Free-Air Temperature (See Note 1)	150					mA
$I_{FM(surge)}$	Peak Surge Current, One Second, at 25°C to 150°C Free-Air Temperature (See Note 2)	3					A
P	Continuous Power Dissipation at (or below) 25°C Free-Air Temperature (See Note 3)	600					mW
$T_{A(opr)}$	Operating Free-Air Temperature Range	−65 to 150					°C

ELECTRICAL CHARACTERISTICS at 25°C free-air temperature (unless otherwise noted)

Symbol	Parameter	1N645* Min	1N645* Max	1N646 Min	1N646 Max	1N647* Min	1N647* Max	1N648 Min	1N648 Max	1N649* Min	1N649* Max	Unit	Conditions
$V_{(BR)}$	Reverse Breakdown Voltage	275		360		480		600		720		V	I_R = 100 μA, T_A = 100°C
I_R	Static Reverse Current		0.2		0.2		0.2		0.2		0.2	μA	V_R = Rated $V_{RM(wkg)}$
			15		15		20		20		25	μA	V_R = Rated $V_{RM(wkg)}$, T_A = 100°C
V_F	Static Forward Voltage		1		1		1		1		1	V	I_F = 400 mA
C_T	Total Capacitance		6 typ		6 typ		6 typ		6 typ		6 typ	pF	V_R = 12 V, f = 1 MHz

NOTES:

1. These values may be applied continuously under single-phase 60-Hz half-sine-wave operation with resistive load. Above 25°C see Thermal Characteristics Chart.
2. These values apply for a one-second square-wave pulse with the device at nonoperating thermal equilibrium immediately prior to the surge.
3. Derate linearly to 200 mW at 150°C free-air temperature at the rate of 3.2 mW/deg.

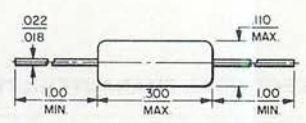
* IN645, IN647 and IN649 are available in JAN and JAN TX versions.

JAN 1N645®
SILICON DIODE

DIFFUSED SILICON HIGH POWER GLASS RECTIFIER

The ITT JAN 1N645 meets MIL-S-19500/240B.

DIMENSIONS



DO-7

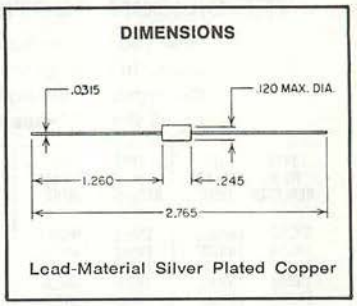
ABSOLUTE MAXIMUM RATINGS

CHARACTERISTICS @ 25°C unless otherwise noted.		UNITS
Peak Inverse Voltage	270	Volts
Power Dissipation	500	mW
Storage Temperature	−65 to +200	°C
Surge Current, 1/120 second, 150°C	5	Amps

ELECTRICAL CHARACTERISTICS @ 25°C unless otherwise noted.

SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITIONS
PIV	270			Vdc	I_R=100μA
I_R			25 15	nA μA	V_R=225V V_R=225V, T=150°C
V_F			1.0	Vdc	I_F=400 mA
C			20	pF	V_R=4V

1-AMP PLASTIC SILICON RECTIFIERS



The ITT Plastic Silicon Rectifier is molded using a new plastic formulation with the following advantages over silicone and epoxy compounds:

- **Lower thermosetting temperature (170°F) resulting in less strain to junctions and surfaces during the molding process.**
- **No pre-cure or post-cure needed.**
- **Moisture resistance and humidity resistance far superior to others.**

ELECTRICAL CHARACTERISTICS @ 25°C unless otherwise noted

		*1N4000 Series	EM500 Series	Units
Peak Reverse Voltage (PRV)	50	1N4001 50	(EM500)	Volts
	100	1N4002 100	(EM501)	
	200	1N4003 200	(EM502)	
	400	1N4004 400	(EM504)	
	600	1N4005 600	(EM506)	
	800	1N4006 800	(EM508)	
	1000	1N4007 1000	(EM510)	
Average Rectified Current @ 25°C Ambient		1.0	1.0	Amps
75°C Ambient		1.0	0.5	Amps
Forward Voltage Drop @ 1 Amp		1.1	1.1	Volts
Reverse Current @ Rated DC Voltage		10	1.0	Volts
Full Cycle Average Reverse Current @ Rated PRV @				
85°C Ambient @ Rated Average Rectified Current		200	200	Volts
100°C Ambient @ Rated Average Rectified Current		50	50	Volts
Half Cycle Surge Current, 60 Hz		30	50	Amps
Temperature Range (operating)		−65 to +175	−65 to +175	°C
Temperature Range — Storage		−65 to +200	−65 to +200	°C

*Electrical Equivalent

ITT SILICON RECTIFIER CROSS-REFERENCE

Now you can replace older types of rectifiers with dependable, inexpensive ITT Plastic types. In most cases, the ITT types will have higher output current and PRV ratings than the types to be replaced. Case dimensions are not always physically identical, in many cases the ITT types are smaller.

TYPE TO BE REPLACED	ITT REPLACEMENT
1N253	1N4002
1N254	1N4003
1N255	1N4004
1N256	1N4005
1N316	1N4001
1N316A	1N4001
1N317	1N40J2
1N317A	1N4002
1N318	1N4003
1N318A	1N4003
1N319	1N4004
1N319A	1N4004
1N320	1N4005
1N320A	1N40J5
1N321A	1N4007
1N322A	1N4007
1N323A	1N4001
1N324A	1N40J2
1N325A	1N4003
1N326A	1N4004
1N327A	1N4005
1N328A	1N4007
1N329A	1N4007
1N332	1N4004
1N333	1N4004
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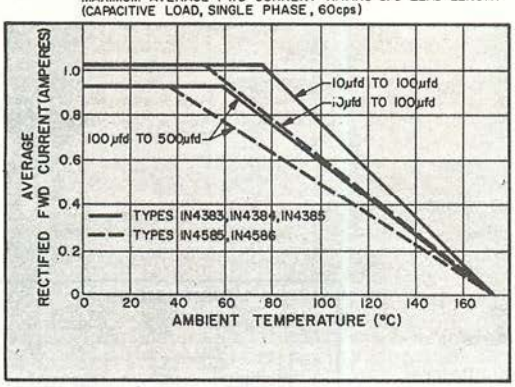
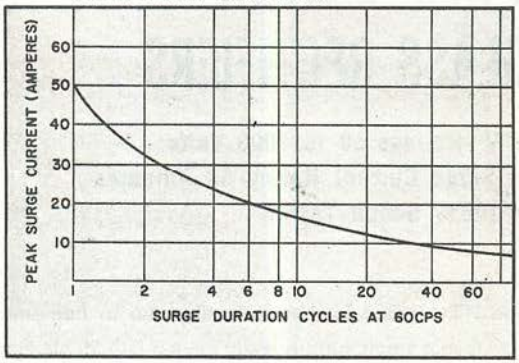
S91H	1N4002
S92	1N4003
S92H	1N4003
S93	1N4004
S93H	1N4004
S94	1N4004

TYPICAL CHARACTERISTICS @ 25°C unless otherwise noted

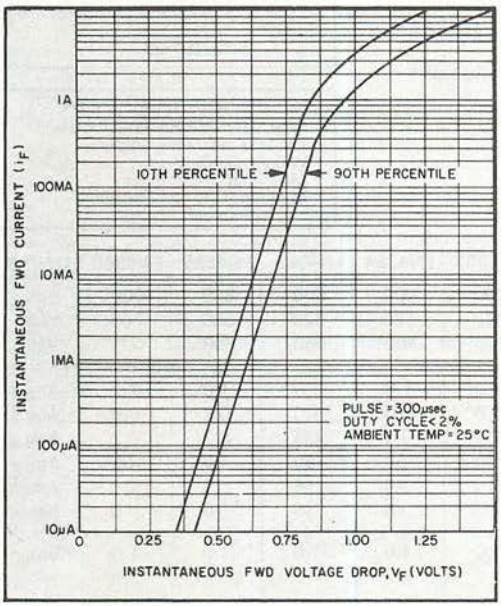
MAXIMUM AVERAGE FWD CURRENT RATING-3/8" LEAD LENGTH
(CAPACITIVE LOAD, SINGLE PHASE, 60cps)



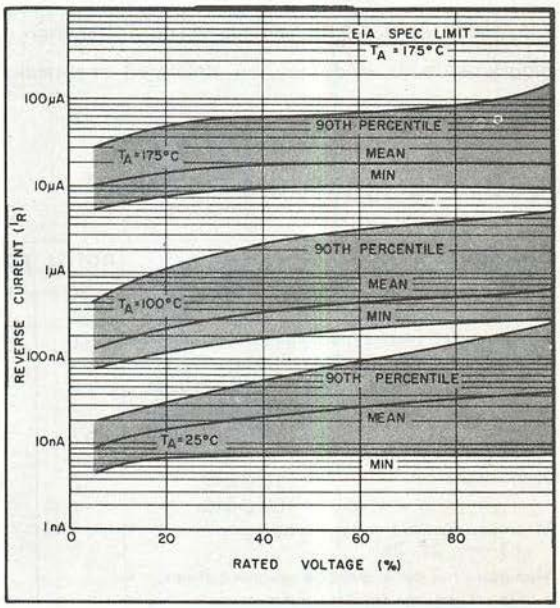
NON-RECURRENT SURGE RATING



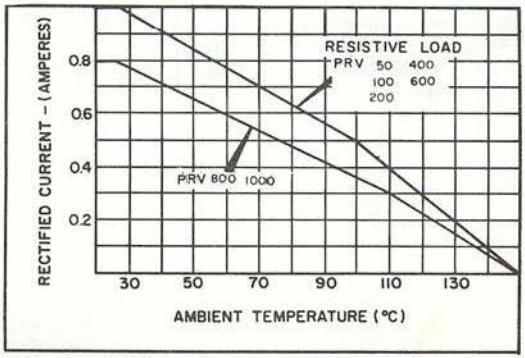
FORWARD VOLTAGE DROP



REVERSE CURRENT



RECTIFIED CURRENT RATING
VS TEMPERATURE

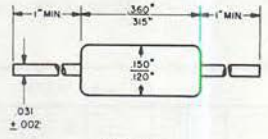


1-AMP SILICON GLASS RECTIFIERS

- V_R Ratings 50 to 1000 Volts
- Surge Current Rating 50 Amperes
- 100% Scope Tested

The ITT 1N4383-5, 1N4585-6, offer up to one-amp rectified current at 100°C in a small, hermetically sealed DO-29 glass package. All units are passivated, 100 percent tested, and have a 50-amp surge current rating to insure a stable, highly reliable rectifier. Rectifiers are supplied with solderable leads and may be delivered reel-packed for automatic insertion equipment.

DIMENSIONS



DO-29

MECHANICAL DATA

Case: Hermetically sealed glass
Leads: Solderable, tin plated
Weight: 0.02 oz.
Mounting position: Any
Marking: ITT, cathode band, part number.

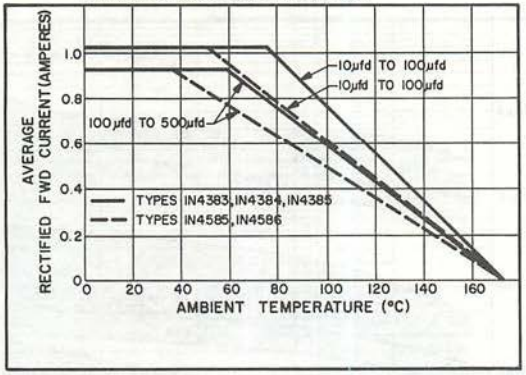
ABSOLUTE MAXIMUM RATINGS[1]

CHARACTERISTICS	RG1122	RG1123	1N4383	1N4384	1N4385	1N4585	1N4586	UNITS
Maximum recurrent peak reverse voltage	50	100	200	400	600	800	1000	Volts
Maximum RMS voltage	35	70	140	280	420	560	700	Volts
Maximum DC blocking voltage	50	100	200	400	600	800	1000	Volts
Maximum average forward rectified current 3/8" lead length — 50°C Ambient	1.0	1.0	1.0	1.0	1.0	1.0	1.0	Amps
100°C Ambient	1.0	1.0	1.0	1.0	1.0	0.6	0.6	Amps
150°C Ambient	0.3	0.3	0.3	0.3	0.3	0.2	0.2	Amps
Maximum peak surge overload current — 1 Cycle	50	50	50	50	50	50	50	Amps
10 Cycles	16	16	16	16	16	16	16	Amps
100 Cycles	6	6	6	6	6	6	6	Amps
Maximum forward voltage drop at 1 amp DC, 25°C	1.0	1.0	1.0	1.0	1.0	1.0	1.0	Volts
Maximum full cycle average reverse current, @rated average forward current and 100°C ambient	275	250	275	250	225	200	200	μamps
Maximum DC leakage at rated DC blocking voltage and 25°C ambient	10	10	10	10	10	10	10	μamps
Typical recovery time at 25°C ambient	10	10	10	10	10	10	10	μsecs
Temperature Range, op & stg	—65 to +175							°C

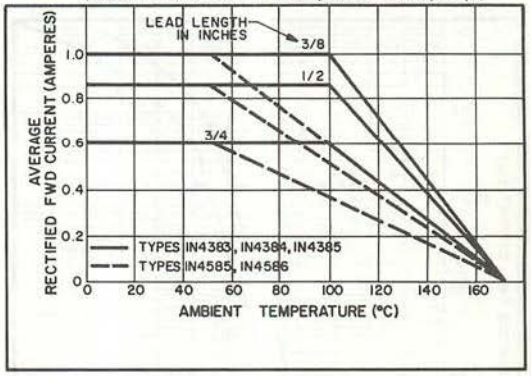
NOTE: 60 cps, inductive or resistive load, single phase half wave.

TYPICAL CHARACTERISTICS @ 25°C unless otherwise noted

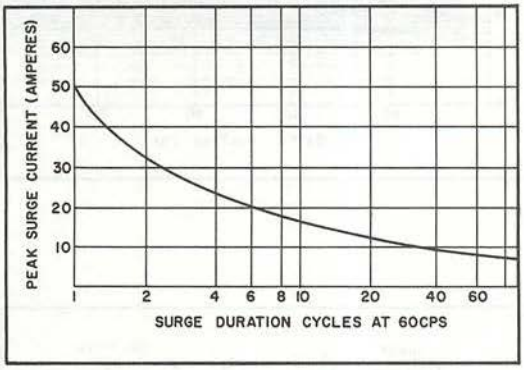
MAXIMUM AVERAGE FWD CURRENT RATING-3/8" LEAD LENGTH
(CAPACITIVE LOAD, SINGLE PHASE, 60cps)



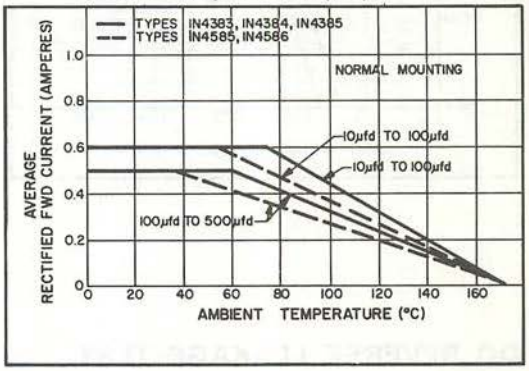
MAXIMUM AVERAGE FORWARD CURRENT RATING
(RESISTIVE OR INDUCTIVE LOAD, SINGLE PHASE, 60cps)



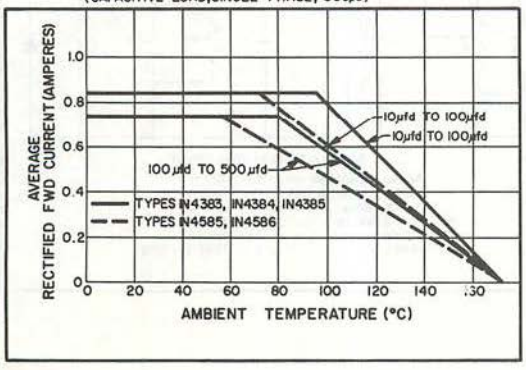
NON-RECURRENT SURGE RATING
(-65°C TO 175°C)



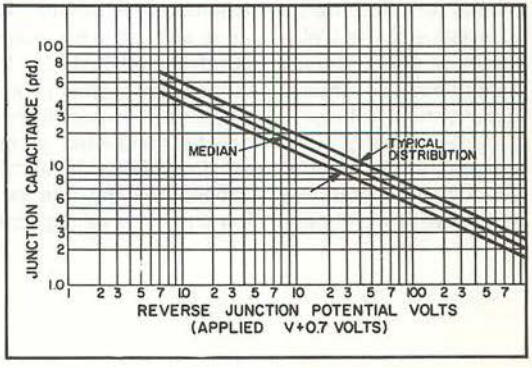
MAXIMUM AVERAGE FWD CURRENT RATING-3/4" LEAD LENGTH
(CAPACITIVE LOAD, SINGLE PHASE, 60cps)



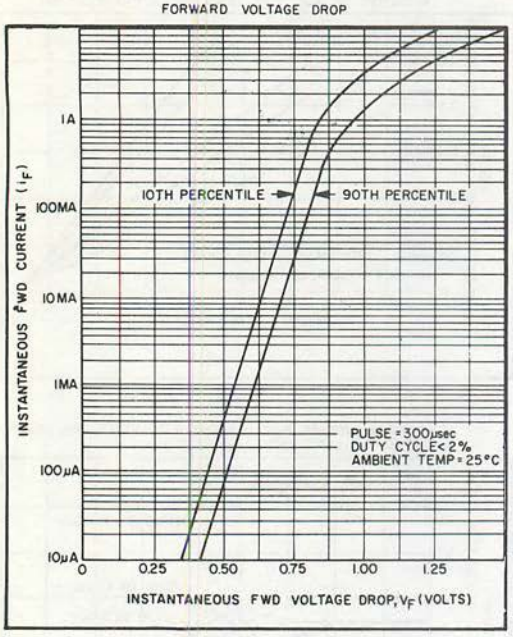
MAXIMUM AVERAGE FWD CURRENT RATING-1/2" LEAD LENGTH
(CAPACITIVE LOAD, SINGLE PHASE, 60cps)

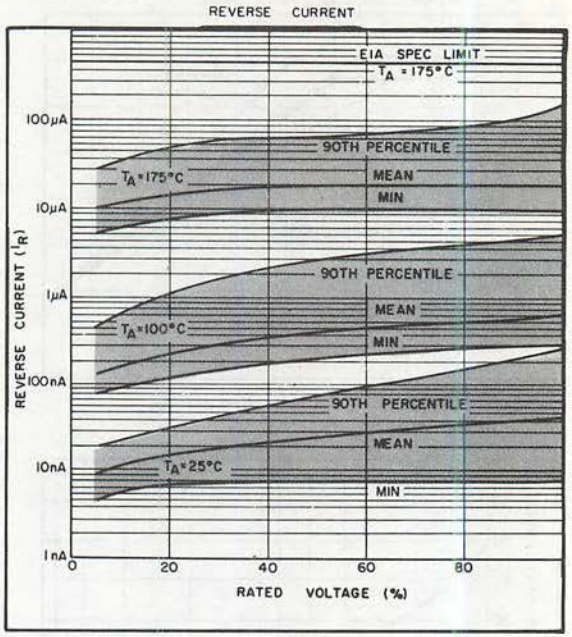


JUNCTION CAPACITANCE vs. REVERSE JUNCTION POTENTIAL



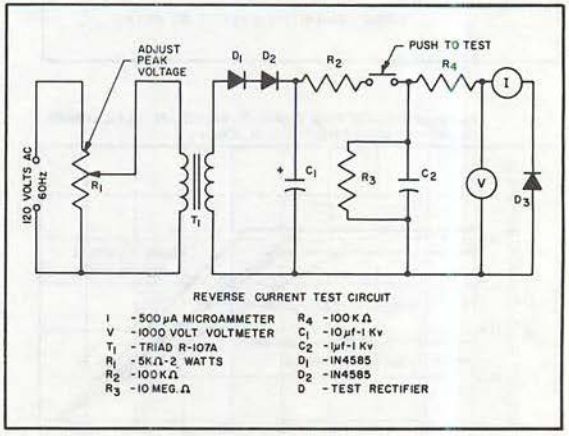
TYPICAL CHARACTERISTICS, continued





DC REVERSE LEAKAGE TEST

The circuit at right provides a simple and inexpensive means for checking the instantaneous leakage characteristics of the 1N4383 series and other low current rectifiers. The pushbutton switch should *not* be omitted as it minimizes junction heating when testing is being done at high voltage, and prevents the possibility of thermal runaway. Tests may be conducted at high temperature by placing the test rectifier(s) in an oven. Junction temperature rise above ambient due to internal heating is generally low enough to be neglected.



REVERSE CURRENT TEST CIRCUIT

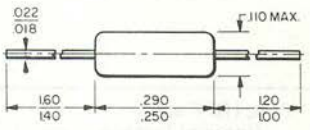
I	- 500µA MICROAMMETER	R_4	- 100K Ω
V	- 1000 VOLT VOLTMETER	C_1	- 10µf - 1 Kv
T_1	- TRIAD R-107A	C_2	- 1µf - 1 Kv
R_1	- 5K Ω - 2 WATTS	D_1	- 1N4585
R_2	- 100K Ω	D_2	- 1N4585
R_3	- 10 MEG. Ω	D	- TEST RECTIFIER

4-LAYER DIODE THYRISTORS

- **Firing Voltages 20 to 100 volts**
- **Switching current <125 μA @ 25°C**
- **ON resistance <2Ω @ 70mA**

The ITT diode thyristor is a reliable negative resistance device designed for use in switching circuits. Typical applications include ring counters, matrixes, pulse generators, relay drivers, multivibrators, pulse modulators, and timing circuits.

DIMENSIONS



DO-7

ELECTRICAL SPECIFICATIONS

Type Number	Switching Voltage (V_S)		Reverse Breakdown Voltage (Min.)
	25°C	−40° to 85°C	
1N3831	20±4	14-25	12
1N3832	25±4	19-30	15
1N3833	30±4	23-36	18
1N3834	35±4	28-41	21
1N3835	40±4	32-46	24
1N3836	45±4	37-51	27
1N3837	50±4	41-57	30
1N3838	100±10	80-115	60
1N3839	20±4	14-25	12
1N3840	25±4	19-30	15
1N3841	30±4	23-36	18
1N3842	35±4	28-41	21
1N3843	40±4	32-46	24
1N3844	45±4	37-51	27
1N3845	50±4	41-57	30
1N3846	100±10	80-115	60

MECHANICAL DATA

Case:
Hermetically sealed glass

Finish:
All external surfaces corrosion resistant and leads readily solderable

Leads:
Dumet, tin plated

Weight:
0.135 grams (approx.)

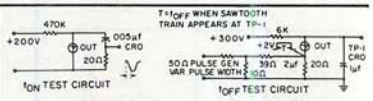
Mounting Position:
Any

Marking:
The symbol for the 4-layer diode is a modified "4". The slant line of the "4" indicates the forward direction of current passing through the device when in the ON state.

ABSOLUTE MAXIMUM RATINGS

CHARACTERISTICS		UNITS
Average Forward Current, 50°C	150	mA
Power Dissipation, 50°C	150	mW
Power-Temperature Derating	1.5	mW/°C
Reverse Breakdown Voltage from T_A = −60 to +125°C	nominal $V_S/2$	min.
Operating and Storage Temperature	−60 to +125	°C

ELECTRICAL CHARACTERISTICS @ 25°C unless otherwise noted

SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITIONS
I_S (forward switching current)			125 250	μA μA	 −60 to +125°C
I_H (holding current)	0.5 14 5		15 50 40	mA mA mA mA	IN3831-38 IN3839-46 IN3831-38 @ −40°C IN3839-46 @ +85°C
I_{ik} (OFF state) (forward leakage current)			5	μA	60% of nom. V_S
V_{ON} (forward voltage drop)			1.2 2.7	V V	I_f = 70 mA I_f = 5A (pulsed)
r_{on} (dynamic forward impedance)			2.0	Ω	I_f = 70 mA
t_{on}		0.1		μsec	
t_{off}		5		μsec	

HOW THE 4-LAYER DIODE OPERATES

The voltage-current characteristic for the 4-layer diode shows three essential operating regions:

I—"off" or high resistance state

II—transition or negative resistance state

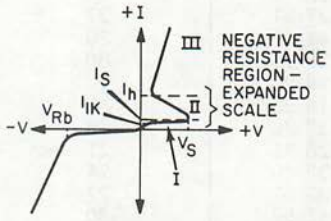
III—"on" or low resistance state

This curve is shown on a very expanded scale (non-linear) for illustration purposes only. Note that as the voltage rises and reaches the switching voltage (V_S), the device begins to switch "on." The current at this point (I_S) is typically several microamperes. The device switches because of an internal feedback mechanism allowing the diode to pass a steadily increasing current as the voltage decreases (negative resistance state, Region II). When "on" (Region III), the 4-layer diode passes a current which is limited principally by the external circuit.

In the "on" state, the device has a dynamic resistance of less than a few ohms and a voltage drop of about one volt. As long as sufficient current is passed by the circuit, the device will remain in the "on" condition. At the point on the curve marked I_h, the circuit is passing just enough current to keep the device in the "on" condition. If the current drops below I_h the diode switches back to the high resistance or "off" condition.

Rate Effect

In its "off" condition the device will pass a capacitive current in response to a sharply rising voltage wave. If the rise rate of this voltage wave is large enough (usually 10 to 100 volts / μS), switching occurs below the DC switching voltage.

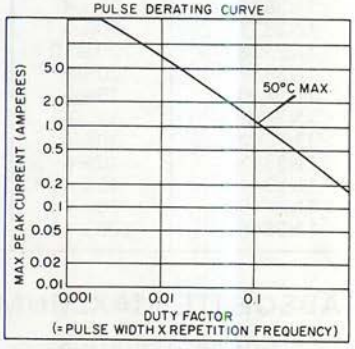


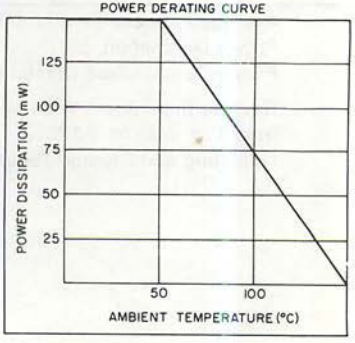
V-I CHARACTERISTICS

TERMS AND SYMBOLS

- V_s Switching Voltage—Closest point to peak voltage in Region II where slope of V-I curve is −330Ω. This definition is adopted because of instrumentation requirements
- I_s Switching Current—Current which flows through the diode at V_S
- I_h Holding Current—The closest point to the minimum voltage in Region II where the slope of the V-I curve is −100Ω
- V_h Holding Voltage—Voltage across the diode at I_h
- I_p Peak Current—Current which the diode can pass when in Region III; duration limited to 50 μs
- R_{on} ON Resistance—Slope of V-I curve measured at currents > I_h
- I_{ik} Leakage Current—Measured in Region I at 60% V_S
- V_{rb} Reverse Breaker Voltage

DERATING CURVES



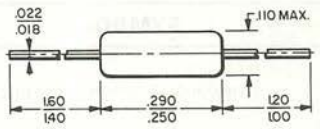


4-LAYER DIODE THYRISTORS

- **Firing Voltages 20 to 200 volts**
- **Switching current <125 μA @ 25°C**
- **ON resistance <2Ω @ 70mA**

The ITT diode thyristor is a reliable negative resistance device designed for use in switching circuits. Typical applications include ring counters, matrixes, pulse generators, relay drivers, multivibrators, pulse modulators, and timing circuits.

DIMENSIONS



DO-7

MECHANICAL DATA

Case:
Hermetically sealed glass

Finish:
All external surfaces corrosion resistant and leads readily solderable

Leads:
Dumet, tin plated

Weight:
0.135 grams (approx.)

Mounting Position:
Any

Marking:
Cathode band
Type number
Manufacturer's Symbol

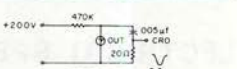
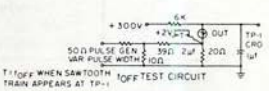
ELECTRICAL SPECIFICATIONS

TYPE	Switching Voltage (V_S) (Volts)	Holding Current (I_h) (mA)	Reverse Breakdown Voltage (Min.)
4E20-8	20±4	1-15	12
4E20-28	20±4	14-45	12
4E30-8	30±4	1-15	18
4E30-28	30±4	14-45	18
4E40-8	40±4	1-15	24
4E40-28	40±4	14-45	24
4E50-8	50±4	1-15	30
4E50-28	50±4	14-45	30
4E80-8	80±8V	1-15	48
4E80-28	80±8V	14-45	48
4E100-8	100±10	1-15	60
4E100-28	100±10	14-45	60
4E200-8	200±20 V	1-15	120
4E200-28	200±20 V	14-45	120
Series A (Broad Spec)			
4E20A	20±6	0.5-60	12
4E30A	30±6	0.5-60	18
4E40A	40±6	0.5-60	24
4E50A	50±6	0.5-60	30
4E80A	80±8	0.5-60	48
4E100A	100±10	0.5-60	60
4E200A	200±20	0.5-60	120

ABSOLUTE MAXIMUM RATINGS

CHARACTERISTICS		UNITS
Average Forward Current, 50°C	150	mA
Power Dissipation, 50°C	150	mW
Power-Temperature Derating	1.5	mW/°C
Reverse Breakdown Voltage from T_A = −40 to +70°C	nominal $V_S/2$	min.
Operating and Storage Temperature	−40 to +70	°C

ELECTRICAL CHARACTERISTICS @ 25°C unless otherwise noted

SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITIONS
I_S (forward switching current)			125 250	μA μA	 −60 to +125°C
I_{ik} (OFF state) (forward leakage current)			15	μA	75% of nom. V_S
V_{ON} (forward voltage drop)			1.4 1.2	V V	I_f = 70 mA@V_S 80, 100, 200 I_f = 70 mA@V_S 20, 30, 40, 50
r_{on} (dynamic forward impedance)			2.0	Ω	I_f = 70 mA
t_{on}		0.1		μsec	
t_{off}		5		μsec	

HOW THE 4-LAYER DIODE OPERATES

The voltage-current characteristic for the 4-layer diode shows three essential operating regions:

I—"off" or high resistance state

II—transition or negative resistance state

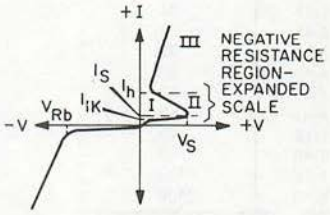
III—"on" or low resistance state

This curve is shown on a very expanded scale (non-linear) for illustration purposes only. Note that as the voltage rises and reaches the switching voltage (V_S), the device begins to switch "on." The current at this point (I_S) is typically several microamperes. The device switches because of an internal feedback mechanism allowing the diode to pass a steadily increasing current as the voltage decreases (negative resistance state, Region II). When "on" (Region III), the 4-layer diode passes a current which is limited principally by the external circuit.

In the "on" state, the device has a dynamic resistance of less than a few ohms and a voltage drop of about one volt. As long as sufficient current is passed by the circuit, the device will remain in the "on" condition. At the point on the curve marked I_h, the circuit is passing just enough current to keep the device in the "on" condition. If the current drops below I_h the diode switches back to the high resistance or "off" condition.

Rate Effect

In its "off" condition the device will pass a capacitive current in response to a sharply rising voltage wave. If the rise rate of this voltage wave is large enough (usually 10 to 100 volts / μS), switching occurs below the DC switching voltage.

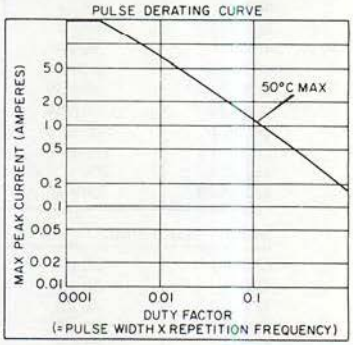


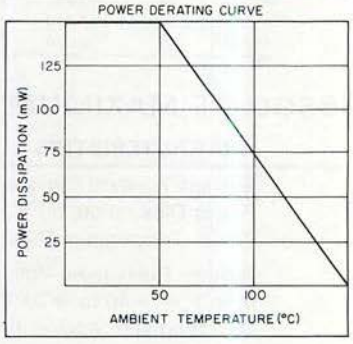
V-I CHARACTERISTICS

TERMS AND SYMBOLS

V_s	Switching Voltage—Closest point to peak voltage in Region II where slope of V-I curve is −330Ω. This definition is adopted because of instrumentation requirements
I_s	Switching Current—Current which flows through the diode at V_S
I_h	Holding Current—The closest point to the minimum voltage in Region II where the slope of the V-I curve is −100Ω
V_h	Holding Voltage—Voltage across the diode at I_h
I_p	Peak Current—Current which the diode can pass when in Region III; duration limited to 50 μs
R_{on}	ON Resistance—Slope of V-I curve measured at currents > I_h
I_{ik}	Leakage Current—Measured in Region I at 75% V_S
V_{rb}	Reverse Breaker Voltage

DERATING CURVES



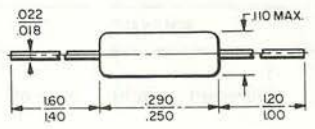


4-LAYER DIODE THYRISTORS

- **Firing Voltages 20 to 200 volts**
- **Switching current <125 μA @ 25°C**
- **ON resistance <2Ω @ 70mA**

The ITT diode thyristor is a reliable negative resistance device designed for use in switching circuits. Typical applications include ring counters, matrices, pulse generators, relay drivers, multivibrators, pulse modulators, and timing circuits.

DIMENSIONS



DO-7

MECHANICAL DATA

Case:
Hermetically sealed glass
Finish:
All external surfaces corrosion resistant and leads readily solderable
Leads:
Dumet, tin plated
Weight:
0.135 grams (approx.)
Mounting Position:
Any
Marking:

Cathode band
Type number
Manufacturer's Symbol

ELECTRICAL SPECIFICATIONS

Mil-Line Series for extended temperature ranges

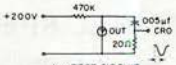
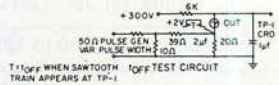
TYPE	Switching Voltage (V_S)		Holding Current (I_h) (mA) 25°C	Reverse Breakdown Voltage (Min.) −60 to 125°C
	25°C	−60 to 125°C		
4E20M-8	20±4	14-25	1-15	10
4E20M-28	20±4	14-25	14-45	10
4E30M-8	30±4	23-36	1-15	15
4E30M-28	30±4	23-36	14-45	15
4E40M-8	40±4	32-46	1-15	20
4E40M-28	40±4	32-46	14-45	20
4E50M-8	50±4	41-57	1-15	25
4E50M-28	50±4	41-57	14-45	25
4E30M-8	80±8	68-92	1-15	40
4E30M-28	80±8	68-92	14-45	40
4E100M-8	100±10	80-115	1-15	50
4E100M-28	100±10	80-115	14-45	50
4E200M-8	200±20	160-230	1-15	100
4E200M-28	200±20	160-230	14-45	100

ABSOLUTE MAXIMUM RATINGS

CHARACTERISTICS		UNITS
Average Forward Current, 50°C	150	mA
Power Dissipation, 50°C	150	mW
Power-Temperature Derating	1.5	mW/°C
Reverse Breakdown Voltage from T_A = −60 to +125°C	nominal $V_S/2$	min.
Operating and Storage Temperature	−60 to +125	°C

TYPE E 4E20M - 4E200M

ELECTRICAL CHARACTERISTICS @ 25°C unless otherwise noted

SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITIONS
I_S (forward switching current)			125 250	μA μA	−60 to +125°C
I_{ik} (OFF state) (forward leakage current)			15	μA	75% of nom. V_S
V_{ON} (forward voltage drop)			1.4 1.2	V V	I_f = 70 mA@V_S 80, 100, 200 I_f = 70 mA@V_S 20, 30, 40, 50
r_{on} (dynamic forward impedance)			2.0	Ω	I_f = 70 mA
t_{on}		0.1		μsec	 t_{ON} TEST CIRCUIT
t_{off}		5		μsec	 $T = t_{OFF}$ WHEN SAWTOOTH TRAIN APPEARS AT TP-1 t_{OFF} TEST CIRCUIT

HOW THE 4-LAYER DIODE OPERATES

The voltage-current characteristic for the 4-layer diode shows three essential operating regions:

I—"off" or high resistance state

II—transition or negative resistance state

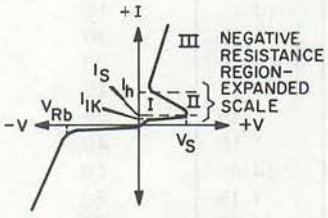
III—"on" or low resistance state

This curve is shown on a very expanded scale (non-linear) for illustration purposes only. Note that as the voltage rises and reaches the switching voltage (V_S), the device begins to switch "on." The current at this point (I_S) is typically several microamperes. The device switches because of an internal feedback mechanism allowing the diode to pass a steadily increasing current as the voltage decreases (negative resistance state, Region II). When "on" (Region III), the 4-layer diode passes a current which is limited principally by the external circuit.

In the "on" state, the device has a dynamic resistance of less than a few ohms and a voltage drop of about one volt. As long as sufficient current is passed by the circuit, the device will remain in the "on" condition. At the point on the curve marked I_h, the circuit is passing just enough current to keep the device in the "on" condition. If the current drops below I_h the diode switches back to the high resistance or "off" condition.

Rate Effect

In its "off" condition the device will pass a capacitive current in response to a sharply rising voltage wave. If the rise rate of this voltage wave is large enough (usually 10 to 100 volts / μS), switching occurs below the DC switching voltage.

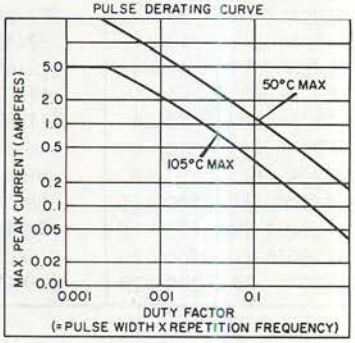


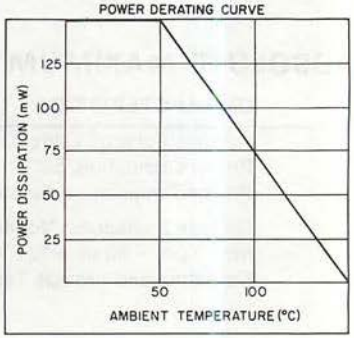
V-I CHARACTERISTICS

TERMS AND SYMBOLS

- V_s Switching Voltage—Closest point to p… voltage in Region II where slope of … curve is −330Ω. This definition is adopte… because of instrumentation requirements
- I_s Switching Current—Current which flows through the diode at V_S
- I_h Holding Current—The closest point to the minimum voltage in Region II where the slope of the V-I curve is −100Ω
- V_h Holding Voltage—Voltage across the diode at I_h
- I_p Peak Current—Current which the diode can pass when in Region III; duration limited to 50 μs
- R_{on} ON Resistance—Slope of V-I curve measured at currents > I_h
- I_{ik} Leakage Current—Measured in Region I at 75% V_S
- V_{rb} Reverse Breaker Voltage

DERATING CURVES





TWENTY-FOUR CIRCUIT APPLICATIONS FOR ITT 4-LAYER DIODES

THEORY OF OPERATION

The ITT Semiconductor Four-Layer Diode is a two-terminal semiconductor switch, sometimes referred to as a negative-resistance diode. These PNPN silicon devices are useful in many applications including pulse generators, oscillators, telephone switching, sweep generators, and multivibrators.

The diode has two stable states; the ON or low impedance state, and the OFF or high impedance state. To turn the device ON, voltage across the terminals must exceed the switching voltage (V_s). The device can be turned OFF by reducing the current through the device below the holding current (I_h).

Figure 1

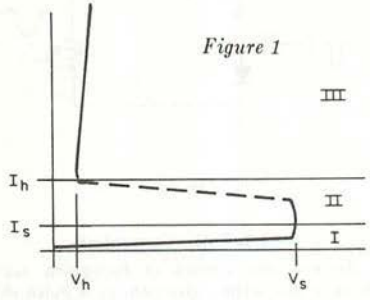


Figure 1 is the V-I characteristic of a typical device. V_s is the point at which the device breaks down and switches to the ON state where current is limited only by the external circuit impedance.

I_h is the minimum current that must be passed through the diode to keep it in the ON state. If the current drops below this value the diode will switch to the OFF state.

Figure 2A

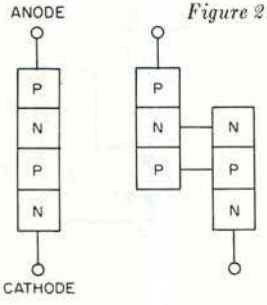
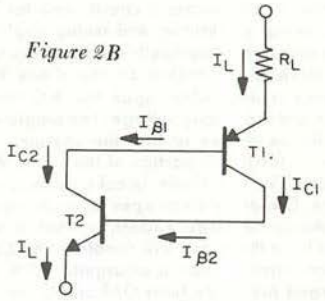


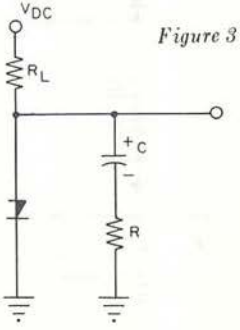
Figure 2B



The PNPN diode can be thought of as a complimentary pair of transistors, one a PNP and the other an NPN as shown in Figure 2A. Figure 2B shows the two transistors as they would appear schematically. The collector of T_2 drives the base of T_1 giving rise to a positive feedback loop with a gain of B_1B_2. As long as B_1B_2 is less than 1 the equivalent circuit is stable with the upper and lower PN junctions biased forward and the middle junction reversed biased. In this condition only a small leakage current flows.

The diode will remain in this condition until either the temperature or the anode voltage is increased to a point where $B_1B_2 = 1$. At this point, the middle junction breaks down and the circuit becomes regenerative. This occurs because the collector of each transistor supplies current to the base of the complimentary transistor in the equivalent circuit and their Betas are current dependent. As soon as they reach unity the device effectively "runs away" or "fires" and the current through the circuit is limited only by external impedance.

Figure 3

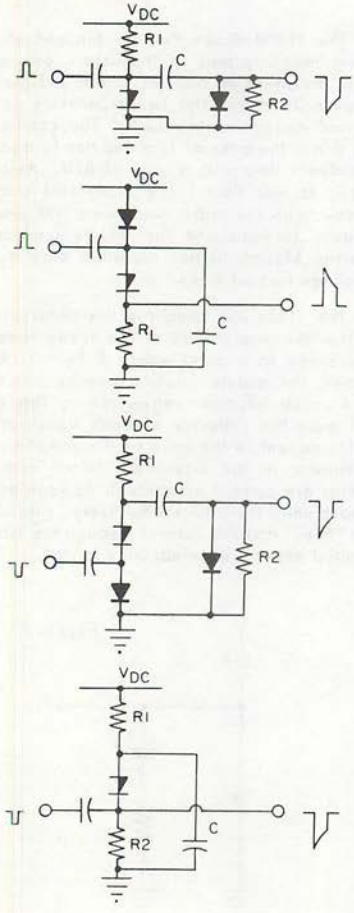


**Application notes will be found in the last pages of this section.

CIRCUITS

Relaxation Oscillator

Figure 3 illustrates a circuit used for oscillator, sweep generator, and timing applications. The output is a saw-tooth voltage the amplitude of which is dependent on the diode V_s. Frequency is dependent upon the $R_L C$ time constant and the supply voltage. The supply voltage should be chosen so that the charging of C is done in the linear portion of the curve. When C reaches V_s the diode breaks down and conducts. C rapidly discharges through the diode. R_L should be large enough so that it will not pass I_h or the diode will remain in the ON condition after C has discharged. With C discharged the diode turns OFF and C commences to charge again. R_L must be able to pass the switching current (I_s) when C reaches V_s and the diode fires again.



Triggered Pulse Generators

These circuits are used mainly for generating or amplifying pulses and for triggering purposes. They are similar to Figure 3 except that the switching voltage of the diode is greater than the supply voltage. Four variations, with their input and output pulses, are shown in Figure 4. A pulse, large enough to break down the diode, is capacitively coupled either positive to the anode or negative to the cathode. The conventional diode is used to present a high impedance to the input pulse.

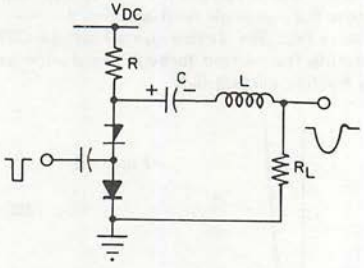
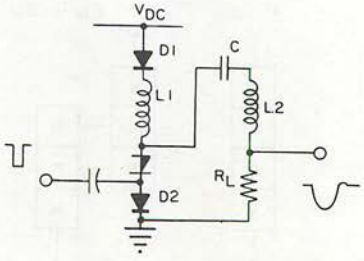


Figure 5

L-C Pulse Generators

As with the circuits in foregoing section, those in this section also require a pulse to fire the diode. V_s of the diode is greater than the supply voltage. In Figure 5, a negative pulse is applied to the cathode which breaks down the diode. C, which was charged to V_{DC} through R, discharges through the diode, L, and R_L. This is a resonant circuit and the wave shape across R_L is a half sinusoid. When the current goes through zero, the voltage across the diode becomes negative, turning it OFF. A small positive output will occur due to the pulse recovery current through the diode.

Figure 6



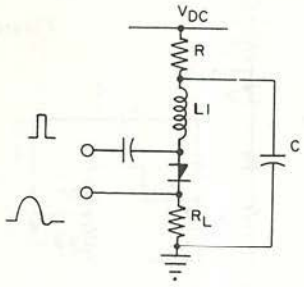


Figure 7

This type of generator does not depend on R being large enough not to pass I_h but rather on the fact that ringing of the L-C loop turns OFF the diode. During the OFF half cycle C charges to V_{DC} but in the opposite polarity. With the completion of the output pulse and the cessation of ringing, C begins to recharge toward the power supply voltage and polarity. Figures 6 and 7 illustrate the same principle but with a resonant charging circuit. C may charge to approximately twice the supply voltage if the circuit Q is high. The resistance of L must be large enough to keep the current through the four-layer diode below its rated maximum. The anode of the diode must be kept negative long enough to turn completely OFF, otherwise the diode will turn back ON when the anode goes positive. This requirement limits the maximum operating repetition rate.

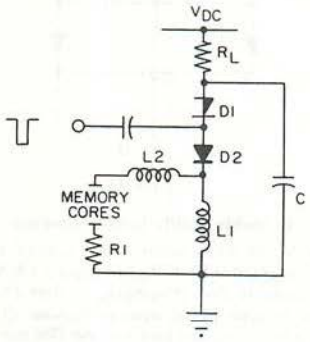


Figure 8

Magnetic Memory Driver Circuits

The purpose of a magnetic memory driving circuit is to provide a current wave form which reads the memory and then restores (writes) the initial flux condition. In Figure 8, the V_s of the four-layer diode is greater than V_{DC}. C charges to V_{DC} through R_L When a negative pulse of the proper magnitude is coupled to the cathode, the four-layer diode (D_1) conducts. R_L is made large enough so that it will not deliver the minimum I_h. C discharges through the four-layer diode (D_1) the conventional diode (D_2), and the inductive load. C must be large enough to supply the "read" peak current. The shape of the curve is dependent on the inductances and R_1. The R_LC product must be selected so that C charges in less time than the time from the end of the "read" pulse to the beginning of the next complete cycle.

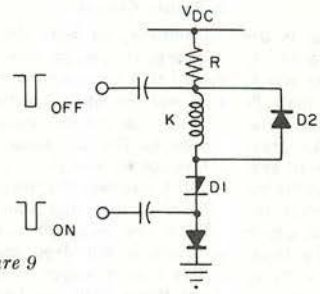


Figure 9

Relay Drivers

In Figure 9, V_s is greater than V_{DC}. A negative pulse on the cathode turns D_1 ON. It remains in this state until it is pulsed OFF by a negative pulse on the anode. This is a typical relay driver application. D_2 prevents excessive spiking caused by the relay inductance.

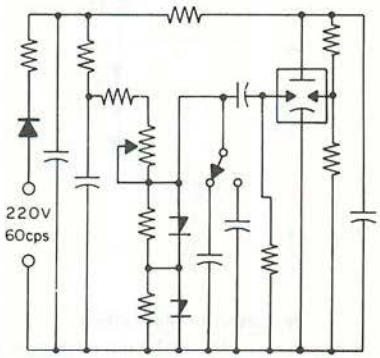


Figure 10

Stroboscope

In Figure 10, the four-layer diodes replace thyratrons as triggers to activate a stroboscope flash tube. The diodes form a relaxation oscillator delivering pulses up to 150V at a few hundred per second depending on the circuit constants. Because of the pulse magnitude two diodes are used in series with equalizing resistors across them.

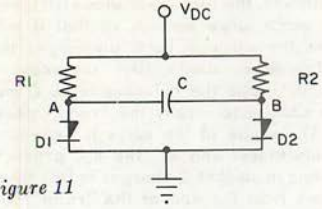


Figure 11

A-Stable Circuit

V_{DC} is greater than V_s of both diodes in Figure 11. When power is applied, one of the diodes will conduct. Let it be assumed that D_1 fires first. Point A will go approximately to ground potential and the current through R_1 will be greater than I_h. The capacitor C will begin to charge through R_2 and D_1 to ground. When the voltage at B exceeds the breakdown potential of D_2, it will conduct and point B will go to ground. Since the capacitor can not charge instantly, point A will drop approximately V_s volts. This puts a negative voltage at A, which if kept there until the turn OFF potential of D_1 is reached, will prevent it from switching back until the voltage at A reaches V_s. C therefore charges through R_1. The circuit oscillates back and forth from D_1 to D_2 with the frequency dependent on R_1C and R_2C and on V_{DC} and the switching voltage of the diodes.

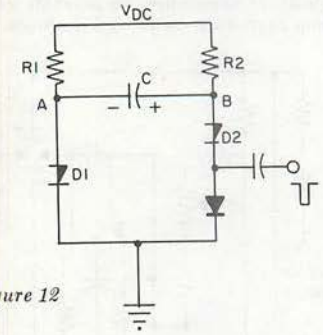


Figure 12

Monostable Multivibrator

If diode D_1 in Figure 12 is selected so that its switching voltage is less than V_{DC}, and diode D_2's is greater than V_{DC}, diode D_1 will normally be in the ON condition and D_2 will be OFF. Capacitor C will charge through R_2. When D_2 is pulsed ON, D_1 will turn OFF due to the commutating action of C. The voltage at point A will then start rising as C charges through R_1 and D_2. When the voltage at point A reaches the switchover voltage of D_1 it will turn ON and D_2 will turn OFF until another pulse is received. Frequency is determined by R_1C, V_{DC}, and V_s of diode D_1.

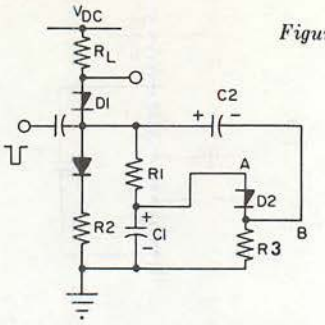


Figure 13

A modification of the gate circuit where both diodes are in the OFF state until a pulse is applied is shown in Figure 13. The V_s of D_1 is slightly higher than V_{DC}. A pulse of current is applied through R_L which turns D_1 ON. C_2 charges through D_1 and R_2 to V_{DC}. C_1 charges through R_1 and D_1 toward V_{DC} also. When the voltage at point A reaches V_s of D_2, it will commence to conduct. The voltage rise at B is commutated back to D_1, turning it OFF, which in turn, turns OFF D_2.

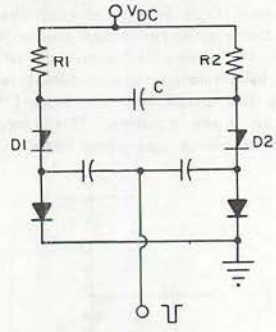


Figure 14

Bi-Stable Multivibrator Flip-Flop

The V_s of both diodes are chosen so that they are greater than V_{DC} in Figure 14. Whichever diode is ON, it remains in that condition until a trigger pulse arrives turning OFF the diode which was ON and turning ON the previously OFF diode by the commutating action of C.

By interchanging one 4-layer diode with its series cathode diode, the circuit will become sensitive to the polarity of the pulses. The circuit will then switchover only when the polarity of the trigger pulse reverses. This is shown in Figure 15. Diode 1 triggers on negative pulses only and diode 2 on positive pulses. Therefore, a positive pulse keeps branch B ON and a negative pulse keeps branch A ON.

Figure 15

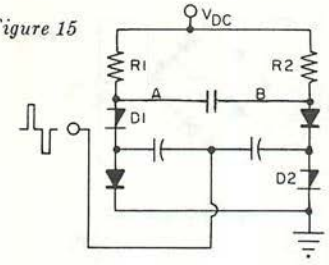
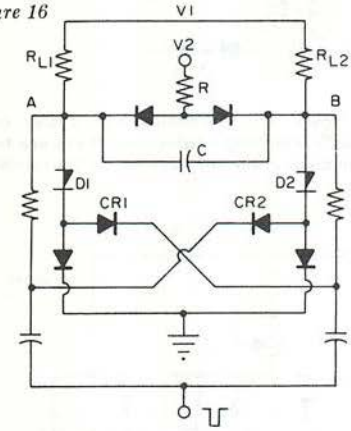
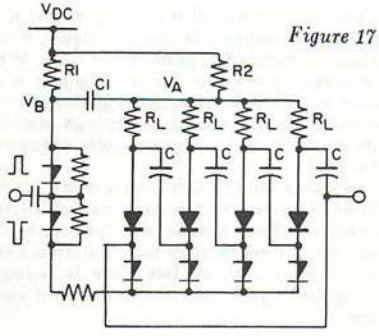


Figure 16



A different steering circuit is shown in Figure 16. Assume that D_1 is ON. Point A will be approximately at ground potential and point B at V_1. When a negative pulse is applied it is blocked by CR_1 but passes through CR_2, causing switchover to take place. Current from V_2 passes through R and D_2 to ground. The principal source of current for the conducting branch is V_2. The R_L's are needed to maintain a voltage of less than V_s across the OFF diode.

Figure 17



Ring Counters

The basic requirement of a ring counter is to turn one stage at a time ON in a simple progression. Each time a trigger pulse is applied, the ON stage will advance one stage. The circuit forms a closed loop, or ring, so that when the final stage has been activated the next pulse will move the ON condition back to the first stage where the cycle begins over again. In Figure 17, one stage will turn ON as soon as power is applied. The commutating capacitor C between the ON stage and the next successive stage charges through R_L and the ON 4-layer diode to V_A, which is less than the V_s of the diodes and keeps them from turning ON. A trigger pulse, either positive or negative, causes V_B to drop almost to ground potential, which in turn, causes V_A to drop at the same time due to the coupling action of C_1. Since R_1 is large enough so that a current of less than I_h flows through the trigger diodes, the pulse is only momentary. The drop in voltage at A turns OFF the ON diode. At the same time C_1 begins to charge and the voltage at A rises again.

The voltage at the high end of the charged commutating capacitor C adds to V_A causing the next stage to fire. The repetition rate of the output pulses equals the rate of the trigger pulses divided by the number of stages.

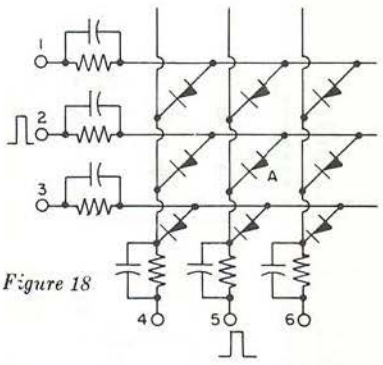


Figure 18

Telephone Switching

When trigger signals of the polarity shown in Figure 18 are simultaneously applied to the lines, one of positive polarity to lines 1, 2, or 3, and the other of negative polarity to lines 4, 5, or 6, two of the lines will be connected. If triggers are applied to lines 2 and 5 as shown, the 4-layer diode A will conduct connecting them together. The series resistors allow a current greater than I_h to flow, thus keeping the diode in the ON state. To open the circuit, a contact is opened to interrupt the flow of current through the diode which will then revert to its OFF condition.

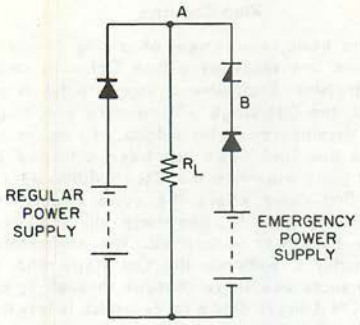


Figure 19

Emergency Power Transfer

In the normal state, the 4-layer diode in Figure 19 is OFF and the regular power supply is the source of power for the load R_L. If the supply voltage should fall off for any reason, the voltage at point A will drop. If this change in voltage is sufficient to cause the potential from B to A to exceed the diode V_s, it will turn ON and the emergency power supply will provide power to the load until the condition is corrected.

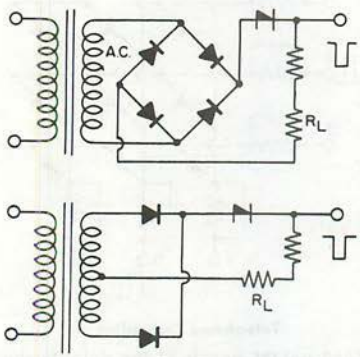


Figure 20

Rectifier Control Circuits

Figure 20 illustrates a method for controlling the power output of a rectifier by varying the point at which a 4-layer diode is triggered. Pulses may be applied at any phase angle from the start of the input waveform (100% power) to 180° (zero power).

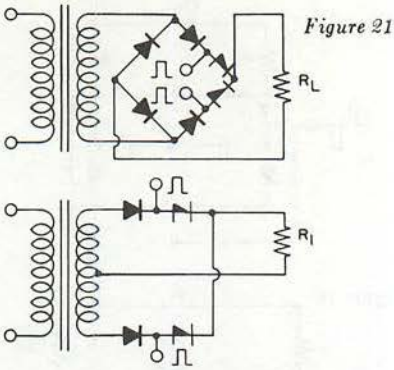


Figure 21

In Figure 21, succeeding half cycles can have different firing angles since there are two control diodes, one for each leg of the rectifier circuit.

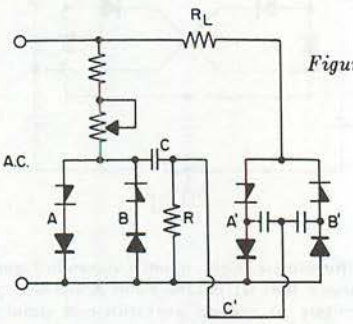


Figure 22

AC Control Circuits

The circuit in Figure 22 is useful for the control of AC power in such applications as light dimmers and motor controls. The trigger portion is composed of two back-to-back relaxation oscillators with an adjustable resistor controlling the time at which they fire the control diodes and thus the amount of current through the load.

The load resistor of the oscillator and C set up the time constant to fire the trigger diodes at approximately 90° in each half cycle. When a positive input cycle occurs the diode A will break down at approximately 90°. The charged capacitor C will discharge through diode A with the result that a negative pulse will appear at point C_1.

This pulse will turn ON control diode A_1 which will allow current to flow until the half cycle is completed. Both diodes will then turn OFF since the current through them will drop below their holding current. This cycle is repeated during the negative portion of the input waveform.

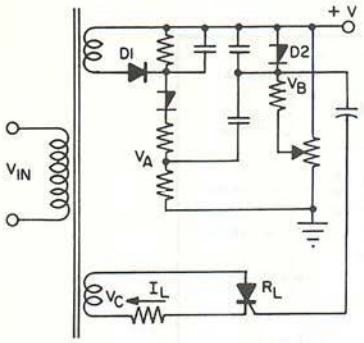


Figure 23

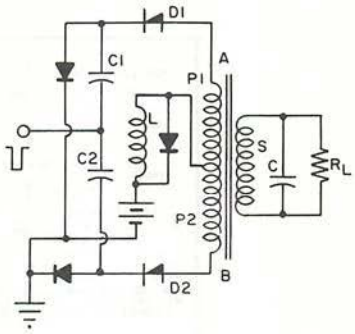


Figure 24

SCR Phasing Circuit

Diode 1 and 2 are both designed into relaxation oscillator circuits in Figure 23. The diode 1 circuit has a frequency of just under 60 cycles per second. The half-wave supply circuit at its anode causes the frequency of the oscillator to be synchronized with the line frequency. The output at V_A is a sawtooth which is coupled to the cathode of D_2. It is superimposed on a DC value set by the potentiometer in the cathode of D_2. As the voltage across D_2 is increased by decreasing the cathode potential, the negative peak of the waveform from D_1 will exceed V_s of D_2 putting it into oscillation at a frequency much greater than that of D_1. This signal is fed to the gate of the SCR which is fired by the steep wave front at the start of oscillations. The timing of the conduction of the SCR is controlled by the setting of the potentiometer.

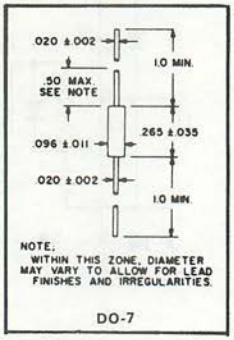
Inverter Circuits

The circuit in Figure 24 is a typical power inverter used to convert DC power to AC power over a range of frequency from 60 to a few thousand cycles. When power is applied, one of the 4-layer diodes begins to conduct. Assume this to be D_1. The battery supplies current through the coil L, primary 1 and D_1. The reflected load limits the current through D_1.

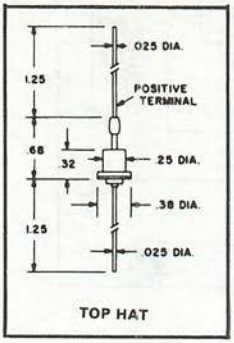
When a negative trigger pulse is applied D_2 will conduct. The commutating capacitor C which is reflected into the primary from across R_L will cause point A to go negative thus turning OFF D_1. L smooths the current during switching. The following negative trigger pulse turns D_1 ON again and C turns D_2 OFF. This completes one cycle.

The switchover voltage of the diodes must be greater than $2XV_{DC}$ and capacitor C must be big enough so that when reflected back into the primary it can turn OFF the diode which was ON just prior to the triggering pulse. The capacitor can be across the primary or the secondary.

THYRISTOR DIODES



DO-7



TOP HAT

DO-7 PACKAGE

TYPE	Switching Voltage (V_s) (Volts) 25°C	−40 to 85°C	Holding Current (I_h) (Milliamps) 25°C	−40°C	Reverse Breakdown 25°C	Capacitance (Typical) 0V Bias
1N3831	20 ± 4	14-25	0.5-15	40 max	12v min	80 pf
1N3832	25 ± 4	19-30	0.5-15	40 max	15v min	70 pf
1N3833	30 ± 4	23-36	0.5-15	40 max	18v min	60 pf
1N3834	35 ± 4	28-41	0.5-15	40 max	21v min	50 pf
1N3835	40 ± 4	32-46	0.5-15	40 max	24v min	45 pf
1N3836	45 ± 4	37-51	0.5-15	40 max	27v min	45 pf
1N3837	50 ± 4	41-57	0.5-15	40 max	30v min	40 pf
1N3838	100 ± 10	80-115	0.5-15	40 max	60v min	30 pf

TYPE	Switching Voltage (V_s) (Volts) 25°C	−40 to 58°C	Holding Current (I_h) (Milliamps) 25°C	85°C	Reverse Breakdown 25°C	Capacitance (Typical) 0V Bias
1N3839	20 ± 4	14-25	14-50	5 min	12v min	80 pf
1N3840	25 ± 4	19-30	14-50	5 min	15v min	70 pf
1N3841	30 ± 4	23-36	14-50	5 min	18v min	60 pf
1N3842	35 ± 4	24-81	14-50	5 min	21v min	50 pf
1N3843	40 ± 4	32-46	14-50	5 min	24v min	45 pf
1N3844	45 ± 4	37-51	14-50	5 min	27v min	45 pf
1N3845	50 ± 4	41-57	14-50	5 min	30v min	40 pf
1N3846	100 ± 10	80-115	14-50	5 min	60v min	30 pf

Commercial Series

TYPE	Switching Voltage (V_s) (Volts)	Holding Current (I_h) (mA)
4E20-8	20 ± 4	1-15
4E20-28	20 ± 4	14-45
4E30-8	30 ± 4	1-15
4E30-28	30 ± 4	14-45
4E40-8	40 ± 4	1-15
4E40-28	40 ± 4	14-45
4E50-8	50 ± 4	1-15
4E50-28	50 ± 4	14-45
4E100-8	100 ± 10	1-15
4E100-28	100 ± 10	14-45
4E200-8	200 ± 20	1-15
4E200-28	200 ± 20	14-15

Mil-Line Series for extended temperature ranges

TYPE	Switching Voltage (V_s) 25°C	−60 to 125°C	Holding Current (I_h) (mA)
4E20M-8	20 ± 4	14-25	1-15
4E20M-28	20 ± 4	14-25	14-45
4E30M-8	30 ± 4	23-36	1-15
4E30M-28	30 ± 4	23-36	14-45
4E40M-8	40 ± 4	32-46	1-15
4E40M-28	40 ± 4	32-46	14-45
4E50M-8	50 ± 4	41-57	1-15
4E50M-28	50 ± 4	41-57	14-45
4E100M-8	100 ± 10	80-115	1-15
4E100M-28	100 ± 10	80-115	14-45
4E200M-8	200 ± 20	160-230	1-15
4E200M-28	200 ± 20	160-230	14-45

Series A (Broad Spec)

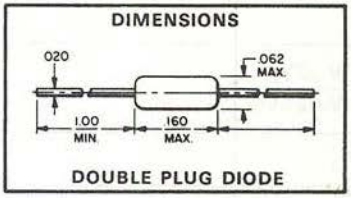
TYPE	Switching Voltage (V_s) (Volts)	Holding Current (I_h) (mA)
4E20A	20 ± 6	0.5-60
4E30A	30 ± 6	0.5-60
4E40A	40 ± 6	0.5-60
4E50A	50 ± 6	0.5-60

TOP-HAT PACKAGE—TYPE J

TYPE	Switching Voltage (V_s) (Volts)	Holding Current (I_h) (mA)
4J50-5	50 ± 5	1-10
4J50-25	50 ± 5	9-45
4J100-5	100 ± 10	1-10
4J100-25	100 ± 10	9-45
4J200-5	200 ± 20	1-10
4J200-25	200 ± 20	9-45

Current Carrying Capacity: 300 mA steady dc.
Maximum peak current rating 20 amperes — dependent on duty factor, repetition rate, pulse duration, ambient temperature.

SILICON PLANAR EPITAXIAL TUNER DIODE



The ITT silicon planar epitaxial tuner diode is intended for television receiver tuner applications where three or four units will provide complete coverage of the VHF broadcast bands respectively. The high guaranteed capacitance ratio of these diodes allows design of electronically tuned FM tuners for 12V operation.

ABSOLUTE MAXIMUM RATINGS

		UNITS
Power dissipation @ 50°C	150	mW
Operating temperature range	0 to 90	°C
Storage temperature range	0 to 100	°C
Peak reverse voltage	30	Volts

ELECTRICAL CHARACTERISTICS (T_j = 25°C unless otherwise specified)

SYMBOL		ITT 109			UNITS	CONDITIONS
		MIN.	TYP.	MAX.		
C_J			30.0		pF	V_R = 3V
		4.2		6.5	pF	V_R = 25V
$\frac{C(V=3V)}{C(V=25V)}$		5				
R_S			0.5		Ohms	V_R = 3V, f = 100 MHz
Q		200	280			V_R = 3V, f = 47MHz
		90				V_R = 3V, f = 100MHz
		55				V_R = 3V, f = 170MHz
L_S			2.5 nH			
I_R				0.5	μA	V_R = 28V

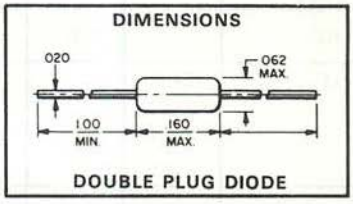
NOTES:

The error of matching in capacitance within a matched set in the voltage range V = 3 . . . 25 Volts is ± 1.5%.

These diodes are available on request in matched sets of any desired capacitance tolerance between 0 and 25 Volts for special applications.

SILICON PLANAR EPITAXIAL TUNER DIODES (LOW INDUCTANCE)

ITT silicon planar epitaxial tuner diodes are intended for television receiver tuner applications where three or four units will provide complete coverage of the VHF and UHF broadcast bands respectively. The high guaranteed capacitance ratio of these diodes allows design of electronically tuned FM tuners for 12V operation.



ABSOLUTE MAXIMUM RATINGS

CHARACTERISTICS		UNITS
Power dissipation @ 50°C	150	mW
Operating temperature range	0 to 90	°C
Storage temperature range	0 to 100	°C
Peak reverse voltage	30	Volts
Soldering temperature (5 secs. at body of diode package)	260	°C

ELECTRICAL CHARACTERISTICS ($T_j = 25°C$ unless otherwise specified)

SYMBOL	ITT 141			ITT 142			UNITS	CONDITIONS
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.		
C_J		11			12		pF	$V_R = 3V$
		2.2	2.5	2.0	2.5	3.0	pF	$V_R = 25V$
$\frac{C_{3.0V}}{C_{25V}}$	4.5	4.8	5.5 5.2	4.0	4.8	6.0		
R_S		0.5			1.0		Ohms	$V_R = 3V$, f = 330 MHz
Q	300			160				$V_R = 3V$, f=47MHz
				80				$V_R = 3V$, f=100MHz
	80			50				$V_R = 3V$, f=170MHz
	30							$V_R = 3V$, f=470MHz
f_c	20			10			GHz	$V_R = 3V$, Q = 1.0
f_o	2.5			2.2			GHz	$V_R = 25V$
L_S		2.5			2.5		nH	At body of diode package
V_{BR}	30			30			Volts	
I_R			5.0			5.0	μA	$V_R = 28V$

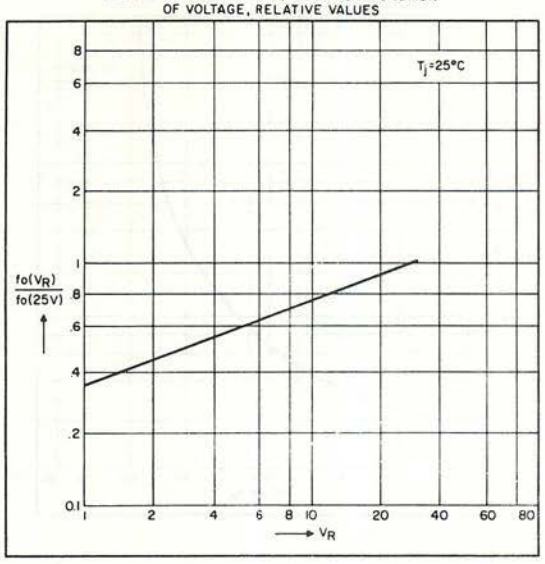
NOTES:

The error of matching in capacitance within a matched set in the voltage range V = 3 . . . 25 Volts is ± 1.5%.

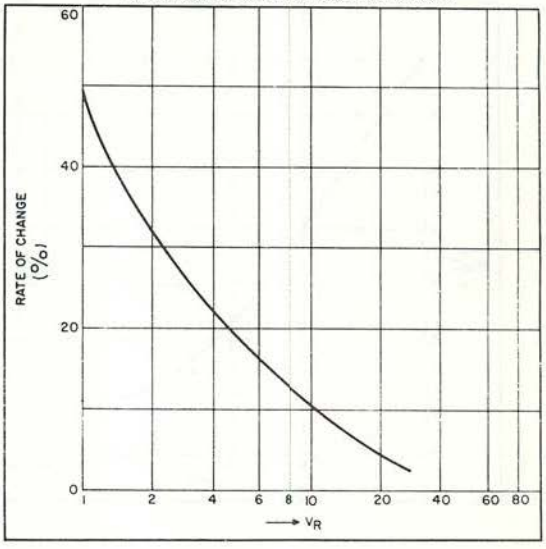
These diodes are available on request in matched sets of any desired capacitance tolerance between 0 and 25 Volts for special applications.

TYPICAL CHARACTERISTICS

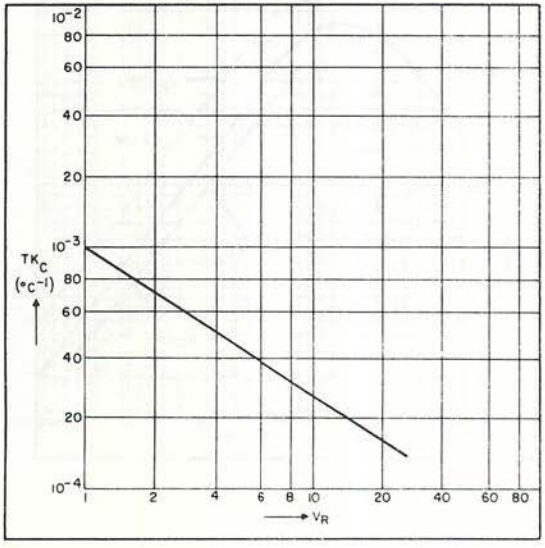
SERIES RESONANCE FREQUENCY AS A FUNCTION OF VOLTAGE, RELATIVE VALUES



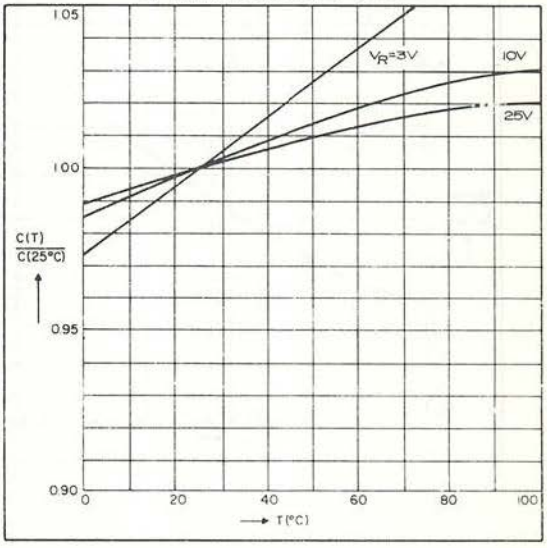
RATE OF CHANGE OF CAPACITANCE VS. VOLTAGE.



TEMPERATURE COEFFICIENT AS A FUNCTION OF VOLTAGE, RELATIVE VALUES

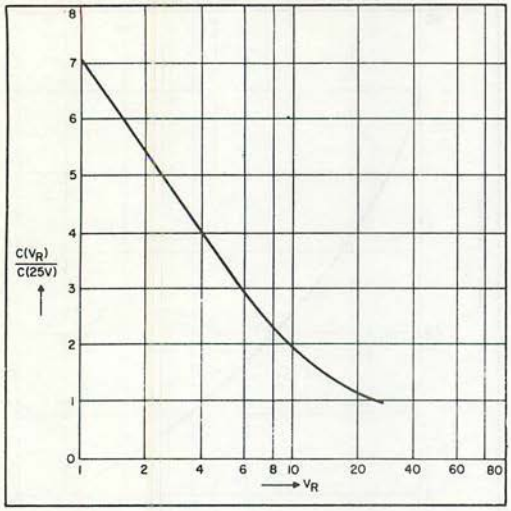


CAPACITANCE AS A FUNCTION OF TEMPERATURE, RELATIVE VALUES

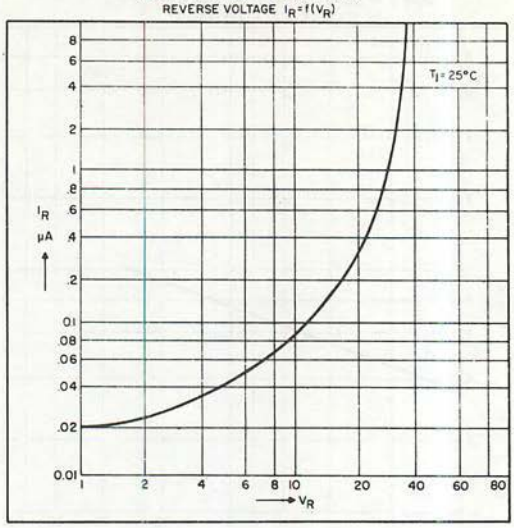


TYPICAL CHARACTERISTICS, continued

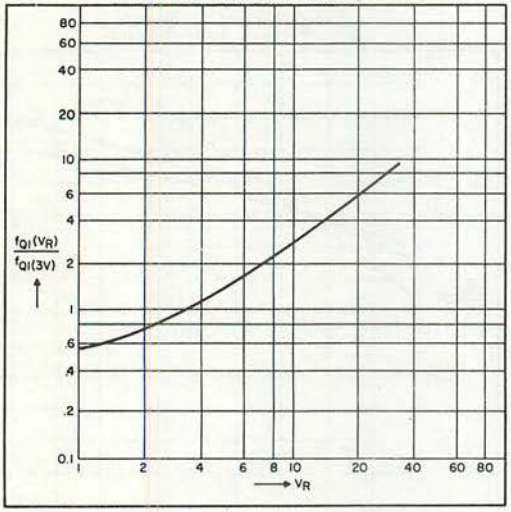
JUNCTION CAPACITANCE (C) AS A FUNCTION OF VOLTAGE, RELATIVE VALUES



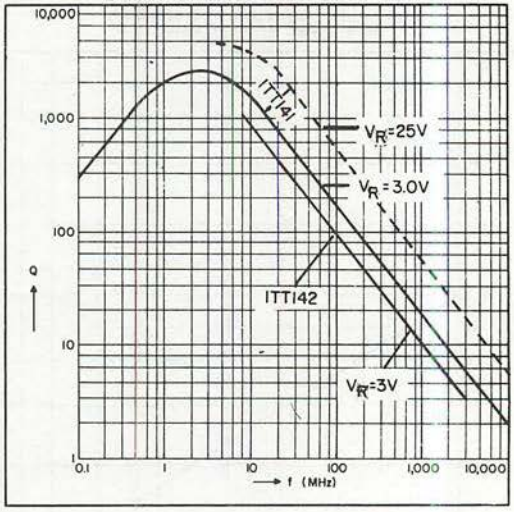
REVERSE CURRENT AS FUNCTION OF REVERSE VOLTAGE $I_R = f(V_R)$



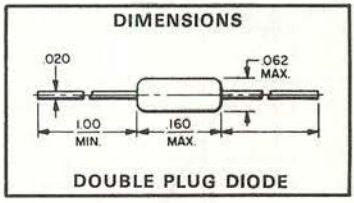
CUTOFF FREQUENCY (fc) AS A FUNCTION OF VOLTAGE, RELATIVE VALUES



Q-FACTOR AS FUNCTION OF FREQUENCY Q = f(f)



SILICON PLANAR EPITAXIAL CAPACITANCE DIODE



The ITT-210 is an improved variable capacitance diode intended for television receiver Automatic Frequency Control and other tuning applications between 1 and 1,000 MHz.

ABSOLUTE MAXIMUM RATINGS

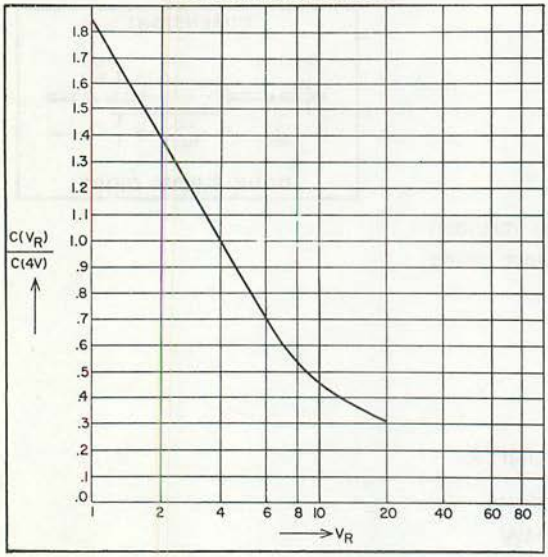
CHARACTERISTICS		UNITS
Reverse Voltage Breakdown @ 5μa	20	Volts
Power Dissipation @ 50°C	150	MW
Operating Temperature Range	0 to 100	°C
Storage Temperature Range	−50 to + 150	°C

ELECTRICAL CHARACTERISTICS @ 25°C unless otherwise noted.

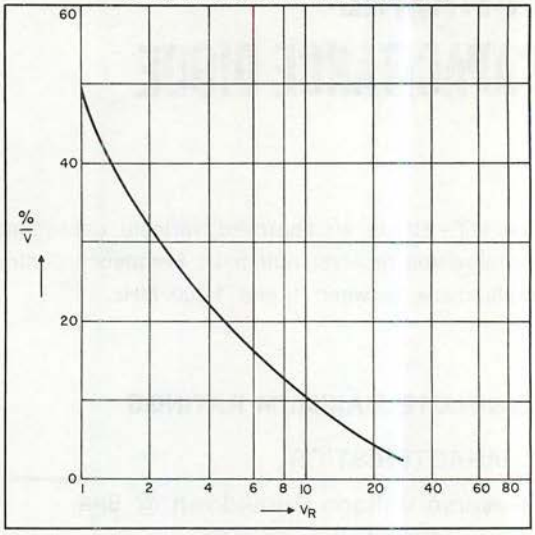
SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITIONS
C	8	20	12	pF	$V_r = 1.0V$
		10		pF	$V_r = 4V$
		8.3		pF	$V_r = 6V$
		5		pF	$V_r = 10V$
Rs		1.0		ohms	F = 30 MHz $V_r = 2V$
Q		540			F = 30 MHz $V_r = 5V$
V_F		.85	1.5	V.	$I_F = 60mA$

TYPICAL CHARACTERISTICS

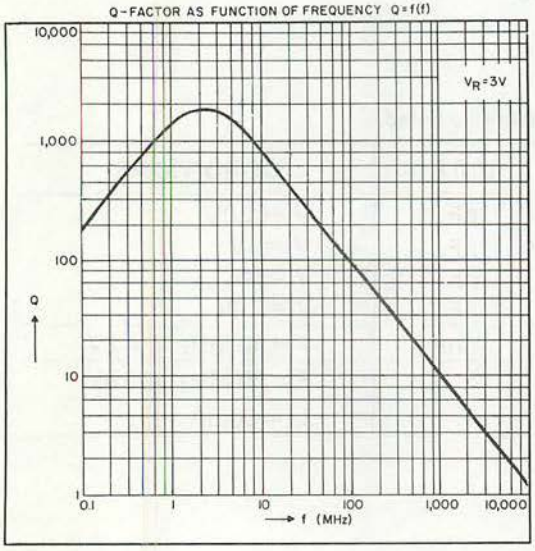
JUNCTION CAPACITANCE (C) AS A FUNCTION OF VOLTAGE, RELATIVE VALUES



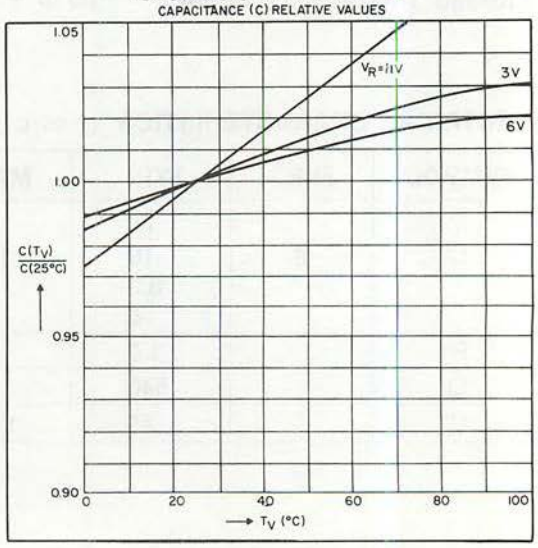
RATE OF CHANGE OF CAPACITANCE VS. VOLTAGE.



Q-FACTOR AS FUNCTION OF FREQUENCY Q=f(f)

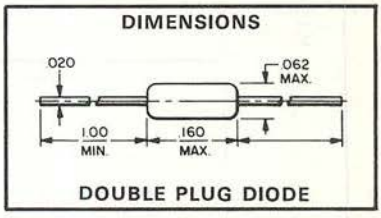


TEMPERATURE AS FUNCTION OF JUNCTION CAPACITANCE (C) RELATIVE VALUES



UHF/VHF WAVE BAND SWITCH

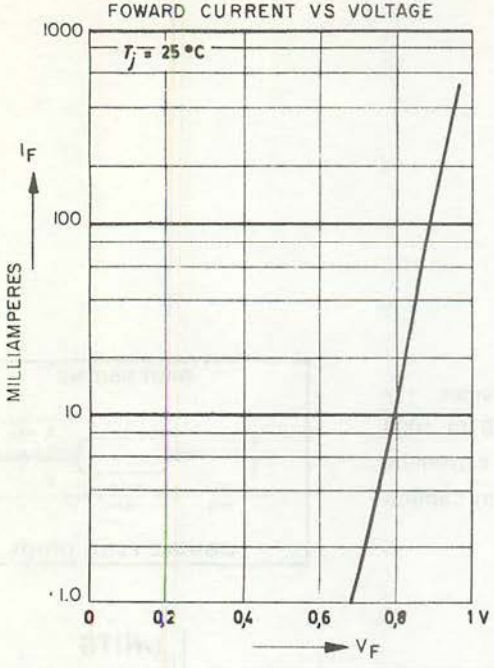
The ITT 243/244 is intended to replace mechanical devices, for switching channels or bands, in the frequency range of 10 to 1000 MHz. The differential forward resistance is constant and extremely small over a wide frequency and current range. The junction capacitance is small and relatively independent of voltage.



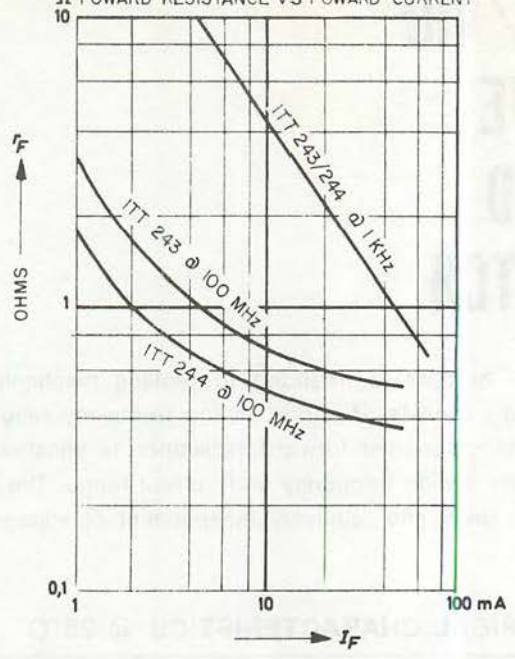
ELECTRICAL CHARACTERISTICS @ 25°C	UNITS
Reverse Voltage (Vr)	20 Volts
Forward Current (If)	100 mA
Forward Voltage (Vf) @ If = 100 mA	<1 Volt
Reverse Current (Ir) @ Vr = 15 V	<100 n Amps
Junction Temperature (Tj)	100°C
Storage Temperature (Ts)	− 55 to + 100°C

DYNAMIC CHARACTERISTICS @ 25°C	ITT 244	ITT 243
Differential Forward Resistance @ f = 50 to 1000 MHz @ If = 10 mA	0.5Ω (TYP 0.4Ω)	1Ω (TYP 0.7Ω)
Relative Change of Forward Resistance with change in Forward Current	3%/mA	5%/mA
Junction Capacitance @ Vr = 15V	< 2.2 Pf	< 2.2 Pf
Relative Change of Junction Capacitance with change of reverse voltage	1%/V	1%/V
Series Inductance (case)	< 2.5 nH	< 2.5 nH
Parallel Resistance (Rp) @ Vr = 15V	1 MΩ	1 MΩ

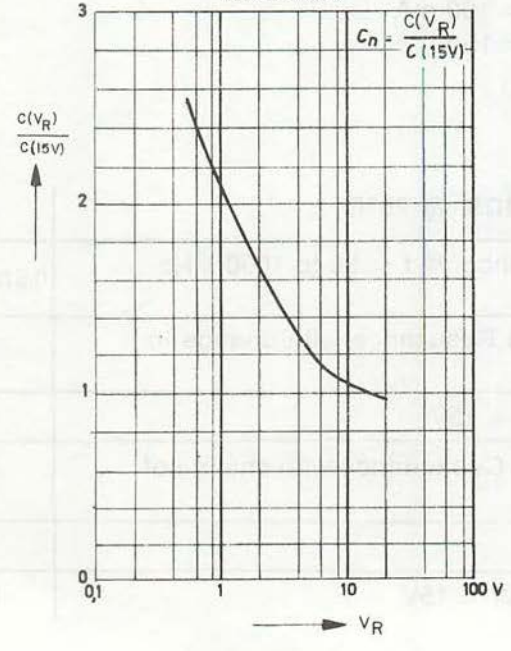
FOWARD CURRENT VS VOLTAGE



Ω FOWARD RESISTANCE VS FOWARD CURRENT



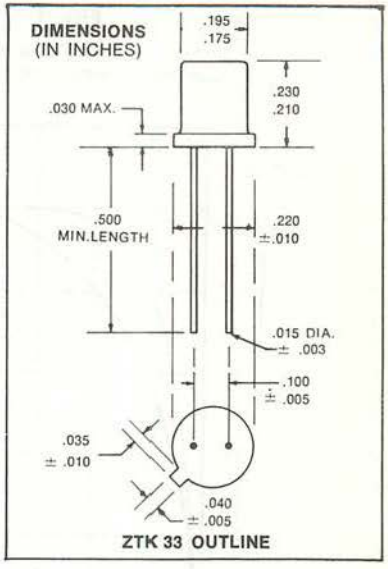
CAPACITANCE AS A FUNCTION OF VOLTAGE, RELATIVE VALUES



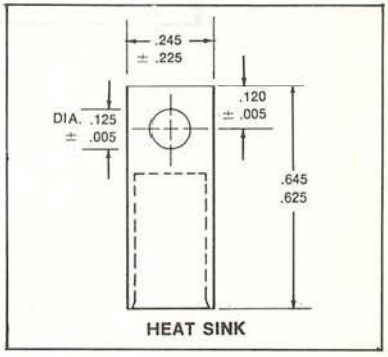
MONOLITHIC TEMPERATURE COMPENSATED ZENER DIODE

- **SINGLE MONOLITHIC ELEMENT**
- **HERMETICALLY SEALED TO-18**
- **MAXIMUM T.C. .005%/°C**

The ZTK33 Series is a new type of reference voltage temperature compensation device which uses proven integrated circuit technology. Devices are hermetically sealed monolithic elements possessing an unusually high degree of stability with maximum temperature coefficients of .005%/°C over the temperature range of −55°C to +100°C. The ZTK33 Series voltage ranges from 30 volts to 36 volts with a ±5% V_Z tolerance around each individual unit's nominal voltage. Special selection can be performed to provide devices with tighter temperature coefficients or voltage tolerances for custom circuit applications. A metal heat sink is available where thermal environment warrants.



ZTK 33 OUTLINE



HEAT SINK

GENERAL DATA:

Case	TO-18 Metal
Mounting Position	Any
Polarity	Cathode To Case, Tab indicates Anode
Operating Temperature	−55°C to +125°C
Storage Temperature	−55°C to +125°C

ELECTRICAL CHARACTERISTICS (T_A = 25°C):

ITT Device Type (1)	Zener Test Current I_{ZT} mA	Zener Voltage V_Z @ I_{ZT}		Maximum Dynamic Impedance (2) Z_{ZT} @ I_{ZT} Ohms	Maximum Zener Current I_{ZM} mA	Maximum $\triangle V_Z$ Over Temperature Range (3)	
		Min. Volts	Max. Volts			V_Z = 30V. Volts	V_Z = 36V. Volts
ZTK33	5	30	36	25	10	.105	.126
ZTK33A	5	30	36	25	10	.232	.279

(1) Device Type: No Suffix; 0°C to +25°C to +70°C
"A" Suffix; −55°C to +25°C to +100°C

(2) Dynamic Impedance: Measured by superimposing a .50mA AC Signal.

(3) Maximum $\triangle V_Z$: All Devices possess a maximum ±.005%/°C Temperature Coefficient over the specified temperature range. Maximum $\triangle V_Z$ limits applicable to total V_Z distribution.

FIG. 1

Typical Transient time lapse from $\triangle V_Z$ after operation a. without heat sink b. with heat sink.

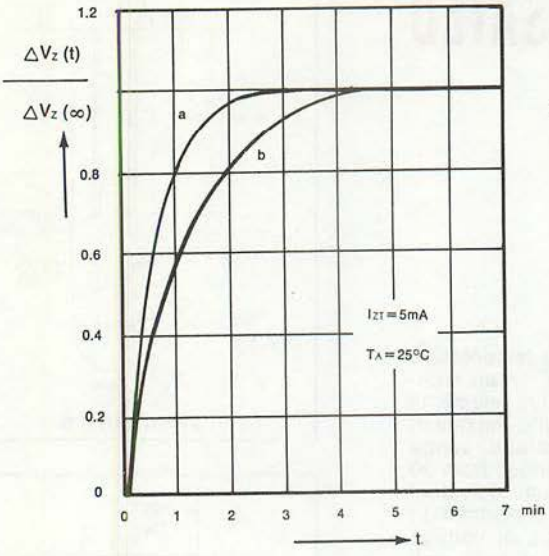


FIG. 2

Typical Change of Dynamic Impedance with Zener Current.

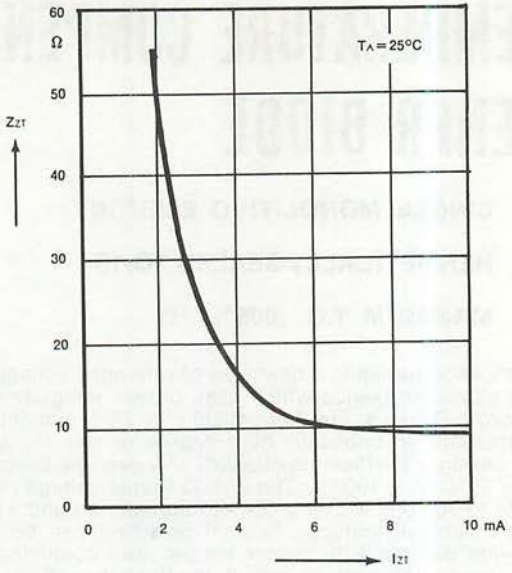
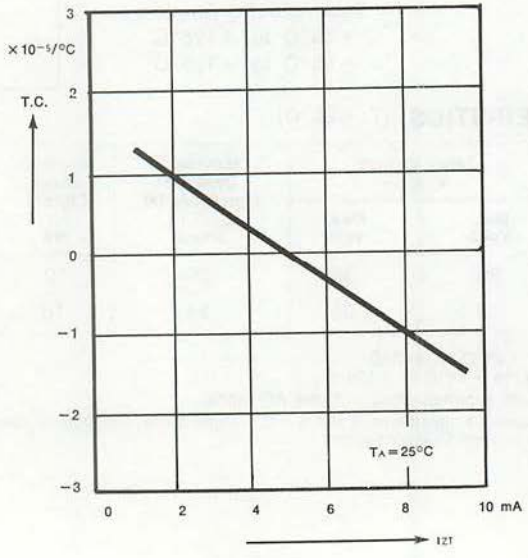


FIG. 3

Typical Change of Temperature Coefficient with Zener Current.

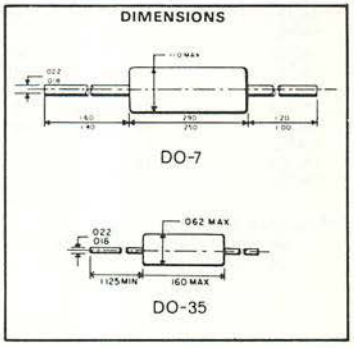


400 mW SILICON ZENER DIODES

- **HERMETICALLY SEALED**
- **INDUSTRY PREFERRED**
- **DO-7 GLASS PACKAGE**

The 400 mW Zener Diodes specified herein are all industry preferred JEDEC types being supplied in the following packages: 1N702 through 1N706 and 1N746 through 1N753 in DO-7 package, 1N707 through 1N726 and 1N754 through 1N759 in DO-35 package, 1N957 through 1N973 in DO-35 package.

Nominal voltages range from 2.7 volts thru 33 volts. Special selection can be performed to provide devices for custom circuit applications. All units are 100% tested and capable of meeting stringent environmental test requirements of MIL-S-19500.



MAXIMUM RATINGS

Junction and Storage Temperatures	−65 to +175°C
D.C. Power Dissipation	400mW
Derating	Per derating curve (3.2mW/°C)

TYPE	Zener Voltage Vz (volts)	Zener Current Iz (MA)	Dynamic Impedance Zz (ohms)	Reverse Current (uA)	Reverse Voltage (volts)	Max. Forward Voltage (volts)	Forward Current (MA)
1N702	2.0/3.2	5	60	—	—	73	1.0
1N703	3.0/3.9	5	55	—	—	10	1.0
1N704	3.7/4.5	5	45	—	—	5	1.0
1N705	4.3/5.4	5	35	—	—	5	1.5
1N706	5.2/6.4	5	20	—	—	5	1.5
1N707	6.2/8.0	5	10	—	—	5	3.5
1N708	5.6	25	2.5	—	—	5	3.5
1N709	6.2	25	4.1	—	—	5	3.5
1N710	6.8	25	4.7	—	—	5	3.5
1N711	7.5	25	5.3	—	—	5	3.5
1N712	8.2	25	6.0	—	—	5	3.5
1N713	9.1	12	7.0	—	—	5	3.5
1N714	10.0	12	8.0	—	—	5	3.0
1N715	11.0	12	9.0	—	—	5	3.0
1N716	12.0	12	10.0	—	—	5	9.0
1N717	13.0	12	11.0	—	—	—	—
1N718	15.0	12	13.0	—	—	—	—
1N719	16.0	12	15.0	—	—	—	—
1N720	18.0	12	17.0	—	—	—	—
1N721	20.0	4	20.0	—	—	—	—
1N722	22.0	4	24.0	—	—	—	—
1N723	24.0	4	28.0	—	—	—	—
1N724	27.0	4	35.0	—	—	—	—
1N725	30.0	4	42.0	—	—	—	—
1N726	33.0	4	50.0	—	—	—	—

MECHANICAL CHARACTERISTICS

CASE: Hermetically sealed glass case.

DIMENSIONS: Per outline drawing.

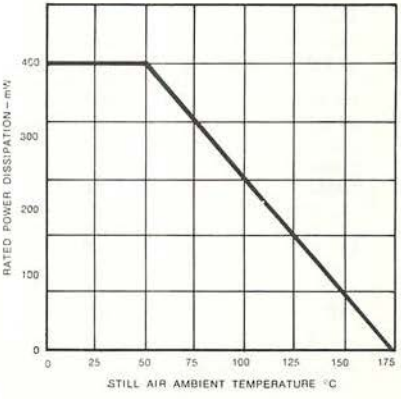
FINISH: All external surfaces are corrosion resistant and leads solderable.

THERMAL RESISTANCE: 250° C/W (Typical) junction to ambient.

POLARITY: Band indicates cathode.

WEIGHT: 2 grams.

MOUNTING POSITION: Any.



1N746 SERIES

ELECTRICAL CHARACTERISTICS ($T_A = 25°C$):

Device Type*	Nominal Zener Voltage V_Z @ I_{ZT} Volts	Test Current I_{ZT} mA	Zener Impedance Max** Z_{ZT} @ I_{ZT} Ohms	Max DC Zener Current I_{ZM} mA	Reverse Leakage Current $T_A = 25°C$ I_R @ $V_R = 1V$ μA	Reverse Leakage Current $T_A = 150°C$ I_R @ $V_R = 1V$ μA
1N746	3.3	20	28	110	10	30
1N747	3.6	20	24	100	10	30
1N748	3.9	20	23	95	10	30
1N749	4.3	20	22	85	2	30
1N750	4.7	20	19	75	2	30
1N751	5.1	20	17	70	1	20
1N752	5.6	20	11	65	1	20
1N753	6.2	20	7	60	0.1	20
1N754	6.8	20	5	55	0.1	20
1N755	7.5	20	6	50	0.1	20
1N756	8.2	20	8	45	0.1	20
1N757	9.1	20	10	40	0.1	20
1N758	10.0	20	17	35	0.1	20
1N759	12.0	20	30	30	0.1	20

*Tolerance Designation:
No Suffix Denotes $V_Z \pm 10\%$;
"A" Suffix, ±5%.

**Zener Impedance: Measured by superimposing an AC Signal equal to 10% of the DC Test Current.

1N957 SERIES ELECTRICAL CHARACTERISTICS ($T_A = 25°C$):

Device Type*	Nominal Zener Voltage V_Z Volts	Test Current I_{ZT} mA	Maximum Zener Impedance** Z_{ZT} @ I_{ZT} Ohms	Maximum Zener Impedance** Z_{ZK} @ I_{ZK} Ohms	Maximum Zener Impedance** I_{ZK} mA	Max. DC Zener Current I_{ZM} mA	Reverse Leakage Current I_R Maximum μA	Reverse Leakage Current Test Voltage*** V_{R1}	Reverse Leakage Current Test Voltage*** V_{R2}
1N957	6.8	18.5	4.5	700	1.0	47	150	5.2	4.9
1N958	7.5	16.5	5.5	700	0.5	42	75	5.7	5.4
1N959	8.2	15	6.5	700	0.5	38	50	6.2	5.9
1N960	9.1	14	7.5	700	0.5	35	25	6.9	6.6
1N961	10	12.5	8.5	700	0.25	32	10	7.6	7.2
1N962	11	11.5	9.5	700	0.25	28	5	8.4	8.0
1N963	12	10.5	11.5	700	0.25	26	5	9.1	8.6
1N964[1]	13	9.5	13	700	0.25	24	5	9.9	9.4
1N965[1]	15	8.5	16	700	0.25	21	5	11.4	10.8
1N966[1]	16	7.8	17	700	0.25	19	5	12.2	11.5
1N967[1]	18	7.0	21	750	0.25	17	5	13.7	13.0
1N968[1]	20	6.2	25	750	0.25	15	5	15.2	14.4
1N969[1]	22	5.6	29	750	0.25	14	5	16.7	15.8
1N970[1]	24	5.2	33	750	0.25	13	5	18.2	17.3
1N971[1]	27	4.6	41	750	0.25	11	5	20.6	19.4
1N972[1]	30	4.2	49	1000	0.25	10	5	22.8	21.6
1N973[1]	33	3.8	58	1000	0.25	9.2	5	25.1	23.8

*Tolerance Designation
No Suffix Denotes $V_Z \pm 20\%$; A Suffix, ±10%; B Suffix, ± 5%.
**Zener Impedance: Measured by superimposing an AC Signal equal to 10% of the DC Test Current.
***Reverse Leakage:
V_{R1} - Test Voltage for 5% Tolerance Device
V_{R2} - Test Voltage for 10% Tolerance Device
No Leakage Specified for 20% Tolerance Device
1. Inquire for availability.

Package DO-41

ONE-WATT (5.1V - 33V) SILICON ZENER DIODES

ABSOLUTE MAXIMUM RATINGS

Characteristics	Unit
DC Power Dissipation	1.0 Watt
Derating Factor	6.67 mW/°C
Junction and Storage Temperature	-65 to +200 °C

One-watt silicon zener diodes designed for constant voltage reference from 5.1 thru 33 volts, with 10% and 5.0% tolerances. These diodes are hermetically sealed for greater reliability.

NOTE 1: The JEDEC type numbers shown have a 5% tolerance on nominal zener voltage. No suffix signifies a 10% tolerance.

NOTE 2: The Zener impedance is derived from the 60 Hz AC voltage, which results when an AC current having an rms value equal to 10% of the DC Zener current (I_{ZT} or I_{ZK}) is superimposed on I_{ZT} or I_{ZK}. Zener impedance is measured at two points to insure a sharp knee on the breakdown curve and eliminate unstable units.

MECHANICAL CHARACTERISTICS

CASE: Hermetically sealed glass case.

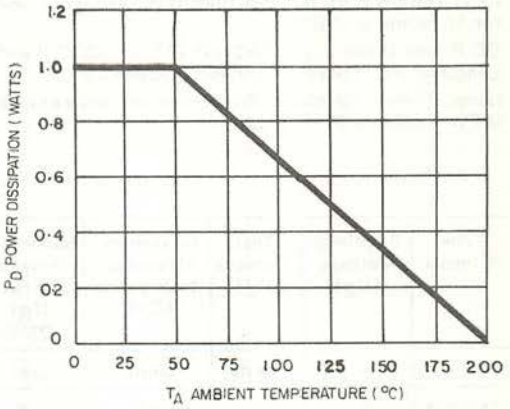
DIMENSIONS: Per outline drawing.

FINISH: All external surfaces are corrosion resistant and leads solderable.

POLARITY: Color Band indicates cathode. When in zener mode cathode is positive.

MOUNTING POSITION: Any.

POWER RATING VS AMBIENT TEMPERATURE



JEDEC TYPE NUMBER	ZENER VOLTAGE (V_Z) NOTE 1	TEST CURRENT (I_{ZT})	MAXIMUM DYNAMIC IMPEDANCE (Z_Z @ I_{ZT}) NOTE 2	MAXIMUM REVERSE CURRENT (I_R @ V_R)	TEST VOLTAGE (V_R)	MAXIMUM REGULATOR CURRENT (I_{ZM})	MAXIMUM KNEE IMPEDANCE (Z_{ZK} @ I_{ZK})	TEST CURRENT (I_{ZK})	MAXIMUM (SURGE) CURRENT (I_S)
	VOLTS	mA	OHMS	mA	VOLTS	mA	OHMS	mA	mA
1N4733A	5.1	49	7	10	1	178	550	1.0	890
1N4734A	5.6	45	5	10	2	162	600	1.0	810
1N4735A	6.2	41	2	10	3	146	700	1.0	730
1N4736A	6.8	37	3.5	10	4	133	700	1.0	660
1N4737A	7.5	34	4.0	10	5	121	700	0.5	605
1N4738A	8.2	31	4.5	10	6	110	700	0.5	550
1N4739A	9.1	28	5.0	10	7	100	700	0.5	500
1N4740A	10	25	7	10	7.6	91	700	0.25	454
1N4741A	11	23	8	5	8.4	83	700	0.25	414
1N4742A	12	21	9	5	9.1	76	700	0.25	380
1N4743A	13	19	10	5	9.9	69	700	0.25	344
1N4744A	15	17	14	5	11.4	61	700	0.25	304
1N4745A	16	15.5	16	5	12.2	57	700	0.25	285
1N4746A	18	14	20	5	13.7	50	750	0.25	250
1N4747A	20	12.5	22	5	15.2	45	750	0.25	225
1N4748A	22	11.5	23	5	16.7	41	750	0.25	205
1N4749A	24	10.5	25	5	18.2	38	750	0.25	190
1N4750A	27	9.5	35	5	20.6	34	750	0.25	170
1N4751A	30	8.5	40	5	22.8	30	1000	0.25	150
1N4752A	33	7.5	45	5	25.1	27	1000	0.25	135

IN5231 thru IN5250
500 mW ZENER DIODES
Package: DO-35

500 millwatt zener diode hermetically sealed in the DO-35 package for greater reliability. Designed for constant reference voltage between 3.3 and 33 volts with 10% and 5% tolerance.

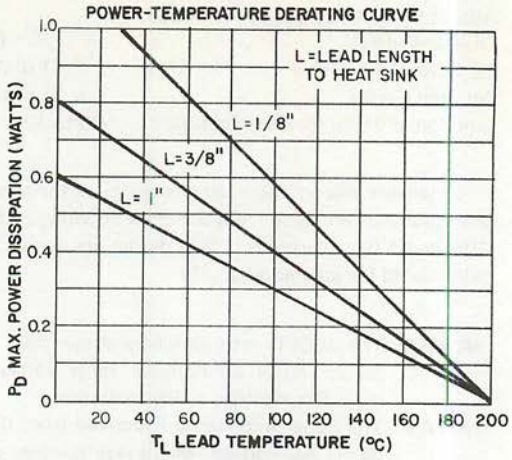
MAXIMUM RATINGS

Junction and Storage Temperature: −65 to +200°C

Lead Temperature not less than 1/16" from the case for 10 seconds: 230°C

DC Power Dissipation: 500 mW @ T_L = 75°C, Lead Length = 3/8" (Derate 4.0 mW/°C above 75°C)

Surge Power: 10 Watts (Non-recurrent square wave @ PW = 8.3 ms, T_J = 55°C)



Type Number	Regulator Voltage (V_Z)	Test Current (I_Z)	Maximum Dynamic Impedance (Z_Z)	Maximum Reverse Current (I_R) 25°C	IR Test Voltage (V_R) (For A Suffix)	IR Test Voltage (V_R) (For B Suffix)	Maximum Regulator Current (I_{ZM})	Maximum Dynamic Knee Impedance (Z_{ZK})	Maximum Temperature Coefficient
	v	ma de	ohms	μa	v	v	ma	ohms	%/°C
1N5231	5.1	20	17	5	1.9	2.0	89	1600	± .030
1N5232	5.6	20	11	5	2.9	3.0	81	1600	+ .038
1N5233	6.0	20	7	5	3.3	3.5	76	1600	+ .038
1N5234	6.2	20	7	5	3.8	4.0	73	1000	+ .045
1N5235	6.8	20	5	3	4.8	5.0	67	750	+ .050
1N5236	7.5	20	6	3	5.7	6.0	61	500	+ .058
1N5237	8.2	20	8	3	6.2	6.5	55	500	+ .062
1N5238	8.7	20	8	3	6.2	6.5	52	600	+ .065
1N5239	9.1	20	10	3	6.7	7.0	50	600	+ .068
1N5240	10	20	17	3	7.6	8.0	45	600	+ .075
1N5241	11	20	22	2	8.0	8.4	41	600	+ .076
1N5242	12	20	30	1	8.7	9.1	38	600	+ .077
1N5243	13	9.5	13	0.5	9.4	9.9	35	600	+ .079
1N5244	14	9.0	15	0.1	9.5	10	32	600	+ .082
1N5245	15	8.5	16	0.1	10.5	11	30	600	+ .082
1N5246	16	7.8	17	0.1	11.4	12	28	600	+ .083
1N5247	17	7.4	19	0.1	12.4	13	27	600	+ .084
1N5248	18	7.0	21	0.1	13.3	14	25	600	+ .085
1N5249	19	6.6	23	0.1	13.3	14	24	600	+ .086
1N5250	20	6.2	25	0.1	14.3	15	23	600	+ .086
1N5251	22	5.6	29	0.1	16.2	17	21	600	+ .087
1N5252	24	5.2	33	0.1	17.1	18	19.1	600	+ .088
1N5253	25	5.0	35	0.1	18.1	19	18.2	600	+ .089
1N5254	27	4.6	41	0.1	20	21	16.8	600	+ .090
1N5255	28	4.5	44	0.1	20	21	16.2	600	+ .091
1N5256	30	4.2	49	0.1	22	23	15.1	600	+ .091
1N5257	33	3.8	58	0.1	24	25	13.8	700	+ .092

SILICON PLANAR DOUBLE PLUG DIODES (DPD's)

ITT Semiconductors' Silicon DPD's (Double Plug Diodes) are Planar Epitaxial Passivated to assure utmost reliability and uniform electrical parameters. They feature carefully controlled forward characteristics over wide current ranges. The pellet is fused to the end plugs, not soldered. Thus, the stability of the anode and cathode contacts is much greater than that of soldered contacts. Sealing is performed in an inert atmosphere eliminating any possibility of sealed-in contamination.

DPD's are smaller than similar DO-7 type diodes. Yet, they have greater inherent reliability due to their fused construction and higher dissipation capabilities. Baked at a minimum of 300°C, DPD's are completely stabilized. Their ruggedness is unsurpassed.

There is a DPD equivalent for all ITT Semiconductors' DO-7 Silicon Planar diodes making it easy to take advantage of these improved characteristics:

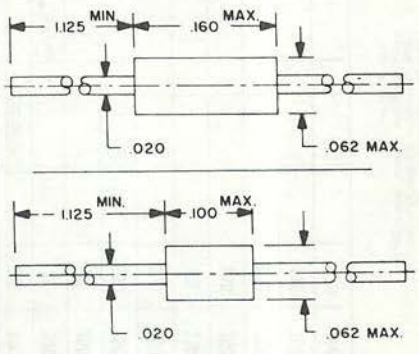
- Low leakage current
- High conductance
- Low capacitance
- Fast switching
- Uniform characteristics
- Improved stability

MECHANICAL DATA

CASE: Hermetically sealed glass
FINISH: All external surfaces corrosion resistant and leads readily solderable
LEADS: Dumet, tin plated
POLARITY: Banded end cathode
WEIGHT: .135 grams (approx.)
MTG. POSITION: Any

DIMENSIONS

STANDARD



AVAILABLE

DPD TYPE #	DO-7 EQUIV. #	BV @ 5 uA V	MAXIMUM V_F @ 25°C												T_{RR} ns	MAXIMUM REVERSE CURRENT			CAP. @ 0.0V PF	T_{FR}	T_{RR} (5) ns	Stored Charge PC	Ave. Rect. Fwd. I @ 25°C mA	Max. Oper. Volt. Cont.	Power Diss. @ 25°C (12) MW
			V @ IF		V @ IF		V@ IF		V @ IF		V @ IF		V @ IF			uA @ 25°C	mA @ 150°C	V_R							
			V	mA	V	mA	V	mA	V	mA	V	mA	V	mA											
1N4148	1N914	75(1)	1.0	10											4(2)	.025	.05	20	4				75		500
1N4149	1N916	75(1)	1.0	10											4(2)	.025	.05	20	2				75		500
1N4150	1N3600		.54/.62	1.0	.66/.74	10	.76/.86	50	.82/.92	100	.87/1.0	200			(3)	0.1	0.1	50	2.5	10ns(4)			150		500
1N4151	1N3604	75	.1.0	50											2(2)	.05	.05	50	2		4		150	50	500
1N4152	1N3605	40	.49/.55	0.1	.53/.59	.25	.59/.67	1.0	.62/.70	2.0	.70/.81	10	.74/.88	20	2(2)	.05	.05	30	2		4		150	30	500
1N4153	1N3606	75	.49/.55	0.1	.53/.59	.25	.59/.67	1.0	.62/.70	2.0	.70/.81	10	.74/.88	20	2(2)	.05	.05	50	2		4		150	50	500
1N4154	1N4009	35	1.0	30											2(2)	0.1	0.1	25	4		4		25	25	500
1N4305	1N4063	75	.505/.575	.25	.55/.65	1.0	.61/.71	2.0	.70/.85	10					2(2)	0.1	0.1	50	2		4		150		500
1N4444		70	.44/.55	0.1	.56/.68	1.0	.69/.82	10	.85/1.0	100						.05	.05	50	2		7		200	50	500
1N4446	1N914A	75(1)	1.0	20											4(2)	.025	.05	20	4				150	75	500
1N4447	1N916A	75(1)	1.0	20											4(2)	.025	.05	20	2				150	75	500
1N4448	1N914B	75(1)	.62/.72	5	1.0	100									4(2)	.025	.05	20	4	2.5V(6)			150	75	500
1N4449	1N916B	75(1)	.63/.73	5	1.0	30									4(2)	.025	.05	20	2	2.5V(6)			150	75	500
1N4450		40(1)	.42/.54	0.1	.52/.64	1.0	.64/.76	10	.80/.92	100	1.0	200			4(2)	.05	.05	30	4				200	30	500
1N4451		40	.40/.50	0.1	.51/.61	1.0	.62/.72	10	.75/.875	100	1.0	300				.05	.05	30	6		10		200	30	500
1N4452		40	.42/.54	0.1	.51/.62	1.0	.60/.71	10	.71/.83	100	1.0	600	.90/1.2	1A	50(7)	.05	.05	30	30				200	30	500
1N4453		30	.43/.55	.01	.51/.63	0.1	.60/.71	1.0	.69/.80	10	.80/92(8)	100				.05	.05	20	30			50/500(9)		20	400
1N4454	1N3064	75	1.0	10											2(2)	0.1	0.1	50	2	3.0V(10)	4			75	500
1N5194	1N483B	80(11)	1.0	100												.025	.005	70						80	250
1N5195	1N485B	200(11)	1.0	100												.025	.005	180						200	250
1N5196	1N486B	250(11)	1.0(13)	100												.025	.005	225						250	250
1N5605	1N457	70(11)	1.0	20												.025	.005	60						70	250
1N5606	1N458	150(11)	1.0	7.0												.025	.005	125						150	200
1N5607	1N459	200(11)	1.0	3.0												.025	.005	175						200	200
1N5608	1N658	120(11)	1.0	100											300(16)	.050	.025	50						120	250
1N5609	1N660	120(11)	1.0	6.0											300(17)	5.0	.050 (15)	100	2.7(14)					120	250

NOTES

(1) BV = 100V @ I_R 100 uA
(2) I_F = 10 mA Recover to 1 mA
V_R = 6V
R_L = 100 Ohms
(3) T_{RR} = 4ns @ I_F = I_R = 10 to 200 mA irr = 0.1 I_F
T_{RR} = 6ns @ I_F = I_R = 200 to 400 mA irr = 0.1 I_F
T_{RR} = 6ns @ I_F = 10 mA, I_R = 1 mA irr = 0.1 mA
(4) I_F = 200 mA tr ≤ 0.4 ns, tp = 100 ns
V_{FR} = 1.0V, DU ≤ 1%
(5) I_F = 10 mA
I_R = 10 mA
Recover to 1 mA
(6) 50 mA peak square wave, 0.1 us pulse width,
5 to 100 KC rep. rate, generator tr ≤ 30 ns
(7) I_F 500 mA
V_R = adjust for I_R = 500 mA Recover to 50 mA
(8) Pulse width = 30 us, duty cycle = 3%,
V_F measured at 25 ± 3us
(9) Ω @ I_F = 1 mA MIL-STD-750 method 4061
(10) I_F = 100 mA peak square wave
0.1 us pulse width
R_L = 50 Ohms tr ≤ 30 ns, 5 to 100 KC
(11) @ 100 uA
(12) Rated Max, Junction Temp. = 200°C
(13) Pulse width = 8.5 msec, duty cycle ≤ 2%.
(14) V_R = 10V, f = 1 MHz
(15) TA = 100 °C
(16) I_F = 5 mA, V_R = 40V
R_I = 2K, Ω = 10 pF
Recover to 80 kΩ
(17) I_F = 30 mA, V_R = 35V
Recover to 400 kΩ

SILICON PLANAR DIODES

HOW TO USE THIS BUYING GUIDE

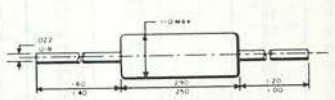
Standard general purpose diodes are listed in numerical order below. Each diode has a line number referenced to the specification tables on pages 2, 3 and 4. Use this buying guide two ways: select the diode by type number, or locate the type number from the specification data.

ITT is the world's leading producer of diodes. Call your ITT sales engineer or distributor for quotation on all your diode needs.

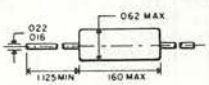
Part No.	Line No.	Part No.	Line No.	Part No.	Line No.	Part No.	Line No.
1N194	45	1N659	68	1N905A	12	1N3654	144
1N194A	44	1N662	126	1N906	10	1N3669	98
1N195	46	1N662A	145	1N906A	13	1N3731	147
1N196	43	1N663	129	1N907	27	1N3872	140
1N251	20	1N663A	146	1N907A	30	1N4009	16
1N379	1	1N690	60	1N908	53	1N4148[1]	108
1N380	2	1N691	130	1N908A	56	1N4149[1]	110
1N381	3	1N692	164	1N914	107	1N4150[1]	71
1N382	6	1N696	54	1N914JAN	142	1N4151[1]	120
1N383	11	1N697	163	1N914A	114	1N4152[1]	41
1N384	14	1N778	155	1N914B	124	1N4153[1]	100
1N385	23	1N789	25	1N916	109	1N4154[1]	37
1N386	40	1N790	24	1N916A	115	1N4305[1]	117
1N387	66	1N791	32	1N916B	118	1N4380	76
1N388	77	1N792	34	1N920	61	1N4444[1]	95
1N389	90	1N793	79	1N921	132	1N4446[1]	113
1N390	103	1N794	78	1N922	165	1N4447[1]	116
1N391	137	1N795	82	1N925	48	1N4448[1]	122
1N392	152	1N796	85	1N926	49	1N4449[1]	123
1N393	168	1N797	157	1N927	91	1N4450[1]	57
1N456	31	1N798	156	1N928	158	1N4451[1]	59
1N456A	36	1N799	159	1N929	15	1N4453[1]	33
1N457	80	1N806	153	1N930	111	1N4454[1]	104
1N457A	84	1N808	154	1N931	167	S298	86
1N460	138	1N810	69	1N934	81	S398	65
1N460A	139	1N811	7	1N993	8	S400	131
1N461	28	1N812	17	1N3062	112	S401	75
1N461A	35	1N813	4	1N3063	102	S402	143
1N462	93	1N814	47	1N3064	105	S403	125
1N462A	96	1N815	5	1N3065	99	S500	133
1N464	169	1N818	128	1N3066	106	S501	87
1N482	38	1N837	149	1N3067	21	S502	62
1N482A	39	1N837A	150	1N3068	22	S504	134
1N482B	58	1N838	170	1N3069	92	S505	88
1N483	94	1N840	70	1N3123	50	S506	63
1N483A	97	1N841	171	1N3124	51	S507	135
1N619	18	1N844	151	1N3206	127	S508	89
1N625	19	1N891	83	1N3298	136	S509	64
1N626	67	1N892	160	1N3600	72	WG140[1]	166
1N627	141	1N903	52	1N3600USN	73	WG141[1]	148
1N643	172	1N903A	55	1N3604	119	WG142[1]	74
1N643A	173	1N904	26	1N3605	42		
1N658	161	1N904A	29	1N3606	101		
1N658A	162	1N905	9	1N3607	121		

Note: 1. Double plug diode package

DIMENSIONS



DO-7 PACKAGE



DOUBLE PLUG DIODE PACKAGE

MECHANICAL DATA

Case:
Hermetically sealed glass

Finish:
All external surfaces corrosion resistant and leads readily solderable

Leads:
Dumet, tin plated

Weight:
0.135 grams (approx.)

Mounting Position:
Any

Marking:
Diodes carry ITT identification, and are EIA Color Coded. Bands 1, 2, 3 and 4 on the illustration above indicate the first, second, third and fourth digit respectively of the type designation, starting from the cathode end of the diode.

Black.....0	Green.....5
Brown.....1	Blue.....6
Red.....2	Violet.....7
Orange.....3	Gray.....8
Yellow.....4	White.....9

ELECTRICAL CHARACTERISTICS @ 25°C unless otherwise noted

V_{RM}	I_F		I_R		High Temp I_R			Reverse Recovery Time t_{rr}					Cap. C		Part No.	Line No.
	mA @	V_F	μA @	V_R	μA	V_R	°C	I_FmA	V_R	Rec. to	nsec	Test Condition	pf @	V_R		
9	35	1	0.5	8.2	5	8.2	100						35	6	1N379	1
11	30	1	0.5	10	5	10	100						30	6	1N380	2
13.5	23	1	0.5	12	5	12	100						28	64	1N381	3
15	5	1	0.5	5	10	5	125	5	−10	0.5mA	250	JAN 256			1N813	4
15	100	1.5	0.5	5	10	5	125	5	−10	0.5mA	250	JAN 256			1N815	5
17	17	1	0.5	15	5	15	100						25	6	1N382	6
20	1	1	1	10	10	10	125	5	−10	0.5mA	250	JAN 256	2	0	1N811	7
20	10	1.2	1	6				10	−6	3mA	4	R_L=75Ω			1N993	8
20	10	1	0.1	20	10	20	100	10	−5		4	R_L=100Ω	1	6	1N905	9
20	10	1	0.1	20	10	20	100	10	−5		4	R_L=100Ω	2.5	6	1N906	10
20	12	1	0.1	18	10	18	100						20	6	1N383	11
20	20	1	0.1	20	10	20	100	10	−5	1mA	4	R_L=100Ω	1	6	1N905A	12
20	20	1	0.1	20	10	20	100	10	−5	1mA	4	R_L=100Ω	2.5	6	1N906A	13
25	9	1	0.1	22	10	22	100						15	6	1N384	14
25	20	1	0.1	20											1N929	15
25	30	1	0.1	25	100	25	150	10	−6		2	R_L=100Ω	4	0	1N4009	16
30	2	1	1	10	10	10	125	5	−10	0.5mA	250	JAN 256	2	0	1N812	17
30	3	1	.08	10	16	10	100								1N619	18
30	4	1.5	1	20	30	20	100	30	−35	400kΩ	1000	IBM Y Mod			1N625	19
30	5	1	0.1	10	10	10	100	5	−10	0.5mA	150		1	0	1N251	20
30	5	1	0.1	20	100	20	150	10	−6	1mA	2	R_L=100Ω	4	0	1N3067	21
30	5	1	0.1	20	100	20	150	30	30mA[2]	1mA	50	R_L=100Ω	6	0	1N3068	22
30	7	1	0.1	27	10	27	100						12	6	1N385	23
30	10	1	5	20	30	20	100	5	−20	200kΩ	250				1N790	24
30	10	1	1	20	30	20	100	5	−20	200kΩ	500				1N789	25
30	10	1	0.1	30	10	30	100	10	−5		4	R_L=100Ω	1	6	1N904	26
30	10	1	0.1	30	10	30	100	10	−5		4	R_L=100Ω	2.5	6	1N907	27
30	15	1	0.5	25	30	25	150						10	0	1N461	28
30	20	1	0.1	30	10	30	100	10	−5	1mA	4	R_L=100Ω	1	6	1N904A	29
30	20	1	0.1	30	10	30	100	10	−5	1mA	4	R_L=100Ω	2.5	6	1N907A	30
30	40	1	0.025	25	5	25	150								1N456	31
30	50	1	5	20	30	20	100	5	−20	200KΩ	500				1N791	32
30	0.01	.43/.55	0.05	20	50	20	150						30	0	1N4453[1]	33
	0.1	.51/.63														
	1	.60/.71														
	10	.69/.80														
	100	.80/.92														
30	100	1	5	20	30	20	100	5	−20	100kΩ	500				1N792	34
30	100	1	0.5	25	30	25	150								1N461A	35
30	100	1	0.025	25	5	25	150						5	0	1N456A	36
35	30	1	0.1	25	100	25	150	10	−6	1mA	2	R_L=100Ω			1N4154[1]	37
36	100	1.1	0.25	30	30	30	150								1N482	38
36	100	1	0.025	30	15	30	150								1N482A	39
37	5.5	1	0.1	33	10	33	100						10	6	1N386	40
40	0.1	.49/.55	0.05	30	50	30	150	10	−6	1mA	2	R_L=100Ω	2	0	1N4152[1]	41
	0.25	.53/.59														
	1	.59/.67														
	2	.62/.70														
	10	.70/.81														
	20	.74/.88														
40	0.1	0.55	0.05	30	50	30	150	10	−6	1mA	2	R_L=100Ω	2	0	1N3605	42
40	1	2	10	40	300	50	150	30	−35		100				1N196	43
40	1	1	10	40	300	40	150	30	−35		200				1N194A	44
40	1.5	2	10	40	300	40	150	30	−35		200				1N194	45
40	2	2	10	40	300	40	150	30	−35		300				1N195	46
40	2	1	0.1	20	10	20	125	5	−10	0.5mA	250	JAN 256			1N814	47
40	5	1	1	10	20	10	100	5	−10	20kΩ	150	JAN 256			1N925	48
40	5	1	0.1	10	10	10	100	5	−10	20kΩ	150	JAN 256			1N926	49
40	10	1.5	0.1	40	10	40	100	10	−5	1mA	4	R_L=100Ω	0.8	6	1N3123	50
40	10	1.5	0.1	40	10	40	100	10	−5	1mA	4	R_L=100Ω	2	6	1N3124	51
40	10	1	0.1	40	10	40	100	10	−5		4	R_L=100Ω	1	6	1N903	52
40	10	1	0.1	40	10	40	100	10	−5		4	R_L=100Ω	2.5	6	1N908	53
40	10	1	0.015	20	20	20	150	10		10mA	5		4	0	1N696	54
40	20	1	0.1	40	10	40	100	10	−5	1mA	4	R_L=100Ω	1	6	1N903A	55
40	20	1	0.1	40	10	40	100	10	−5	1mA	4	R_L=100Ω	2.5	6	1N908A	56
40	0.1	.42/.54	0.05	30	50	30	150	10	−6	1mA	4	R_L=100Ω	4	0	1N4450[1]	57
	1	.52/.64														
	10	.64/.76														
	100	.80/.92														
	200	1														

Notes: 1. Double plug diode package 2. I_RmA

ELECTRICAL CHARACTERISTICS, continued

V_{RM}	I_F		I_R		High Temp I_R			Reverse Recovery Time trr					Cap. C		Part No.	Line No.
	mA	@ V_F	μA	@ V_R	μA	V_R	°C	I_FmA	V_R	Rec. to	nsec	Test Condition	pf	@ V_R		
40	100	1	0.025	30	5	30	150								1N482B	58
40	0.1	.40/.50	0.05	30	50	30	150						6	0	1N4451[1]	59
	1	.51/.61														
	10	.62/.72														
	100	.75/.88														
	300	1														
40	400	1	0.25	30	50	30	150	500	−30	10kΩ	800	R_L=1kΩ			1N690	60
40	500	1	0.25	30	50	30	150	500	−30	10kΩ	300	R_L=1kΩ	9	7.5	1N920	61
40	500	1	0.05	25				500	−30	10kΩ	15	R_L=100Ω	7	9	S502	62
40	500	1	0.05	25				500	−30	10kΩ	30	R_L=100Ω	7	9	S506	63
40	500	1	0.05	25				500	−30	10kΩ	50	R_L=100Ω	7	9	S509	64
40	500	0.9	0.2	25				500	−30	10kΩ	200	R_L=1kΩ	7	9	S398	65
43	4.5	1	0.1	39	10	39	100						8	6	1N387	66
50	4	1.5	1	35	30	35	100	30	−35	400kΩ	1000	IBM Y Mod			1N626	67
50	6	1	5	50	25	50	100	30	−35	400kΩ	300	JAN 256	2.7	10	1N659	68
50	10	1	1	40				10			50				1N810	69
50	150	1	0.1	40	15	40	100	30	−35	400kΩ	300	JAN 256			1N840	70
50	1	.54/.62	0.1	50	100	50	150	20 to	20 to		4	irr=0.1 I_F	2.5	0	1N4150[1]	71
	10	.66/.74						200	200[2]							
	50	.76/.86						200 to	200 to		6	irr=0.1 I_F				
	100	.86/.92						400	400[2]							
	200	.87/1.0						10	1[2]		6	irr=0.1 mA				
50	200	1	0.1	50	100	50	150	10		0.1mA	6		2.5	0	1N3600	72
50	200	1	0.1	50	100	50	150	10		1.1mA	4	R_L=100Ω	2.5	0	1N3600	73
															USN	
50	250	1	0.1	30				10	−6	1mA	6	R_L=100Ω	4	0	WG142[1]	74
50	400	1	0.1	30				400	−30	10kΩ	15	R_L=100Ω	7	9	S401	75
50	570	1.4	50	50				570	−15	1mA	1.8	R_L=100Ω	3	15	1N4380	76
52	3.5	1	0.1	47	10	47	100						6	6	1N388	77
60	10	1	5	50	30	50	100	5	−40	200kΩ	250				1N794	78
60	10	1	1	50	30	50	100	5	−20	200kΩ	500				1N793	79
60	20	1	0.025	60	5	60	150						8	0	1N457	80
60	30	1	0.025	60	6	60	150	30	−35	400kΩ	1000				1N934	81
60	50	1	5	50	3	50	100	5	−40	200kΩ	500				1N795	82
60	50	1	0.1	50	25	50	100			80kΩ	300	JAN 256			1N891	83
60	100	1	0.025	60	5	60	150								1N457A	84
60	100	1	5	50	30	50	100	5	−40	100kΩ	500				1N796	85
60	500	1	0.2	30				500	−50	10kΩ	200	R_L=1kΩ	7	9	S298	86
60	500	1	0.1	30				500	−30	10kΩ	15	R_L=100Ω	7	9	S501	87
60	500	1	0.1	30				500	−30	10kΩ	30	R_L=100Ω	7	9	S505	88
60	500	1	0.1	30				500	−30	10kΩ	50	R_L=100Ω	7	9	S508	89
62	2.7	1	1	56	50	50	100						5.6	6	1N389	90
65	10	1	0.1	10	10	10	100	5	−10	20kΩ	150	JAN 256			1N927	91
65	50	1	0.1	50	100	50	100	30	30mA[2]	1mA	50	R_L=100Ω	6	0	1N3069	92
70	5	1	0.5	60	30	60	150						8	0	1N462	93
70	100	1.1	0.25	60	30	60	150								1N483	94
70	0.1	.44/.55	0.05	50	50	50	150	10	−6	1mA	2	R_L=100Ω	2	0	1N4444[1]	95
	1	.56/.68														
	10	.69/.82														
	100	.85/1.0														
70	100	1	0.5	60	30	60	150								1N462A	96
70	100	1	0.025	60	15	60	150								1N483A	97
70	400	1.1	0.25	70				300	−10	1mA	200	R_L=100Ω	10	10	1N3669	98
75	0.1	0.53	0.1	50	100	50	150	10	−6	1mA	2	R_L=100Ω	1.5	0	1N3065	99
75	0.1	.49/.55	0.05	30	50	30	150	10	−6	1mA	2	R_L=100Ω	2	0	1N4153[1]	100
	0.25	.53/.59														
	1	.59/.67														
	1	.62/.70														
	10	.70/.81														
	20	.74/.88														
75	0.1	0.55	0.05	50	50	50	150	10	−6	1mA	2	R_L=100Ω	2	0	1N3606	101
75	0.25	0.58	0.1	50	100	50	150	10	−1	1mA	4	R_L=100Ω	2	0	1N3063	102
75	2	1	1	68	50	68	100						5.2	6	1N390	103
75	10	1						10	−6	1mA	2	R_L=100Ω	2	0	1N4454[1]	104
75	10	1	0.1	50	100	50	150	10	−1	1mA	4	R_L=100Ω	2	0	1N3064	105
75	10	1	0.1	50	100	50	150	10	−6	1mA	2	R_L=100Ω	1	0	1N3066	106
75	10	1	0.025	20	50	20	150	10	−6	1mA	4	R_L=100Ω	4	0	1N914	107
75	10	1	0.025	20	50	20	150						4	0	1N4148[1]	108
75	10	1	0.025	20	50	20	150	10	−6	1mA	4	R_L=100Ω	2	0	1N916	109
75	10	1	0.025	20	50	20	150						2	0	1N4149[1]	110

Notes: 1. Double plug diode package 2. I_RmA

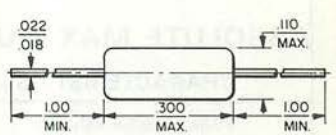
ELECTRICAL CHARACTERISTICS, continued

V_{RM}	I_F		I_R		High Temp I_R			Reverse Recovery Time trr					Cap. C		Part No.	Line No.
	mA	@ V_F	μA	@ V_R	μA	V_R	°C	I_FmA	V_R	Rec. to	nsec	Test Condition	pf	@ V_R		
75	20	1	0.1	50											1N930	111
75	20	1	0.1	50	100	50	150	10	−6	1mA	2	R_L=100Ω	1	0	1N3062	112
75	20	1	0.025	20	50	20	150	10	−6	1mA	4	R_L=100Ω	4	0	1N4446[1]	113
75	20	1	0.025	20	50	20	150	10	−8	1mA	4	R_L=100Ω	4	0	1N914A	114
75	20	1	0.025	20	50	20	150	10	−6	1mA	4	R_L=100Ω	2	0	1N916A	115
75	20	1	0.025	20	50	20	150	10	−6	1mA	4	R_L=100Ω	2	0	1N4447[1]	116
75	0.25	.50/.58						10	−6	1mA	2	R_L=100Ω	2	0	1N4305[1]	117
	1	.55/.65														
	2	.61/.71														
	10	.70/.81														
75	30	1	0.025	20	50	20	150	10	−6	1mA	4	R_L=100Ω	2	0	1N916B	118
75	50	1	0.05	50	50	50	150	10	−6	1mA	2	R_L=100Ω	2	0	1N3604	119
75	50	1	0.05	50	50	50	150	10	−6	1mA	2	R_L=100Ω	2	0	1N4151[1]	120
75	50	1	0.05	50	50	50	150	10	−6	1mA	2	R_L=100Ω	2	0	1N3607	121
75	5	.62/.72	0.025	20	50	20	150	10	−6	1mA	4	R_L=100Ω	4	0	1N4448[1]	122
	100	1.0														
75	5	.63/.73	0.025	20	50	20	150	10	−6	1mA	4	R_L=100Ω	2	0	1N4449[1]	123
	30	1.0														
75	100	1	0.025	20	50	20	150	10	−6	1mA	4	R_L=100Ω	4	0	1N914B	124
75	200	1	0.1	50	100	50	150	200	200mA[2]	0.1mA	6	R_L=100Ω	2.5	0	S403	125
80	10	1	1	10	100	50	100	5	−40	100kΩ	500		3	10	1N662	126
80	10	1	0.025	20	50	20	150	10	−6	1mA	4	R_L=100Ω	4	0	1N3206	127
80	30	1.5	0.25	60	20	60	100	20	−40		500	JAN 256			1N818	128
80	100	1	5	75	50	75	100	5	−40	200kΩ	500				1N663	129
80	400	1	0.25	60	50	60	150	500	−50	10kΩ	800	R_L=1kΩ			1N691	130
80	400	1	0.1	50				400	−30	10kΩ	15	R_L=100Ω	7	9	S400	131
80	500	1	0.25	60	50	60	150	500	−50	10kΩ	300	R_L=1kΩ			1N921	132
80	500	1	0.1	50				500	−30	10kΩ	15	R_L=100Ω	7	9	S500	133
80	500	1	0.1	50				500	−30	10kΩ	30	R_L=100Ω	7	9	S504	134
80	500	1	0.1	50				500	−30	10kΩ	50	R_L=100Ω	7	9	S507	135
80	500	0.9	0.2	60	45	60	150	500	−30	50mA	50	R_L=50Ω			1N3298	136
90	1.5	1	1	82	50	82	100						4.8	6	1N391	137
90	5	1	0.01	10	0.2	10	100						3	10	1N460	138
90	15	1	0.01	10	0.2	10	100						4	10	1N460A	139
90	150	1	0.1	75				200	−20	5mA	50	R_L=100Ω	5	0	1N3872	140
100	4	1.5	1	75	30	75	100	30	−35	400kΩ	1000	IBM Y Mod			1N627	141
100	10	1	5	75	50	20	150	10			5	R_L=100Ω	2.8	1.5	1N914JAN	142
100	25	1	10	80	0.5	20	71	30	−35	400kΩ	100	R_L=2kΩ			S402	143
100	50	1	0.025	75	25	75	150	5	−6.5	1mA	4				1N3654	144
100	100	1	1	10	100	50	100	5	−40	100kΩ	300	JAN 256			1N662A	145
100	100	1	0.1	75	15	75	100	5	−40	200kΩ	300	JAN 256			1N663A	146
100	100	1	0.050	50	50	50	150	10	−6	1mA	3	R_L=100Ω	2	0	1N3731	147
100	100	1	0.050	50				10	−6	1mA	3	R_L=100Ω	2	0	WG141[1]	148
100	150	1	0.1	75	15	75	100	30	−35	400kΩ	500	JAN 256			1N837	149
100	150	1	0.1	80	15	80	100	30	−35	400kΩ	300	JAN 256			1N837A	150
100	200	1	0.1	80	15	80	100	30	−35	400kΩ	500	JAN 256			1N844	151
110	1.2	1	1	100	50	100	100						4.5	6	1N392	152
110	4	1	0.5	100	50	100	125	5	−40		300	JAN 256			1N806	153
110	100	1	1	100	50	100	125	30	−35		300	JAN 256 R_L=500Ω			1N808	154
112	10	1	0.5	100	30	100	125	5	−40	400kΩ	300	JAN 256			1N778	155
120	10	1	5	100	30	100	100	5	−40	200kΩ	250				1N798	156
120	10	1	1	100	30	100	100	5	−40	200kΩ	500				1N797	157
120	10	1	0.1	10	10	10	100	5	−10	20kΩ	150				1N928	158
120	50	1	5	100	30	100	100	5	−40	200kΩ	500				1N799	159
120	50	1	0.1	100	25	100	100			80kΩ	300	JAN 256			1N892	160
120	100	1	0.05	50	25	50	150	5	−40	80kΩ	300				1N658	161
120	100	1	0.025	50	10	50	150	5	−40	80kΩ	300	JAN 256			1N658A	162
120	250	1	1	50				100	−10	10mA	5		25	0	1N697	163
120	400	1	0.25	90	50	90	150	500	−50	10kΩ	800	R_L=1kΩ			1N692	164
120	500	1	0.25	90	100	90	150	500	−50	10kΩ	300	R_L=1kΩ			1N922	165
125	150	1						10	−6	1mA	4	R_L=100Ω			WG140[1]	166
125	20	1	0.1	100											1N931	167
135	0.9	1	1	120	50	120	100						4.2	6	1N393	168
150	3	1	0.5	125	30	120	150								1N464	169
150	150	1	0.1	125	15	125	100	30	−35	400kΩ	500	JAN 256			1N838	170
150	150	1	0.1	120	15	120	100	30	−35	400kΩ	300	JAN 256			1N841	171
175	10	1	0.025	10	15	100	100	5	−40	200kΩ	300				1N643	172
175	40	1	1.0	100	15	100	100						3	−10	1N643A	173

Notes: 2. I_RmA 1. Double plug diode package

SILICON EPITAXIAL PLANAR SWITCHING DIODE

DIMENSIONS



DO-7

ABSOLUTE MAXIMUM RATINGS

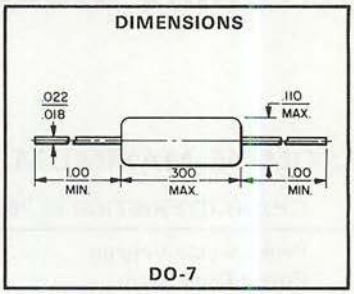
CHARACTERISTICS @ 25°C		UNITS
Peak Inverse Voltage	100	Volts
Power Dissipation	250	mW
Storage Temperature	−65 to +200	°C
Avg. Rect. Fwd. Current	75	mA
Surge Current, 1 sec.	500	mA

ELECTRICAL CHARACTERISTICS @ 25°C unless otherwise noted.

SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITIONS
PIV	100			Vdc	$I_R = 100\mu A$
I_R			5.0 .025 50	μA μA μA	$V_R = 75V$ $V_R = 20V$ $V_R = 20V$, T = 150°C
V_F			1.0	Vdc	$I_F = 10$ mA
T_{rr}			4.0	nsec	$I_F = 10$ mA, $V_R = 6V$
C			4.0	pF	$V_R = 0V$
T_{fr}			2.5	Vdc	50 mA Peak Square Wave, 0.1 μsec Pulse Width, 5 KC Rep. Rate, Max. Volt. Drop

SILICON EPITAXIAL PLANAR SWITCHING DIODE

The ITT JAN 1N914 diode meets MIL-S-19500/116B.



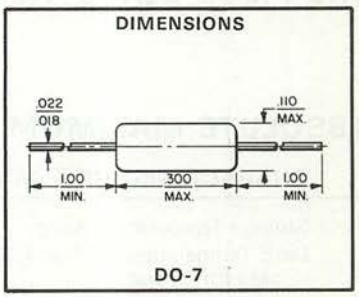
ABSOLUTE MAXIMUM RATINGS

CHARACTERISTICS @ 25°C		UNITS
Peak Inverse Voltage	100	Volts
Power Dissipation	250	mW
Storage Temperature	−65 to +200	°C
Avg. Rectified Fwd. Current	75	mA
Surge Current, 1 second	500	mA

ELECTRICAL CHARACTERISTICS @ 25°C unless otherwise noted.

SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITIONS
PIV	100			Vdc	$I_R = 100\mu A$
I_R			25 5.0 50 100	nA μA μA μA	$V_R = 20V$ $V_R = 75V$ $V_R = 20V$, T = 150°C $V_R = 75V$, T = 150°C
V_F			1.0	Vdc	$I_F = 10mA$
C			4.0 2.8	pF pF	$V_R = 0V$ $V_R = 1.5V$
T_{rr}			5.0	nsec	$I_F = I_R = 10mA$, C = 3pF, $R_L = 100\Omega$, Rec. to 1.0mA
T_{fr}			5.0	Vdc	50mA/20 nsec, Rep. Rate Less than 100 KC

SILICON EPITAXIAL PLANAR SWITCHING DIODE



ABSOLUTE MAXIMUM RATINGS

CHARACTERISTICS @ 25°C		UNITS
Peak Inverse Voltage	100	Volts
Power Dissipation	250	mW
Storage Temperature	−65 to +200	°C
Avg. Rect. Fwd. Current	75	mA
Surge Current, 1 sec.	500	mA

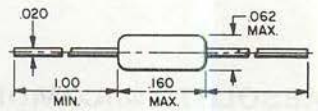
ELECTRICAL CHARACTERISTICS @ 25°C unless otherwise noted.

SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITIONS
PIV	100			Vdc	I_R=100 μA
I_R			5.0 .025 50	μA μA μA	V_R=75V V_R=20V V_R=20V, T=150°C
V_F			1.0	Vdc	I_F=10 mA
T_{rr}			4.0	nsec	I_F=10 mA, V_R=6V
C			2.0	pF	V_R=0V
T_{fr}			2.5	Vdc	50 mA Peak Square Wave, 0.1μsec Pulse Width, 5KC Rep. Rate, Max. Volt. Drop.

SILICON EPITAXIAL PLANAR DIODE

ONE PIECE GLASS—HERMETICALLY SEALED

DIMENSIONS



DOUBLE PLUG DIODE

ABSOLUTE MAXIMUM RATINGS

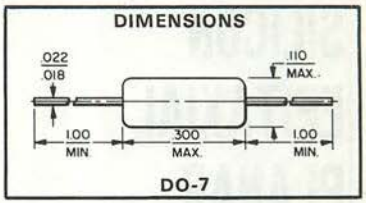
CHARACTERISTICS @ 25°C:		UNITS
Storage Temperature Range	—65 to 200	°C
Lead Temperature 1/16 ± 1/32" from case for 10 sec	300	°C
Continuous Reverse Operating Voltage	75	Volts
Power Dissipation	500	mW
Derating Factor	2.85	MW/°C

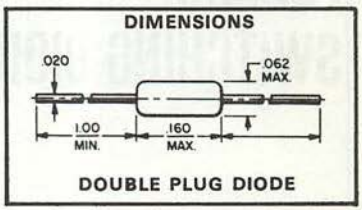
ELECTRICAL CHARACTERISTICS @25°C unless otherwise noted

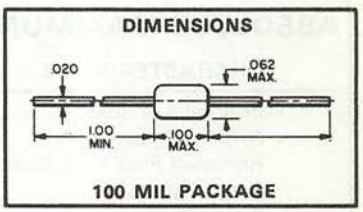
CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	CONDITION
Peak Inverse Voltage	75			V	5μa
Peak Inverse Voltage	100			V	100μa
Forward Voltage			1.0	V	10mA
Reverse Current			25	na	20V
Reverse Current		150	50	μa	20V
Capacitance			4	pf	0V
Reverse Recovery Time		Note 1	4	nsec	1mA

Note 1. If=10 mA Vr=6 V R_l=100 ohms recover to 1. mA

SILICON EPITAXIAL PLANAR SWITCHING DIODE







ABSOLUTE MAXIMUM RATINGS

CHARACTERISTICS @ 25°C		UNITS
Peak Inverse Voltage	75	Volts
Avg. Rect. Current	200	mA
Recurrent Peak Fwd. Current	900	mA
Surge Current, 1 sec.	1	Amp
Power Dissipation	500	mW
Operating Temperature	−65 to +150	°C
Storage Temperature	−65 to +175	°C

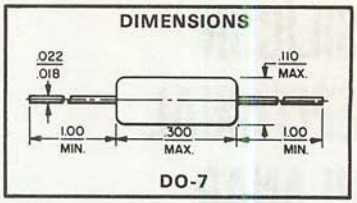
ELECTRICAL CHARACTERISTICS @ 25°C unless otherwise noted.

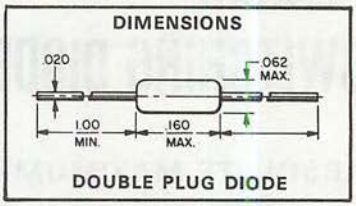
SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITIONS
V_F	.87		1.0	Vdc	I_F=200 mA
	.82		.92	Vdc	I_F=100 mA
	.76		.86	Vdc	I_F=50 mA
	.66		.74	Vdc	I_F=10 mA
	.54		.62	Vdc	I_F=1 mA
I_R			100	nA	V_R=50V
			100	μA	V_R=50V, T=150°C
PIV	75			Vdc	I_R=5μA
C			2.5	pF	V_R=0V
T_{rr}			4.0	nsec	I_F=I_R=10 to 200 mA Rec. to 0.1 of I_F
			6.0	nsec	I_F=I_R=200 to 400 mA Rec. to 0.1 of I_F

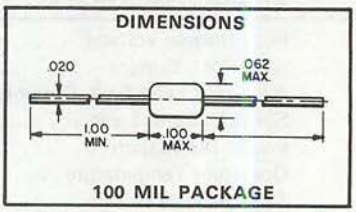
ITT601 ITT601 DPD ITT601 MP

SILICON SWITCHING DIODE

SILICON EPITAXIAL PLANAR SWITCHING DIODE







ABSOLUTE MAXIMUM RATINGS

CHARACTERISTICS @ 25°C		UNITS
Peak Inverse Voltage	50	Volts
Avg. Rect. Current	200	mA
Recurrent Peak Fwd. Current	900	mA
Surge Current, 1 sec.	1	Amp
Power Dissipation	500	mW
Operating Temperature	−65 to +150	°C
Storage Temperature	−65 to +175	°C

ELECTRICAL CHARACTERISTICS @ 25°C unless otherwise noted

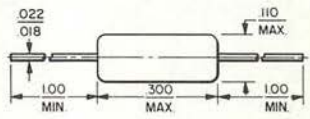
SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITIONS
V_F			1.2	Vdc	I_F=500mA
			1.0	Vdc	I_F=400mA
	.80		.90	Vdc	I_F=200mA
	.75		.85	Vdc	I_F=100mA
	.62		.70	Vdc	I_F=10 mA
I_R			100	nA	V_R=30V
			100	μA	V_R=30V, T=150°C
PIV	50			Vdc	I_R=5μA
C			3.0	pF	V_R=0V
T_{rr}			6.0	nsec	I_F=I_R=10 mA, R_L=100Ω Rec. to 1.0 mA

SILICON EPITAXIAL PLANAR SWITCHING DIODE

ABSOLUTE MAXIMUM RATINGS

CHARACTERISTICS @ 25°C		UNITS
Peak Inverse Voltage	30	Volts
Avg. Rect. Current	50	mA
Recurrent Peak Fwd. Current	150	mA
Surge Current, 1 sec.	150	mA
Power Dissipation	250	mW
Power Derating Factor	2	mW/°C
Operating Temperature	−65 to +150	°C
Storage Temperature	−65 to +175	°C

DIMENSIONS



DO-7

ELECTRICAL CHARACTERISTICS @ 25°C unless otherwise noted.

SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITIONS
PIV	30			Vdc	$I_R = 5\mu A$
V_F	.89		1.1	Vdc	$I_F = 50$ mA
	.81		.95	Vdc	$I_F = 20$ mA
	.76		.88	Vdc	$I_F = 10$ mA
	.64		.74	Vdc	$I_F = 1$ mA
	.52		.61	Vdc	$I_F = 100\mu A$
	.42		.50	Vdc	$I_F = 10\mu A$
I_R			50	nA	$V_R = 15V$
			50	μA	$V_R = 15V$, T = 150°C
C			.75	pF	$V_R = 0V$
T_{rr}			700	psec	$I_F = I_R = 10$ mA, 100Ω Pulse Gen., .25 nsec Detector .1 nsec; Rec. to 1.0 mA

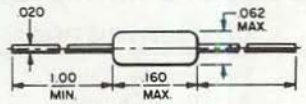
ITT2001 ITT2002 ITT2003

SILICON SWITCHING DIODE

SILICON EPITAXIAL PLANAR SWITCHING DIODE

For General Purpose High-Voltage Applications

DIMENSIONS



DOUBLE PLUG DIODE

MAXIMUM RATINGS @ 25°C (NOTE 1)

	ITT 2001	ITT 2002	ITT 2003
Peak Inverse Voltage	100 Volts	200 Volts	250 Volts
Average Rectified Current	150 ma	150 ma	150 ma
Forward Current Steady State D.C.	250 ma	250 ma	250 ma
Recurrent Peak Forward Current	400 ma	400 ma	400 ma
Peak Forward Surge Current Pulse Width of 1.0 Second	1.0 A	1.0 A	1.0 A
Power Dissipation	300 mw	300 mw	300 mw
Power Derating	3.3 mw/°C	3.3 mw/°C	3.3 mw/°C
Operating Temperature	−65°C to +175°C	−65°C to +175°C	−65°C to +175°C
Storage Temperature, Ambient	−65°C to +200°C	−65°C to +200°C	−65°C to +200°C

ITT2001 — ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
VF	Forward Voltage		1.0	Volts	IF = 100 ma
IR_1	Reverse Current		0.1	ua	VR = 50 V
IR_2	Reverse Current (150°C)		100	ua	VR = 50 V
BV	Breakdown Voltage	100		Volts	IR = 100 ua
Qs	Store Charge (Note 2)		500	pc	IF = 10 ma
Co	Capacitance		5.0	pf	VR = 0 V, f = 1 MHz

NOTES: 1. The maximum ratings are limiting values above which life or satisfactory performance may be impaired.
2. This test is equivalent to Trr @ IF = IR = 30 ma, RL — 100 ohms, recovered to 3 ma to be less than 50 nsec.

ITT2002 — ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
VF	Forward Voltage		1.0	Volts	IF = 100 ma
IR_1	Reverse Current		0.1	ua	VR = 150 V
IR_2	Reverse Current (150°C)		100	ua	VR = 150 V
BV	Breakdown Voltage	200		Volts	IR = 100 ua
Qs	Storage Charge (Note 2)		500	pc	IF = 10 ma
Co	Capacitance		5.0	pf	VR = 0 V, f = 1 MHz

ITT2003 — ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

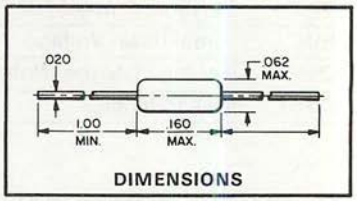
SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
VF	Forward Voltage		1.0	Volts	IF = 100 ma
IR_1	Reverse Current		0.1	ua	VR = 150 V
IR_2	Reverse Current (150°C)		100	ua	VR = 150 V
BV	Breakdown Voltage	250		Volts	IR = 100 ua
Qs	Store Charge (Note 2)		500	pc	IF = 10 ma
Co	Capacitance		5.0	pf	VR = 0 V, f = 1 MHz

ITT3001 ITT3002 ITT3003®

SILICON PLANAR DIODE

HIGH VOLTAGE HIGH TEMPERATURE DOUBLE PLUG DIODE

For General Purpose, High-Temperature, High-Voltage Applications



DIMENSIONS

MAXIMUM RATINGS (25°C) NOTE 1

	3001	3002	3003
Peak Inverse Voltage	70 Volts	150 Volts	200 Volts
Average Rectified Current	100 ma	100 ma	100 ma
Forward Current Steady State D.C.	200 ma	200 ma	200 ma
Recurrent Peak Forward Current	300 ma	300 ma	300 ma
Peak Forward Surge Current Pulse Width of 1.0 Second	1.0 A	1.0 A	1.0 A
Power Dissipation	250 mw	250 mw	250 mw
Power Derating	2.0 mw/°C	2.0 mw/°C	2.0 mw/°C
Operating Temperature	−65°C to +175°C	−65°C to +175°C	−65°C to +175°C
Storage Temperature, Ambient	−65°C to +200°C	−65°C to +200°C	−65°C to +200°C

ITT 3001 — ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
VF	Forward Voltage		1.0	Volts	IF = 100 ma
IR_1	Reverse Current		0.025	ua	VR = 60 V
IR_2	Reverse Current (150°C)		5	ua	VR = 60 V
BV	Breakdown Voltage	70		Volts	IR = 100 ua
Co	Capacitance		8	pf	VR = 0 V, f = 1 MHz

NOTES:
1. The maximum ratings are limited values above which life or satisfactory performance may be impaired.
2. All Diodes must have black body coat.

ITT3002 — ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
VF	Forward Voltage		1.0	Volts	IF = 200 ma
IR_1	Reverse Current		1.0	na	VR = 125 V
IR_2	Reverse Current (150°C)		3.0	ua	VR = 125 V
BV	Breakdown Voltage	150		Volts	IR = 100 ua
Co	Capacitance		6.0	pf	VR = 0 V, f = 1 MHz

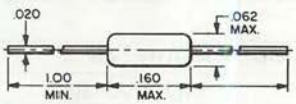
ITT3003 — ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
VF	Forward Voltage		1.0	Volts	IF = 100 ma
IR_1	Reverse Current		.025	ua	VR = 175 V
IR_2	Reverse Current (150°C)		5	ua	VR = 175 V
BV	Breakdown Voltage	200		Volts	IR = 100 ua

GENERAL PURPOSE SILICON DIODE

This device is a Silicon Double Plug Diode for general-purpose, high-temperature application in computer, industrial and military applications.

DIMENSIONS



DOUBLE PLUG DIODE

ABSOLUTE MAXIMUM RATINGS

Storage temperature range, T_{stg} ..... −55°C to +200°C

Lead or terminal temperature at a distance not less than 1/16″ from the seated surface (or case) for 2 seconds ..... +275°C

	1N5194	1N5195	1N5196
Reverse voltage, 25°C free air	80 V	200 V	250 V
Maximum steady state power dissipation at 25°C, free air	250mw	250mw	250mw
Derating factor	1.43mw/°C	1.43mw/°C	1.43mw/°C

ELECTRICAL CHARACTERISTICS

	1N5194		1N5195		1N5196	
	MIN	MAX	MIN	MAX	MIN	MAX
Forward Voltage, Vf @ If = 100 ma		1.0 V		1.0 V		1.0 V†
Breakdown Voltage, Bvr Ir = 100 ua	80 V		200 V		250 V	
Reverse Current, Ir @ Vr = 70 V		25 na		25 na*		25 na*
Reverse Current, Ir @ Vr = 70 V @ 150°C		5 ua		5 ua*		5 ua*

† Pulsed—width 8.5 msec max duty cycle 2% or less

* Vr = 180V

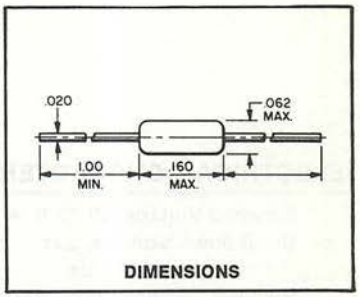
* Vr = 225V

CROSS-REFERENCE TO ELECTRICAL EQUIVALENTS

DO-7 TYPES	DPD TYPES
IN483B	IN5194
IN485B	IN5195
IN486B	IN5196

GENERAL PURPOSE SILICON DIODES

This device is a Silicon Double Plug Diode for general purpose use in computer, industrial and military applications.



DIMENSIONS

ABSOLUTE MAXIMUM RATINGS

Storage temperature range, T_{stg} ..... −65°C to +200°C

Lead or terminal temperature at a distance not less than 1/16″ from the seated surface (or case) for 15 seconds ..... +275°C

	1N5605	1N5606	1N5607	1N5608/9
Reverse voltage, 25°C free air	70 V	150 V	200 V	120 V
Maximum steady state power dissipation at 25°C, free air	250mw	200mw	200mw	250mw
Derating factor				2mw/°C

ELECTRICAL CHARACTERISTICS

	1N5605		1N5606*		1N5607*	
	MIN	MAX	MIN	MAX	MIN	MAX
Forward Voltage, Vf @ If = 20 ma		1.0 V		1.0 V		1.0 V
Breakdown Voltage, Bvr Ir = 100 ua	70 V		150 V		200 V	
Reverse Current, Ir @ Vr = 60 V		25 na		25 na		25 na
Reverse Current, Ir @ Vr = 60 V @ 150°C ..		5 ua		5 ua		5 ua

*If = 7 ma, Vr = 125 V *If = 3 ma, Vr = 175 V

ELECTRICAL CHARACTERISTICS — 1N5608	MIN	MAX
Forward Voltage, Vf @ If = 100 ma		1.0 V
Breakdown Voltage, Bvr		
Ir — 100 ua	120 V	
Reverse Current, Ir @ 50 V		50 na
Reverse Current, Ir @ 50 V @ 150°C		25 ua
*Reverse Recovery Time, Trr		
If = 5 ma, Vr = 40 V		
R1 = 2 K, C1 = 10 pf		
Recover to 80K ohms		300 nsec

ELECTRICAL CHARACTERISTICS — 1N5609	MIN	MAX
Forward Voltage, Vf @ If = 6 ma		1.0 V
Breakdown Voltage, Bvr		
Ir = 100 ua	120 V	
Reverse Current, Ir @ 100 V		5 ua
Reverse Current, Ir @ 100 V @ 100°C		50 ua
Capacitance, C		
Vr = 10 V, f = 1 mc		2.7 pf
Reverse Recovery time, Trr		
If = 30 ma, Vr = 35 V,		
Recover to 400K ohms		300 nsec

CROSS-REFERENCE TO ELECTRICAL EQUIVALENTS

DO-7 TYPES	DPD TYPES
1N457	1N5605
1N458	1N5606
1N459	1N5607
1N658	1N5608
1N660	1N5609