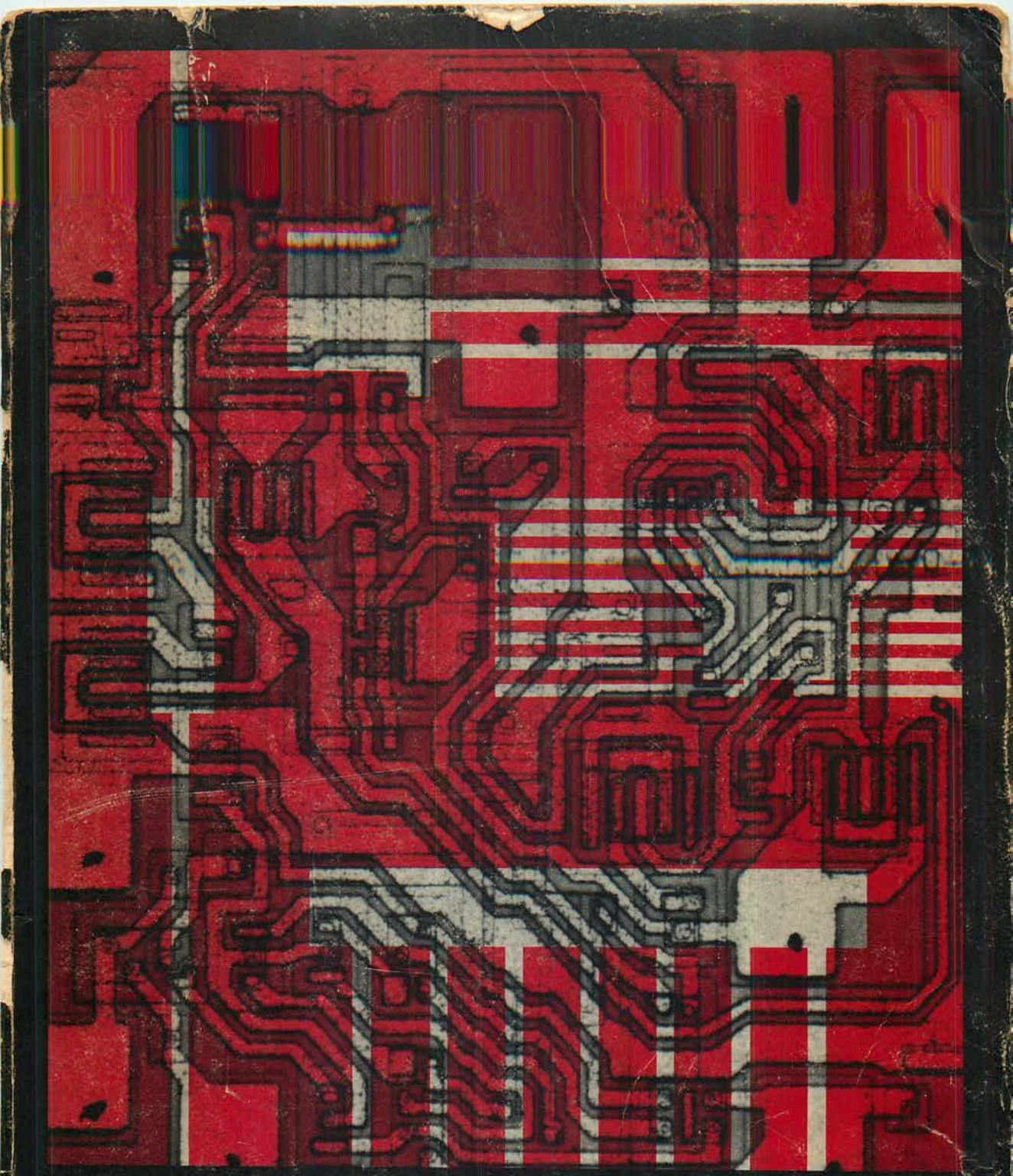

PRODUCT CATALOG 1972/1973

ITT
SEMICONDUCTORS

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725M72

Printed In U.S.A.

All ITT integrated circuits are available both in wafer and in chip form. Since the completed individual encapsulated product is capable of being more extensively and thoroughly tested than the wafer, these specifications are limited to the capability of the chip and the attendant testing equipment.

USE

DTL and Linear circuits are normally supplied with plain backing. Gold backing can be furnished upon special request. All other circuits are supplied with gold backing. Recommended die attach temperature is 420°C for either type of backing. A 98% gold, 2% silicon preform is recommended for die attach with all plain-backed chips. One mil aluminum wire, ultrasonically bonded to the pads, is recommended for connecting the chip to the circuit.

PACKAGING FOR SHIPMENT

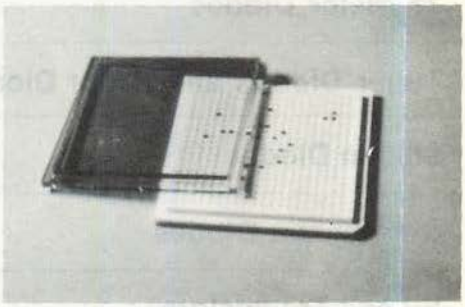
Wafers will be shipped in the plastic package shown. Chips will be packaged in carriers as indicated.

IDENTIFICATION

All integrated circuit dice will be identified by the appropriate three or four-digit code, together with the individual suffix number indicating the temperature range.

For example, a 930 limited-temperature range chip would be a "930-5." A 930 full-temperature range chip would be a "930-1."

I. C. WAFER PACKAGE



CHIP PACKAGE

MIL AND HI-REL SEMICONDUCTORS

Virtually all ITT Semiconductors are available with hi-rel processing. IC's, for example, can be processed for any portions of, or all of, MIL-STD-883 and MIL38510. Many diodes and transistors are available as JAN, JAN/TX, or MIL types.

Whenever you need hi-rel semiconductors, check ITT. Your local representative can give up-to-date information on availability, price, etc.

This series offers a wide range of digital integrated circuit devices from simple NAND gates to large complex functions. They form a TTL family (Transistor-Transistor Logic) guaranteed to operate over the following ambient temperature ranges:

Military range, 54 series	−55°C to 125°C
Industrial range, 74 series	0°C to 75°C

All devices operate over a frequency range between D.C. and typically 20 MHz, and are fully compatible with all 54/74 series TTL and 930 series DTL.
Clamping diodes are provided at the inputs to enhance the inherent high noise immunity when driving transmission lines. Most outputs are of totem pole configuration to give good drive capability, i.e. high fan-out, especially into large capacitive loads. Other outputs include an open-circuit collector connection.

FEATURES

High speed—typical propagation delay (gate) of 9 ns.
Guaranteed noise margin—greater than 400 mV.
Low power dissipation—10 mW per gate at 50% duty cycle.
Worst case fan-out of 10.
Low output impedance.
Logic levels guaranteed over range of supply voltage and operating temperature
Wide range of functions—many SSI and MSI functions.
Compatible with other DTL, TTL logic series.

INDEX FOR STANDARD 7400 SERIES

For the military range, replace 74 in the type number by 54.

TYPE	DESCRIPTION
ITT7400	Quad 2 i/p NAND
ITT7401	Quad 2 i/p NAND (open-collector 5-5 V rating)
ITT7401A	Quad 2 i/p NAND (open-collector 15 V rating)
ITT7402	Quad 2 i/p NOR
ITT7403	Quad 2 i/p NAND (open-collector 5-5 V rating)
ITT7403A	Quad 2 i/p NAND (open collector 15 V rating)
ITT7404	Hex inverter
ITT7405	Hex inverter (open-collector 5-5 V rating)
ITT7405A	Hex inverter (open-collector 15 V rating)
ITT7406	Hex inverter buffer/driver (open-collector 30 V rating)
ITT7407	Hex buffer/driver (open-collector 30 V rating)
ITT7410	Triple 3 i/p NAND
ITT7412	Triple 3 i/p NAND (open-collector 5 V rating)
ITT7412A	Triple 3 i/p NAND (open-collector 15 V rating)
ITT7413	Dual 4 i/p Schmitt Trigger
ITT7416	Hex inverter buffer/driver (open-collector 15 V rating)
ITT7417	Hex buffer/driver (open-collector 15 V rating)
ITT7420	Dual 4 i/p NAND
ITT7426	Quad 2 i/p high voltage interface NAND (open collector
ITT7428	Quad 2 i/p NOR buffer
ITT7430	8 i/p NAND
ITT7437	Quad 2 i/p NAND buffer
ITT7438	Quad 2 i/p NAND buffer (open collector 5.5 V rating)
ITT7440	Dual 4 i/p NAND Buffer
ITT7441A	B.C.D. to decimal decoder/driver
ITT7442	B.C.D. to decimal decoder
ITT7443	Excess 3 to decimal decoder
ITT7444	Excess 3 gray to decimal decoder
ITT7445	B.C.D. to decimal decoder (open collector 30 V rating)
ITT7450	Expandable dual 2 wide, 2 i/p A.O.I.
ITT7451	Dual 2 wide, 2 i/p A.O.I.
ITT7453	Expandable 4 wide, 2 i/p A.O.I.
ITT7454	4 wide, 2 i/p A.O.I.
ITT7460	Dual 4 i/p expander
ITT7470	D.C. clocked J-K flip-flop
ITT7472	J-K master-slave flip-flop
ITT7473	Dual J-K master-slave flip-flop
ITT7474	Dual D-type edge-triggered flip-flop
ITT7475	Quad bistable latch
ITT7476	Dual J-K master-slave flip-flop with preset and clear
ITT7480	Gated full adder
ITT7481	16-bit full memory
ITT7482	2-bit full adder
ITT7483	4-bit full adder
ITT7484	16-bit memory
ITT7486	Quad 2 i/p exclusive—OR
ITT7490	Decade counter
ITT7491A	8-bit shift register
ITT7492	Divide by 12 counter
ITT7493	4-bit binary counter
ITT7494	5-bit shift register
ITT7495	4-bit shift register (reversible)
ITT7496	4-bit shift register
ITT74104	Gated J-K master-slave flip-flop (see ITT9000)

TYPE	DESCRIPTION
ITT74105	Gated J-K master-slave flip-flop (see ITT9001)
ITT74107	Dual J-K master-slave flip-flop
ITT74118	Hex set/reset latch
ITT74121	Monostable
ITT74145	B.C.D. to decimal decoder (open-collector 15 V rating)
ITT74150	16-bit data selector/multiplexer
ITT74151	8-bit data selector/multiplexer
ITT74154	4-line-to-16-line decoder/demultiplexer (see ITT9311)
ITT74155	Dual 2 to 4 line decoder/demultiplexer
ITT74156	Dual 2 to 4 line decoder/demultiplexer (o/c 5-5V rating)
ITT74161	Synchronous binary up counter (see ITT9316)
ITT74180	8-bit parity generator/checker
ITT74192	Synchronous BCD-Up/Down counter
ITT74193	Synchronous Binary 4-bit up/down counter

FUNCTIONAL INDEX

Gates

FUNCTION	TYPE
NAND	ITT7400
	ITT7401*
	ITT7401A*
	ITT7403*
	ITT7403A*
	ITT7410
	ITT7412
	ITT7412A
	ITT7420
	ITT7426*
	ITT7430
	ITT7437
	ITT7438
	ITT7440
NOR	ITT7402
	ITT7428
Inverter	ITT7404
	ITT7405*
	ITT7405A*
	ITT7406
	ITT7416
Non-Inverter	ITT7407
	ITT7417
Schmitt Trigger	ITT7413
And-Or-Invert (A.O.I.)	ITT7450
	ITT7451
	ITT7453
	ITT7454
Expander	ITT7460*
Exclusive OR	ITT7486

Flip-flops

FUNCTION	TYPE
J-K	ITT7470
	ITT7472
	ITT7473
	ITT7476
	ITT74104
	ITT74105
	ITT74107
D-type	ITT7474
Latch	ITT7475
	ITT74118

Counters

Decade	ITT7490
Divide by 12	ITT7492
	ITT74192
Divide by 16	ITT7493
	ITT74161
	ITT74193

Shift registers

4 Bit	ITT7494
	ITT7495
5 Bit	ITT7496
8 Bit	ITT7491A

Memories

16 Bit RAM	ITT7481
	ITT7484

Decoders/demultiplexers

B.C.D. to decimal	ITT7441A*
	ITT7442
	ITT7445*
	ITT74145*
Excess 3 to decimal	ITT7443
Excess 3 gray to decimal	ITT7444
4 Line to 16 line	ITT74154
2 Line to 4 line	ITT74155
	ITT74156*

Data selector/multiplexer

16 Bit	ITT74150
8 Bit	ITT74151

Adders

2 Bit	ITT7482
4 Bit	ITT7483
1 Bit	ITT7480

Monostable

	ITT74121

Parity gen/check

8 Bit	ITT74180

*Devices with open collector outputs.

INTRODUCTION TO TTL

The TTL circuit configurations are designed so that the uniform logic and noise margin levels apply to all the standard devices in the families. Thus many parameters and their limits are common. In addition the operating conditions are identified for each family. Once these standard operating conditions are understood it becomes possible for the designer to use the family by simply referring to the logic and connection diagrams on each data sheet. All common information is included in the remainder of this section.

For ease of reading, the data only refers to the ITT7400 series family but it is equally applicable to the ITT5400 series. Where there are exceptions these are clearly indicated on the individual data sheets concerned.

LOGIC DEFINITION

Positive logic is used throughout the data sheets. This is defined as follows.

Logical '0' = Low voltage; typically 0.2 V but ⟨ 0.8 V
Logical '1' = High voltage; typically 3.3 V but ⟩ 2.0 V

Current flowing into a device terminal is defined as positive.

D.C. CHARACTERISTICS COMMON TO ALL DEVICES (except where otherwise stated)

D.C. tests are carried out under the specified conditions. All inputs and outputs are tested for all possible logic states. Worst state load currents and voltages are applied and the test limits are applicable over the full temperature range.

	Min.	Max.	Unit
Supply voltage, V_{CC}:			
74 series	4.75	5.25	V
54 series	4.5	5.5	V
Operating temperature:			
74 series	0	75	°C
54 series	−55	125	°C

D.C. noise margin typically greater than 1V.

ABSOLUTE MAXIMUM RATINGS

(above which the useful life of the device may be impaired)

Continuous supply voltage V_{CC} (Note 1) 7V
Input voltage . . . . . 5.5 V
Voltage between inputs . . . . . 5.5 V
Continuous input current . . . . . −10 mA
Standard output voltage . . . . . −0.5 to 5.5 V
Storage temperature . . . . . −65°C to 150°C

Note I
This rating is reduced to 5.5 V if unused inputs are connected directly to V_{CC}.

STANDARD CHARACTERISTICS (limits apply over the full range of operating temperature and for standard totem pole output except where otherwise stated).

PARAMETER	LIMIT (Note 8)				CONDITIONS	
	Min.	Typ.	Max.	Unit	V_{CC}	
V_{IH}	2.0			V	Min.	V_{OL} ⟨ 0.4V or V_{OH} ⟩ 2.4V (Note 1)
V_{IL}			0.8	V	Min.	V_{OL} ⟨ 0.4V or V_{OH} ⟩ 2.4V (Note 2)
V_{OL} (standard output)		0.22	0.4	V	Min.	I_{OL}=16 mA, V_{IH}=2V or V_{IL}=0.8V (Note 3)
V_{OL} (buffer output) V_{OH}	2.4	3.3		V	Min.	V_{IL}=0.8V or V_{OH}=2.0V (Note 4)
I_{CEX} open collector only			250	μA	Min.	V_{IL}=0.8V, V_{IH}=2V, V_{OUT}=max. o/p voltage rating
$-I_F$		1.0	1.6	mA	Max.	V_F=0.4V (Note 5)
I_R			40	μA	Max.	V_R=2.4V, input loading-1 unit load (Note6)
I_R			1.0	mA	Max.	V_R=5.5 V irrespective of input loading
$-I_{SC}$						
54 series	20		55	mA	Max.	V_{OUT}=0 V (Note 7)
74 series	18		55	mA	Max.	V_{IH}=2.0V or V_{IL}=0.8V; apply according to logic function

Where characteristics for devices differ from the above table these are shown in the data sheets.

Note 1
Condition at outputs dependent on the truth table of the device. For example, for gates and buffers, V_{OL} ⟨ 0.4 V applies, and for flip-flops, shift registers, counters, decoders, etc. either V_{OL} ⟨ 0.4 V or V_{OH} ⟩ 2.4 V applies at each output. Output conditions do not apply for 7486, 7460, 7445, 74145, and 7441A. This parameter does not apply for 7413 and 74121, because of the Schmitt trigger inputs.

Note 2
Conditions at outputs dependent on the truth table of the device, for example; for gates and inverters V_{OH} ⟩ 2.4 V. Output conditions do not apply for devices with open collector output. This parameter does not apply for 7413, 74121.

Note 3
Conditions V_{IH} and V_{IL} depend on device truth table. Limits for 7441A, 7445 and 74145 are shown on the appropriate data sheets.

Note 4
This parameter for totem pole output devices only. V_{IL} and V_{IH} apply according to the truth table. I_{OH}=−400 μA for devices with Fan-out=10; I_{OH}= −800 μA for devices with Fan-out=20; I_{OH} = −1.2 mA for devices with Fan-out=30, etc.

Note 5
Limits apply for an input loading of 1 unit load; for other input loadings multiply limits by number of unit loads. For flip-flops, see appropriate data for test conditions.

Note 6
All other inputs at 0 V for 7472, 7473, 7476, 74107. For 7470 all other inputs at 0 V except J and K which are at 4.5 V. For 7474 consult data sheet. Limits to be multiplied by the input loading of the device.

Note 7
Maximum limit = 57 mA for devices with internal feedback connections, (e.g. flip-flops and some complex devices). For 7400 series simple NAND gates not more than two outputs may be shorted at any time. For all other devices and for all 5400 series not more than one output to be shorted at any time. Open collector devices: no parameter for $-I_{SC}$.

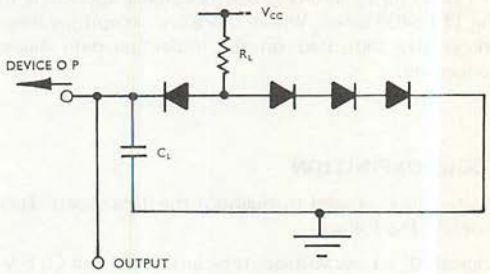
Note 8
Typical limits are at ambient temperature, T_A=25°C and V_{CC}=5 V.

A.C. TESTS

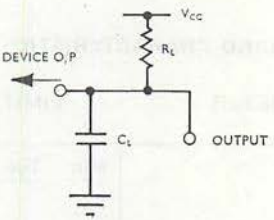
Testing of propagation delays is carried out using the typical switching load circuits shown below. These load circuits are designed to simulate full fan-out loading. An oscilloscope with high impedance probes and having a bandwidth of at least 100 MHz is suitable for these measurements.

TYPICAL SWITCHING TEST LOAD CIRCUITS

For totem pole outputs:



For open collector outputs:



ORDERING CODE FOR TTL CIRCUITS

Operating Temperature Range
5400 series −55 to +125°C
7400 series 0 to +75°C

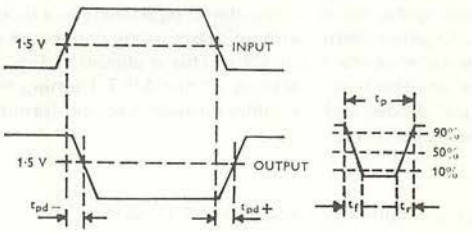
Package (add)
B for Flat Pack
J for Ceramic Dual In-Line
N for Plastic Dual In-Line

Example:
ITT7400J
is 0°C to +75°C Range in Ceramic Dual In-Line Package

Notes

1. Diodes are type 1N4148.
2. The values of C_L and R_L are quoted in the data sheets. Value of C_L includes probe and jig capitance.
3. The characteristics of the pulse generator used at the input of the device are stated in the data sheets. Typical characteristics are: V_{OUT}=3.5V; Rise time, tr, =Fall time, t_f,=less than 15 ns; Z_o = 50 Ω; Pulse Repetition Frequency, P.R.F. = 1 MHz; Pulse width for gate, t_p = 500 ns.

Waveforms



1. HIGH LOGIC STATE '1' (ON STATE)

The NAND gate has two stable operating states. These are illustrated in Figs. 1A and 1B.

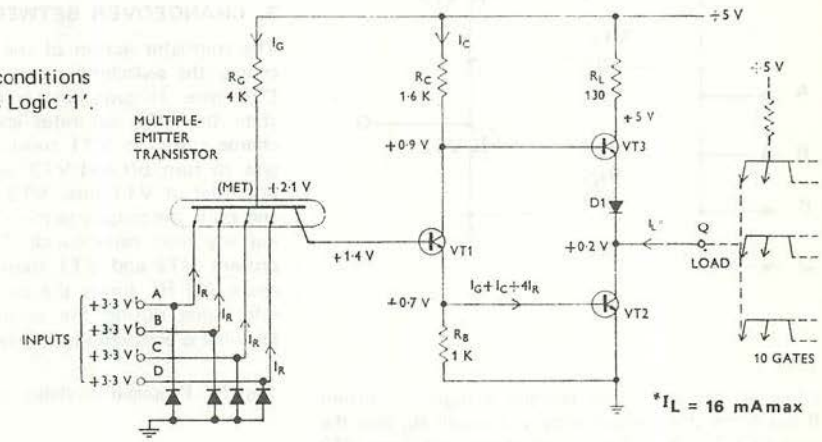


Fig. 1A. Typical 'ON' conditions with all inputs Logic '1'.

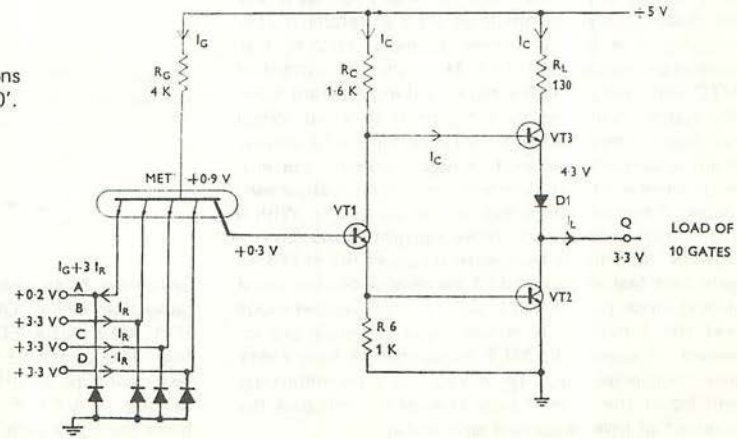
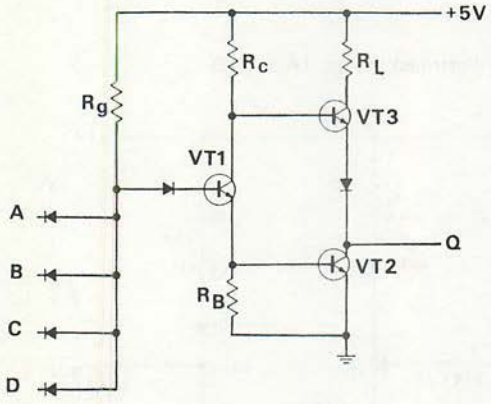


Fig. 1B. Typical 'OFF' conditions with one input Logic '0'.

The d.c. operation of this circuit is more readily understood if the multiemitter transistor (MET) connecting the inputs is considered equivalent to a diode AND gate in series with an offset diode connected to the base of transistor VT1. This is shown in Fig. 2, the emitter-base junctions of the MET forming the input diodes and the collector-base junction forming the offset diode.

Fig. 2. Simplified analogy of TTL gate.



When all the inputs are positive a logic '1' current flows from the positive supply through R_g into the base of VT1 which heavily conducts and turns VT2 'ON' into the saturated state. Since both VT1 and VT2 are saturated, there is insufficient voltage across the base emitter terminals of VT3 to render it conducting. The output voltage is about +0.2 V, (i.e. saturation voltage of VT2). The collector current of VT2 will consist of the total 'sinking' current from the gates connected to the output terminal. When the base current drive to VT2 is high, VT2 can remain saturated even with a large collector current, with adverse circuit tolerances and temperature variations. This permits a fan-out of up to 10. With a multiemitter transistor, more current flows from a positive held input than with a conventional D.T.L. gate (the leakage current of the reverse biassed input diode) since the MET is biassed in the inverted mode and the functions of emitter and collector are reversed. However, the MET is designed to have a very low inverse gain and I_R is kept to a minimum. I_R will equal the emitter base leakage current plus the product of inverse current gain and I_G.

2. LOW OR OFF STATE

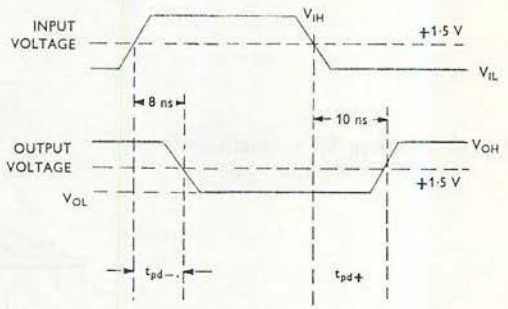
The opposite state shown in Fig. 1B is achieved if the voltage of any number of inputs is reduced below a threshold level of about + 1.5 volts. Fig. 1B shows the conditions when input A is at +0.2 volts (a typical output voltage of a previous gate). No base current flows into VT1 since the collector of the MET is at too low a potential, with respect to its base.

Therefore, no current will flow through VT1 and VT2 other than leakage current (which can be neglected in this analysis). The transistor VT3 will conduct to provide sufficient output current to maintain following gates connected to the output terminal at 3.3 V positive in logic 1. The fan-out is high (10) under worst case conditions because of the low output impedance of VT3.

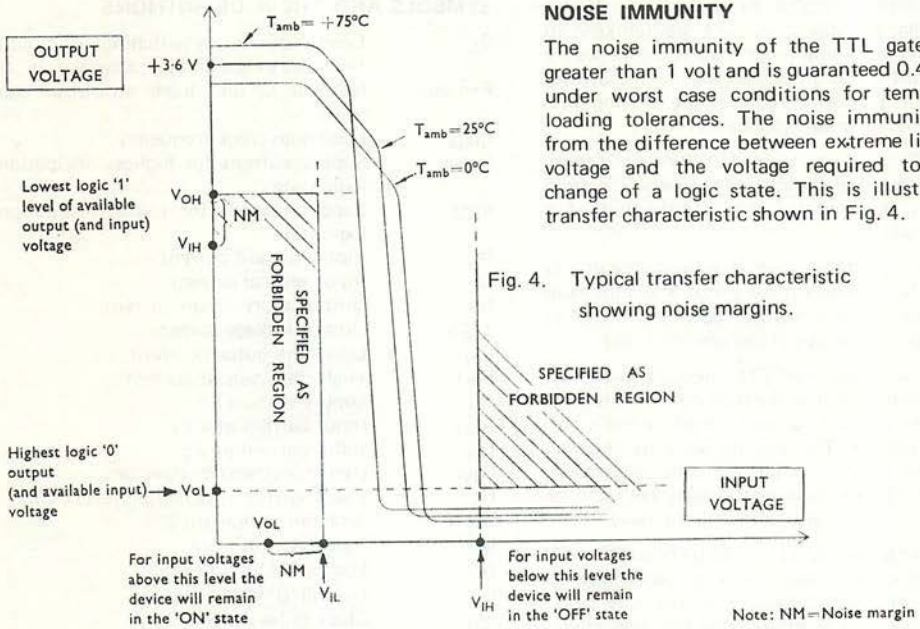
3. CHANGEOVER BETWEEN STATES

The transistor action of the MET considerably improves the switching speed when compared with a DTL gate. In switching from the ON to the OFF state the MET saturates and rapidly removes the charge stored in VT1 turning it off. Then VT2 begins to turn off and VT3 turns on as the collector potential of VT1 rises. VT3 assists VT2 to turn off and pulls the output terminal rapidly positive, charging any load capacitance. The diode D1 helps to prevent VT2 and VT1 from conducting simultaneously and RL limits the current through VT3 to a safe value during the switch over if the output terminal is accidentally shorted.

Fig. 3. Propagation delay waveforms.



Switching from the OFF to the ON state is more rapid than ON to OFF since none of the transistors VT1, VT2 and MET are saturated in the OFF condition. The switch to the ON condition is particularly fast owing to additional drive by transistor VT1 in turning on VT2. Fig. 3 shows the typical switching times from this gate.



NOISE IMMUNITY

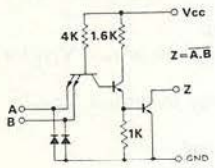
The noise immunity of the TTL gate is typically greater than 1 volt and is guaranteed 0.4 V minimum under worst case conditions for temperature and loading tolerances. The noise immunity is derived from the difference between extreme limits of input voltage and the voltage required to ensure the change of a logic state. This is illustrated by the transfer characteristic shown in Fig. 4.

Fig. 4. Typical transfer characteristic showing noise margins.

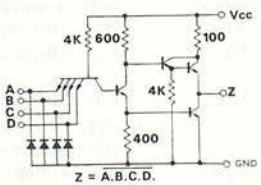
GATES DIFFERING FROM THE STANDARD CIRCUIT

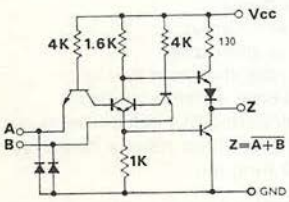
Typical variations from the standard NAND gate circuit configuration are shown in the following circuit diagrams.

Open collector (e.g. 7401)



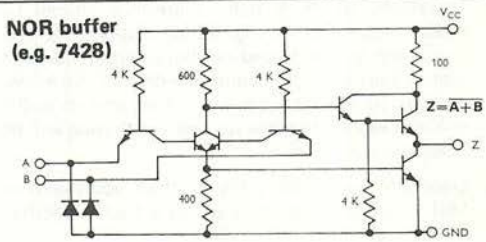
NAND buffer (e.g. 7440)

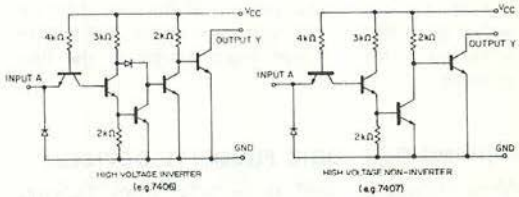




NOR gate (e.g. 7402)

NOR buffer (e.g. 7428)





BASIC RULES FOR THE USE OF TTL DEVICES

1. Spare inputs should be connected to used inputs if the fan-out permits. Otherwise connected to the V_{CC} power line via a resistor of value 1 K ohm or greater. This is particularly important for the 'preset' and 'clear' asynchronous inputs.
2. Gates from the same package may be paralleled where necessary for better driving capability.

3. Interconnection lengths of 12 inches or less (capacitance of about 50 pF) are unlikely to give ringing problems; lengths up to 24 inches are possible with good ground arrangements. Greater length will probably require line driving precautions (see separate Application Note).
4. 'Wired-OR' can be performed at the output terminals of open-collector networks however a speed penalty is incurred by the introduction of a resistive pull-up.
5. In calculating system speeds, due allowance should be made for the maximum set-up and minimum clock pulse width times on flip-flops, as well as the propagation delays of the elements used.
6. If relays are driven from TTL circuitry, care must be taken to ensure that the load connection wires to the relay contacts do not introduce noise into the logic system. This can be done by allowing these wires only to enter the logic system enclosure at a point close to the relay contacts, or in extreme cases by also shielding the relay.
7. Similarly external inputs should be brought on to the printed circuit connections at right angles to the other wiring, the printed circuit itself being laid out to ensure least coupling between inputs and other connections.
8. If system speed is high, allowance should be made when calculating power supply requirements for the increased network supply currents due to current spiking and line driving. An allowance at 10 MHz of 15% for spiking and up to 0.5 mA per each gate node for the line driving will be adequate for this.
9. Decouple every 10 gates or their equivalent in MSI functions with 0.01 μF to 0.1 μF capacitors of R.F. rating.

In conclusion, a careful perusal of the data sheet together with the points mentioned above, will help in achieving a trouble free logic design at the first attempt.

DRIVING DTL LOGIC FROM TTL DEVICES

When driving ITT930 series DTL from 74/5400 series TTL the full fan-out of the TTL is available.

DRIVING TTL LOGIC FROM DTL DEVICES

Driving ITT7400 series TTL from ITT930 series DTL necessitates a reduction of the full fan-out from 8 to 3 for standard gates and from 25 to 20 for buffers. Increased fan-out can be achieved with standard DTL gates by using an additional pull-up resistor.

SYMBOLS AND THEIR DEFINITIONS

C_L	Load capacitor in switching test circuit (includes probe and jig capacitance).
Fan-out	Number of unit loads an output can drive.
f_{max}	Maximum clock frequency.
I_{CCH}	Supply current for highest dissipation logic state.
I_{CCL}	Supply current for lowest dissipation logic state.
I_F	Input forward current.
I_R	Input reverse current.
I_{SC}	Output short circuit current.
I_{CEX}	Output leakage current.
I_{OL}	Low state output current.
I_{OH}	High state output current.
I_{CC}	Supply current.
I_{IN+}	Input current at V_{T+}.
I_{IN-}	Input current at V_{T-}.
P_{dyn}	Dynamic power dissipation.
R_L	Load resistor in switching test circuit.
T_A	Ambient temperature.
t_h	Input hold time.
t_{h+}	Logical '1' hold time.
t_{h-}	Logical '0' hold time.
t_{cp}	Clock pulse width.
t_p	Preset or clear pulse width.
t_{po}	Output pulse width.
t_{pd+}	Propagation delay to logical '1' on output.
t_{pd-}	Propagation delay to logical '0' on output.
t_n	State of output (or input) before the active edge of the clock pulse.
t_{n+1}	State of output (or input) after the active edge of the clock pulse.
t_{min}	Minimum width trigger pulse.
t_{sp+}	Logical '1' input set up time.
t_{sp-}	Logical '0' input set up time.
V_{CC}	Supply voltage.
V_H	Hysteresis voltage.
V_{IH}	Input high voltage to ensure V_{OL} (or V_{OH})*.
V_{IL}	Input low voltage to ensure V_{OH} (or V_{OL})*.
V_{OL}	Output low voltage.
V_{OH}	Output high voltage.
$V_{OH(M)}$	Output breakdown voltage of open collector device.
V_{IN}	Voltage at an input.
V_{OUT}	Voltage at an output.
V_{T+}	Positive edge threshold voltage.
V_{T-}	Negative edge threshold voltage.
WIRED-OR	The commoning of open collector outputs with a pull-up resistor to perform the AND function.

*Output level dependent on device logic as found from truth table.

ITT7400	Quad 2 input NAND gate
ITT7401 ITT7401A	Quad 2 input NAND gate with open collector output
ITT7402	Quad 2 input NOR gate
ITT7403 ITT7403A	Quad 2 input NAND gate with open collector output
ITT7404	Hex inverter
ITT7405 ITT7405A	Hex inverter (open collector)
ITT7406	Hex inverter/buffer/driver (open collector)
ITT7407	Hex buffer/driver (open collector)
ITT7410	Triple 3 input NAND gate
ITT7412	Triple 3 input NAND gate (open collector)
ITT7412A	Triple 3 input NAND gate (open collector)
ITT7416	Hex inverter/buffer/driver (open collector)
ITT7417	Hex inverter/driver (open collector).
ITT7420	Dual 4 input NAND gate
ITT7426	Quad 2 input high voltage interface NAND gate (open collector)
ITT7428	Quad 2 input NOR buffer
ITT7430	Single 8 input NAND gate
ITT7437	Quad 2 input NAND buffer
ITT7438	Quad 2 input NAND buffer (open collector)
ITT7440	Dual 4 input NAND buffer

DESCRIPTION

ITT7400, ITT7410, ITT7420, ITT7430, ITT7440 are standard totem pole output gate devices.
ITT7401(A), ITT7403(A), ITT7405(A), ITT7412(A), ITT7438 are open collector output devices featuring:

Wired or capability
Output rating 5.5V - Suffix "A" denotes 15V

ITT7406, 7416, 7407, 7417 are high voltage open collector devices featuring:

Output rating 30V (54/7406, 54/7407), 15V (54/7416, 54/7417)
Sink current 40 mA (7406, 07, 16, 17), 30 mA (5406, 07, 16, 17)

ITT7426 is an open collector device featuring:

Wired or capability
Output rating 15V
Low I_{CEX}
} **Suitable as MOS interface device**

ITT7437, 7438, 7440 is a NAND buffer featuring a FAN OUT OF 30.
ITT7402 is a NOR gate with standard totem pole output.
ITT7428 is a NOR buffer featuring: FAN OUT OF 30.

The circuits of all these devices are the same as those shown in the general information section, except some have a different number of inputs.

TYPICAL CHARACTERISTICS

Device type		Propagation delay ns	Power dissipation per package (50% duty cycle) mW
Quad 2 input NAND	7400	9	40
Triple 3 input NAND	7410	9	30
Dual 4 input NAND	7420	9	20
Single 8 input NAND	7430	9	10
Open collector 2 input NAND	7401,01A	22	40
	7403,03A	22	40
	7412,12A	22	40
Quad 2 input interface NAND	7426	22	40
Hex inverter	7404	9	60
Open collector Hex inverter	7405(A)	24	60
	7406,16	15	105
	7407,17	14	145
Dual 4 input NAND buffer	7440	9	53
Quad 2 input NAND buffer	7437	10	107
Quad 2 input NAND buffer (Open Collector)	7438	12	93
Quad 2 input NOR gate	7402	9	55
Quad 2 input NOR buffer	7428	9	100

Input loading factor . . . . . 1 unit load

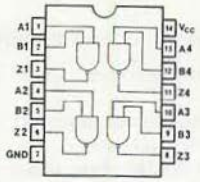
Fan out (for totem pole outputs):
- Standard gates . . . . . 1 to 10 unit loads
- Buffer gates . . . . . 1 to 30 unit loads

7406, 07, 16, 17 . . . . . 40 mA Sink Current
7406, 07, 16, 17 30 mA Sink Current

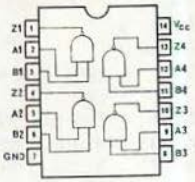
Output voltage rating for open collector outputs 5.5V
Except those with suffix A and 7426, 7416, 7417 . . . . . 15.0V
Except 7406, 7407. . . . . 30.0V

Pin configuration (top view)

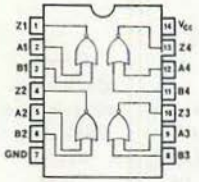
7400, 7403, 7403A, 7426, 7437, 7438



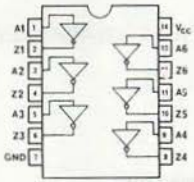
7401, 7401A



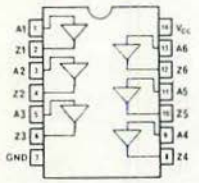
7402, 7428



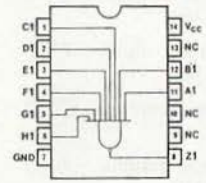
7404, 7405, 7405A, 7406, 7416



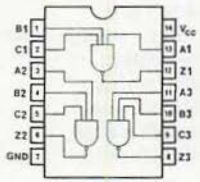
7407, 7417



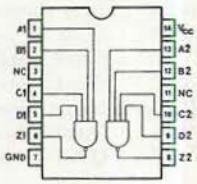
7430



7410, 7412, 7412A



7420, 7440



D.C. CHARACTERISTICS

Information on the absolute maximum ratings and the other D.C. characteristics of these devices (which are common to other integrated circuits in this series) is stated in the general information section.

PARAMETER	LIMIT				CONDITIONS	
	Min.	Typ.	Max.	Unit	V_{CC}	
I_{CCL}						
ITT7400, 01, 01A, 03, 03A, 26		12	22	mA	Max.	V_{IN} on all inputs=5.0V
7407, 17		21	30	mA		
7410, 12, 12A		9	16.5	mA		
7406, 16		24	38	mA		
7420		6	11	mA		
7430		3	5.5	mA		
7404, 05, 05A		18	33	mA		
7440		17	27	mA		
7402		14	27	mA		
7428		35	56	mA		
7437, 38		34	54	mA		

PARAMETER	LIMIT				CONDITIONS	
	Min.	Typ.	Max.	Unit	V_{CC}	
I_{CCH}						
7400, 01, 01A, 03, 03A		4	8	mA	Max.	V_{IN} on all inputs=0 V
7406, 16		30	42	mA		
7407, 17		29	41	mA		
7410, 12, 12A		3	6	mA		
20		2	4	mA		
30		1	2	mA		
26, 40		4	8	mA		
04, 05, 05A		6	12	mA		
02		8	16	mA		
28		12	24	mA		
37		9	15.5	mA		
38		5	8.5	mA		

Exceptions to common characteristics:

PARAMETER		LIMIT				CONDITIONS	
		Min.	Typ.	Max.	Unit	V_{CC}	
$-I_{SC}$	7428	40		125	mA	Max.	*V_{OUT}=0V
$-I_{SC}$	7440	18		70	mA	Max.	*V_{OUT}=V_{IN}=0V
$-I_{SC}$	5440,54/7437	20		70	mA	Max.	*V_{OUT}=V_{IN}=0V
$V_{OH(M)}$	7426	15			V	Min.	V_{IL}=0.8V, I_{OH}=1mA
I_{CEX}	7426			50	μA	Min.	V_{IL}=0.8V, V_{OUT}=12V
V_{OL}	7406/16			0.7V.		Min.	V_I=2.0V, I_{OL}=40mA
V_{OL}	5406/16			0.7V		Min.	V_I=2.0V, I_{OL}=30mA
V_{OL}	7407/17			0.7V		Min.	V_I=0.8V, I_{OL}=40mA
V_{OL}	5407/17			0.7V		Min.	V_I=0.8V, I_{OL}=30mA
V_{OL}	54/7407/17			0.4V		Min.	V_I=0.8V, I_{OL}=16mA
I_{OH}	54/7406			250μA		Min.	V_I=0.8V, V_{OH}=30V
I_{OH}	54/7416			250μA		Min.	V_I=0.8V, V_{OH}=15V
I_{OH}	54/7407			250μA		Min.	V_I=2.0V, V_{OH}=30V
I_{OH}	54/7417			250μA		Min.	V_I=2.0V, V_{OH}=15V

*Only one output to be short-circuited at any time.

SWITCHING CHARACTERISTICS

Switching test circuits as shown in the general information section.

Note

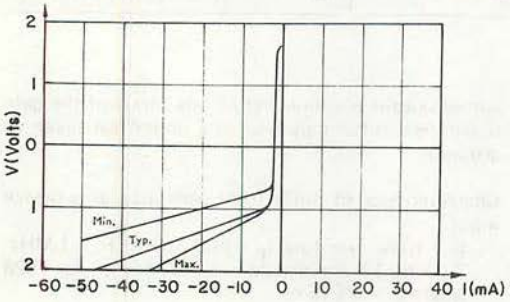
Other inputs of the gate under test taken to 2.4 V, except 7402, other input of the gate under test taken to ground. For 7428 the pulse input is taken to a 7400 series gate with the other inputs at 2.4 V and whose output is connected to one input of the gate under test (other inputs of gate under test taken to ground).

Characteristics of pulse from generator at a device input:

t_r = 10 ns, t_f = 4 ns, t_p = 500 ns, P.R.F. = 1 MHz, Z_o = 50 Ω, Amplitude = 3.5 V, except for 7428 where $t_r = t_f \leq 15$ ns.

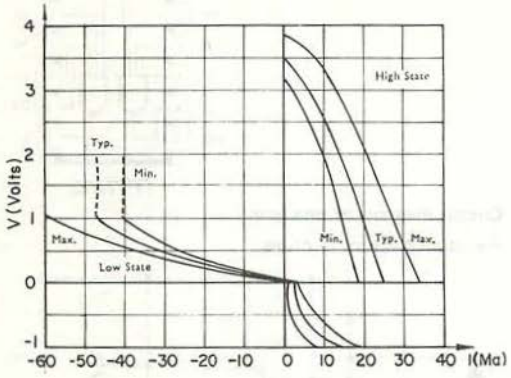
PARAMETER	LIMIT				CONDITIONS
	Min.	Typ.	Max.	Unit	
t_{pd+}					
7400,10,20,30		10	22	ns	See test circuits in introduction, C_L=15 pF, R_L=400 Ω
7401,01A,03,03A,12,12A		35	45	ns	R_L=4 K Ω, C_L=15 pF
7426		16	24	ns	R_L=1 K Ω, C_L=15 pF
7404		10	22	ns	R_L=400 Ω, C_L=15 pF
7405,05A		40	55	ns	R_L=400 Ω, C_L=15 pF
7406,16		10	15	ns	R_L=110 Ω, C_L=15 pF
7407,17		6	10	ns	R_L=110 Ω, C_L=15 pF
7440		10	22	ns	R_L=133 Ω, C_L= 15 pF
7402		10	22	ns	R_L=400 Ω, C_L=15 pF
7428		10	15	ns	R_L=133 Ω, C_L=15 pF
7437		13	22	ns	R_L=133 Ω, C_L=45 pF
7438		14	22	ns	R_L=133 Ω, C_L=45 pF
t_{pd-}					See test circuit:
7400,10,20,30		8	15	ns	R_L=400 Ω, C_L=15 pF
7426		11	17	ns	R_L=1 K Ω, C_L=15 pF
7406,16		15	23	ns	R_L=110 Ω, C_L=15 pF
7407,17		20	30	ns	R_L=110 Ω, C_L=15 pF
7401,01A,03,03A,12,12A		8	15	ns	R_L=400 Ω, C_L=15 pF
7404,05,05A		8	15	ns	R_L=400 Ω, C_L=15 pF
7440		8	15	ns	R_L=133 Ω, C_L=15 pF
7402		8	15	ns	R_L=400 Ω, C_L=15 pF
7428		8	15	ns	R_L=133 Ω, C_L=15 pF
7437		8	15	ns	R_L=133 Ω, C_L=45 pF
7438		11	18	ns	R_L=133 Ω, C_L=45 pF

TYPICAL CHARACTERISTICS OF STANDARD NAND GATES



Typical and 95% Limit Input Characteristics (at 5 V and 0°C to 75°C)

Typical and 95% Limit Output Characteristics (at 5 V and 0°C to 75°C)



APPLICATION NOTES

Wired-Or Function

The purpose of the 5.5 V open collector devices is primarily to perform the 'wired-OR' function which can not be implemented by the standard active pull up output circuit. The open collector devices require an external resistor between output and V_{CC}. The choice of resistor value is a compromise between fan out requirements, the number of commoned outputs, power dissipation and speed. Limiting values of R_X are given by the following inequalities.

$$R_X > \frac{V_{CC}(\text{max.}) - V_{OL}(\text{max.})}{(10-N)\, I_F}$$

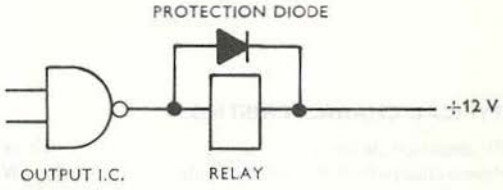
$$R_X < \frac{V_{CC}(\text{min.}) - V_{OH}(\text{min.})}{M.I_{CEX} + N.I_R}$$

Where M=Number of outputs commoned together in the 'Wired-OR' function; N=Fan out required.

High Voltage Output

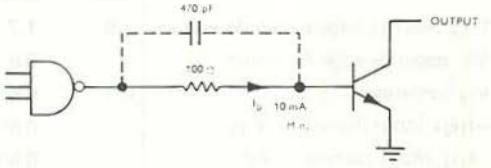
A typical use of the high voltage open collector device:

Miniature relay drives – A protection diode is required to prevent turn off transients damaging the output transistor (as shown).



Output Interfacing

When interfacing between TTL logic and lamps, relays etc. a discrete driving transistor is normally used. If there are several such interface transistors being driven from one multiple gate TTL device a problem is encountered in determining the value of base resistor to be used, to ensure maximum base drive without risk of over dissipating the ICC, when all outputs are high. The circuit shown below is suitable for use with the ITT devices and gives minimum base current of 10 mA.



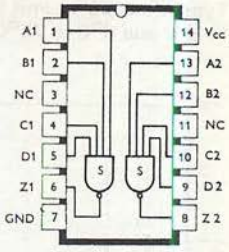
Standard 74 Series Gate

The inclusion of the 470 pF capacitor will give a considerable improvement in speed of this circuit. If the transistor used is a 2N2369A propagation delay times from the gate inputs to output of 10ns can be achieved.

ITT7413
DUAL 4-INPUT POSITIVE NAND SCHMITT TRIGGER

- **Temperature compensated thresholds**
- **Hysterisis 0.8 V**
- **Fan out=10, low state**
- **Fan out-20, high state**
- **Operates from signal with slow rise and fall times**
- **Pulse shaper**

Pin configuration (top view)



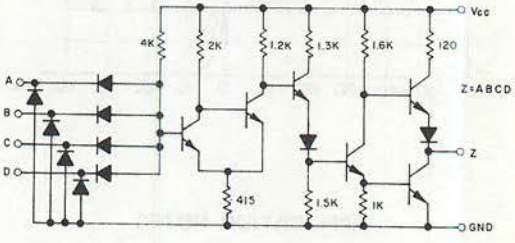
ITT7413

TYPICAL CHARACTERISTICS

Propagation delay	17 ns
Power dissipation (50% duty cycle)	85 mW
Input loading factor	1 unit load
Fan out	1 to 10 unit loads, low state 1 to 20 unit loads, high state
Positive threshold	1.7 V
Negative threshold	0.9 V

Circuit diagram of one gate

Resistance values in ohms



D.C. CHARACTERISTICS

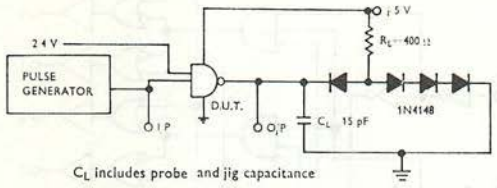
PARAMETER	LIMIT				CONDITIONS	
	Min.	Typ. at 25°C	Max.	Units	V_{CC}	
V_{T+} positive edge threshold voltage	1.5	1.7		V	5.0V	V_{OL} ⟨ 0.4V
V_{T-} negative edge threshold		0.9	1.1	V	5.0V	V_{OH} ⟩ 2.4V
V_H hysteresis	0.4	0.8		V	5.0V	
$-I_{IN+}$ input current at V_{T+}		0.65		mA	5.0V	$V_{IN}=V_{T+}$
$-I_{IN-}$ input current at V_{T-}		0.85		mA	5.0V	$V_{IN}=V_{T-}$
I_{CCH}		20	36	mA	Max.	V_{IN} on all inputs 5.0V
I_{CCL}		14	28	mA	Max.	V_{IN} on all inputs 0V

Information on the absolute maximum ratings and the other D.C. characteristics of this device (which are common to other integrated circuits in this series) is stated in the general information section.

SWITCHING CHARACTERISTICS V_{CC}=5.0 V, T_{AMB}=25°C

PARAMETER	LIMIT				CONDITIONS
	Min.	Typ.	Max.	Unit	
t_{pd+}		18	35	ns	See test circuit
t_{pd-}		15	30	ns	See test circuit

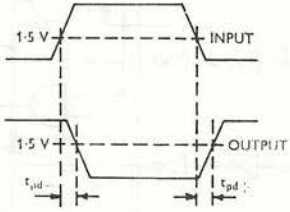
Switching test circuit



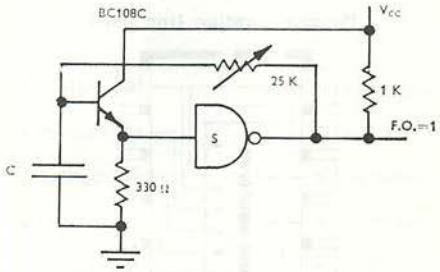
C_L includes probe and jig capacitance

Pulse Characteristics
t_r = 10 ns
t_p = 4 ns
f_o = 500 ns
P.R.F. = 1 MHz
Z_o = 50 Ω
Amplitude - 3.5 V

Waveforms



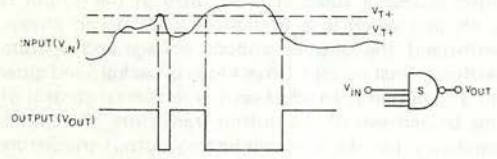
An alternative circuit is also illustrated which avoids the use of such large and expensive capacitors to achieve low frequencies. It also has the advantage of easy adjustment. Typical values of C for 1 Hz with transistor current gain of 200 is 40 μF.



APPLICATION NOTES

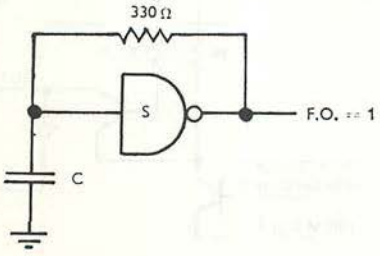
Pulse Shaper

Any input signal with slowly changing voltages will be unambiguously shaped by the ITT7413 due to its schmitt input.



Multivibrator

The circuit shown will have operated as a self starting multivibrator having frequency range of 1 Hz to 10 MHz. Typical values of C are 2,000 μF for 1 Hz and 200 pF for 10 MHz. Mark space ratio 1:3.

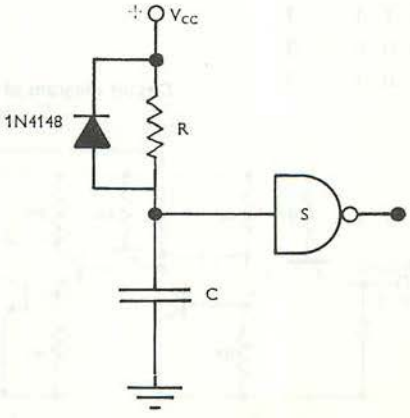


Supply Switch on Reset Driver

It is often required that I.C. logic systems should be reset to a known state on switch on of supply voltage. This function is automatically provided by the circuit shown. The output pulse is given approximately by the relation

$$t = 0.4\ C \left(\frac{4R \times 10^3}{R + 4 \times 10^3} \right)$$

This time constant should be designed to be longer than the start up time of the V_{CC} power supply. The diode is provided to ensure fast discharge of C.



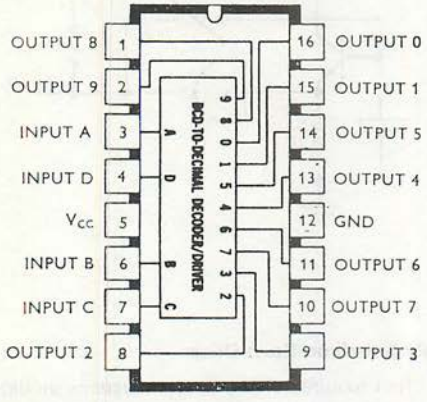
ITT7441A
BCD TO DECIMAL DECODER/ DRIVER

- **For driving gas-filled cold cathode indicator tubes**

TYPICAL CHARACTERISTICS

Power dissipation	140 mW
Input loading factor	1 unit load
Output load	≤7 mA
Output voltage	85 V

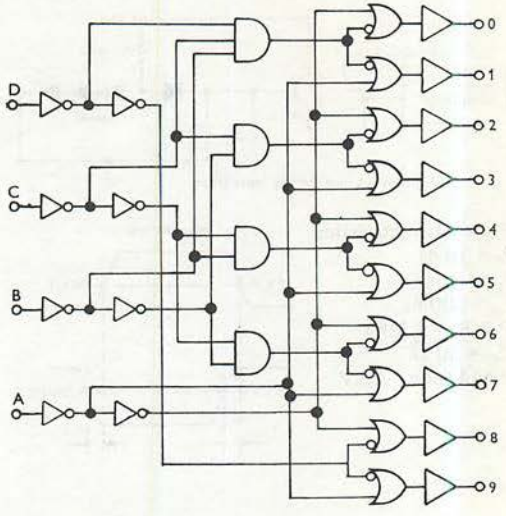
Pin configuration (top view)



Truth Table

D	C	B	A	O/P	OVER RANGE				
0	0	0	0	0	1	0	1	0	2&8
0	0	0	1	1	1	0	1	1	3&9
0	0	1	0	2	1	1	0	0	4&8
0	0	1	1	3	1	1	0	1	5&9
0	1	0	0	4	1	1	1	0	6&9
0	1	0	1	5	1	1	1	1	7&9
0	1	1	0	6					
0	1	1	1	7					
1	0	0	0	8					
1	0	0	1	9					

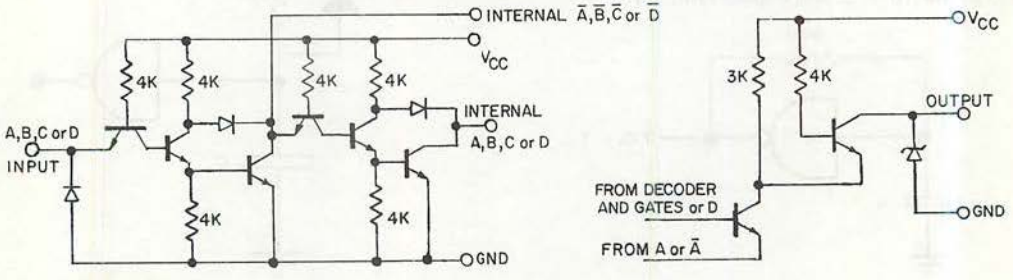
Logic diagram



DESCRIPTION

The input circuitry of the ITT7441A consists of eight inverters which are used to produce true and complement logic levels of the input signals which are suitable for internal use. The decoding from BCD is achieved by four AND gates and ten NOR gates. The output drivers are designed to drive gas-filled indicator tubes. The circuitry of the output is such that when it is in the off state it can always withstand the unused cathode voltage and operate with minimal current (thus keeping background glow to a minimum). In addition due to special control of the breakdown of the output transistors, there is no tendency for the non conducting output transistors to oscillate.

Circuit diagram of typical input and output circuits
Resistance values in ohms

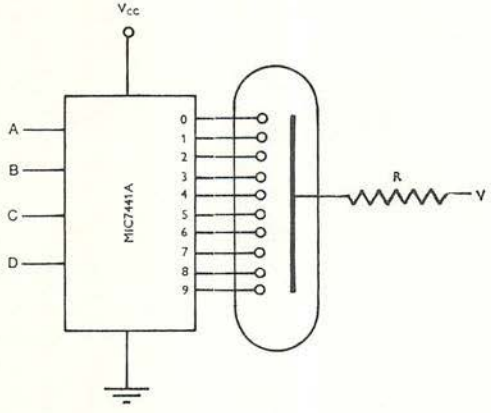


PARAMETER	LIMIT				CONDITIONS
	Min.	Typ.at 25°C	Max.	Units	V_{CC}
$V_{OH(M)}$	70	85		V	Max. I_{OH}=2 mA
I_{CEX}			50	μA	Max. V_{CEX}=55V
V_{OL}			2.4	V	Min. I_{OL}=7 mA
I_{CC}		21	42	mA	Max.

Information on the absolute maximum ratings and the other DC characteristics of this device (which are common to other integrated circuits in this series) is stated in the general information section.

NUMERICAL INDICATOR TUBE DRIVING

The circuit illustrates typical connection of ITT-7441A to a numerical indicator tube.



R and V are selected from tube manufacturers data. The ground connection must be of low impedance.

The ITT7441A ensures that the prebias voltage does not fall below 70 volts. A numerical indicator tube must be chosen such that the prebias current does not exceed 2 mA at a prebias voltage of 70 volts.

APPLICATION NOTE

Decoding

It is not generally realized that decoders designed as BCD to decimal decoders can be used with non-standard input and output connections. This allows the user greater flexibility on board layout for BCD, and ability to decode other codes.
The charts below show some possible input and output connections for the following codes:
BCD, Excess three Gray, Gray, Biquinary and 2421. Also shown is the truth table for each code. The box represents the decoder with standard connections marked. To the left of the box are shown the variations of input connections and to the right the variations of output connections.

BCD

Input a	Input b			Output a	Output b	D	C	B	A	Dec
			0	0	0	0	0	0	0	0
			1	1	1	0	0	0	1	1
A	A	A	2	2	4	0	0	1	0	2
			3	3	5	0	0	1	1	3
B	C	B	4	4	2	0	1	0	0	4
			5	5	3	0	1	0	1	5
C	B	C	6	6	6	0	1	1	0	6
			7	7	7	0	1	1	1	7
D	D	D	8	8	8	1	0	0	0	8
			9	9	0	1	0	0	1	9

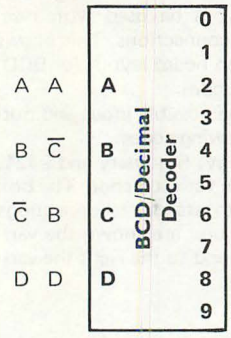
BCD/Decimal Decoder

Excess Three Gray

Input a	Input b			Output a	Output b	D	C	B	A	Dec
			0	1	1	0	0	1	0	0
			1	8	8	0	1	1	0	1
D	D	A	2	2	4	0	1	1	1	2
			3	7	5	0	1	0	1	3
A	$\overline{B}$	B	4	4	2	0	1	0	0	4
			5	5	7	1	1	0	0	5
$\overline{B}$	A	C	6	3	3	1	1	0	1	6
			7	6	6	1	1	1	1	7
$\overline{C}$	$\overline{C}$	D	8	0	0	1	1	1	0	8
			9	9	9	1	0	1	0	9

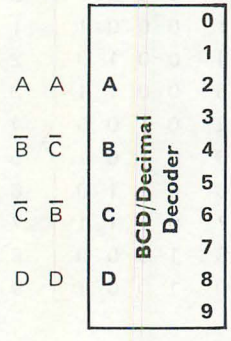
BCD/Decimal Decoder

Gray



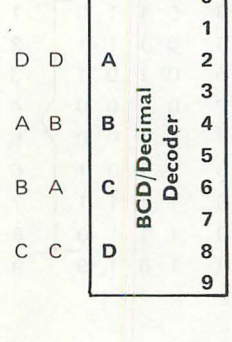
Output a	Output b	D	C	B	A	Dec
7	7	0	0	0	0	0
6	6	0	0	0	1	1
4	0	0	0	1	1	2
5	1	0	0	1	0	3
0	4	0	1	1	0	4
1	5	0	1	1	1	5
3	3	0	1	0	1	6
2	2	0	1	0	0	7
8	8	1	1	0	0	8
9	9	1	1	0	1	9

2421



Output a	Output b	D	C	B	A	Dec
6	6	0	0	0	0	0
7	7	0	0	0	1	1
4	2	0	0	1	0	2
5	3	0	0	1	1	3
2	4	0	1	0	0	4
3	5	0	1	0	1	5
0	0	0	1	1	0	6
1	1	0	1	1	1	7
8	8	1	1	1	0	8
9	9	1	1	1	1	9

Biquinary



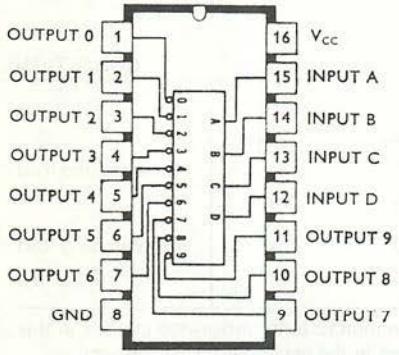
Output a	Output b	D	C	B	A	Dec
0	0	0	0	0	0	0
5	5	0	0	0	1	1
1	2	0	0	1	0	2
6	7	0	0	1	1	3
2	1	0	1	0	0	4
7	6	1	0	0	0	5
3	3	1	0	0	1	6
8	8	1	0	1	0	7
4	4	1	0	1	1	8
9	9	1	1	0	0	9

- **2421 Decoder**
- **Biquinary Decoder**
- **3 line to 8 line decoder with strobe**
- **Recognition of invalid input codes**

TYPICAL CHARACTERISTICS

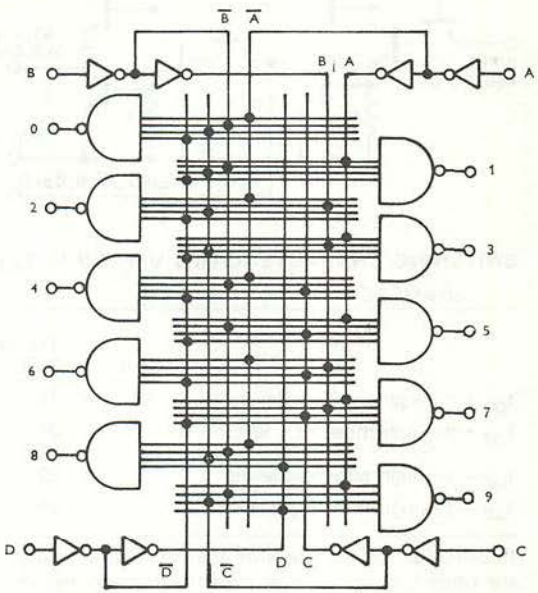
Propagation delay	25 ns
Power dissipation	140 mW
Input loading factor	1 unit load
Fan out	1 to 10 unit loads

Pin configuration (top view)



Logic Diagram

Connections are shown for the ITT7442. The matrix connections are different for the ITT7443 and the ITT7444 and they can be determined from the truth table.

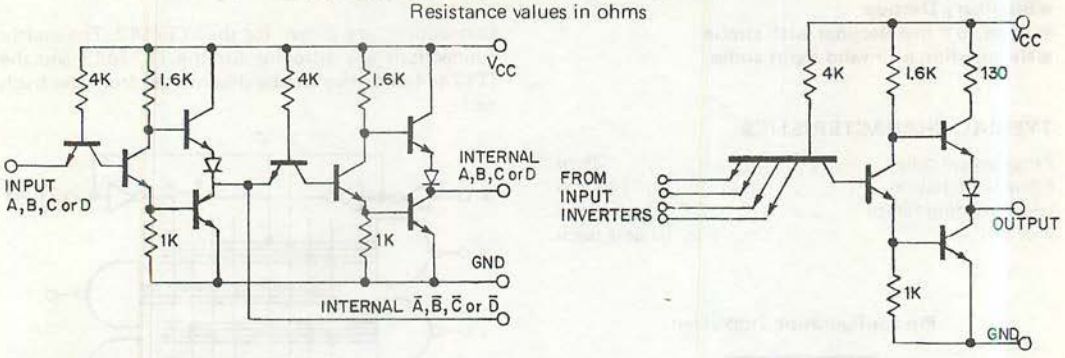


Truth Table

	BCD Input				Excess 3 Input				Excess 3 Gray Input				Decimal Output									
Dec.	D	C	B	A	D	C	B	A	D	C	B	A	0	1	2	3	4	5	6	7	8	9
0	0	0	0	0	0	0	1	1	0	0	1	0	0	1	1	1	1	1	1	1	1	1
1	0	0	0	1	0	1	0	0	0	1	1	0	1	0	1	1	1	1	1	1	1	1
2	0	0	1	0	0	1	0	1	0	1	1	1	1	1	0	1	1	1	1	1	1	1
3	0	0	1	1	0	1	1	0	0	1	0	1	1	1	1	0	1	1	1	1	1	1
4	0	1	0	0	0	1	1	1	0	1	0	0	1	1	1	1	0	1	1	1	1	1
5	0	1	0	1	1	0	0	0	1	1	0	0	1	1	1	1	1	0	1	1	1	1
6	0	1	1	0	1	0	0	1	1	1	0	1	1	1	1	1	1	1	0	1	1	1
7	0	1	1	1	1	0	1	0	1	1	1	1	1	1	1	1	1	1	1	0	1	1
8	1	0	0	0	1	0	1	1	1	1	1	0	1	1	1	1	1	1	1	1	0	1
9	1	0	0	1	1	1	0	0	1	0	1	0	1	1	1	1	1	1	1	1	1	0
Over Range Conditions																						
10	1	0	1	0	1	1	0	1	1	0	1	1	1	1	1	1	1	1	1	1	1	1
11	1	0	1	1	1	1	1	0	1	0	0	1	1	1	1	1	1	1	1	1	1	1
12	1	1	0	0	1	1	1	1	1	0	0	0	1	1	1	1	1	1	1	1	1	1
13	1	1	0	1	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1
14	1	1	1	0	0	0	0	1	0	0	0	1	1	1	1	1	1	1	1	1	1	1
15	1	1	1	1	0	0	1	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1

Circuit diagram of typical input and output circuits

Resistance values in ohms

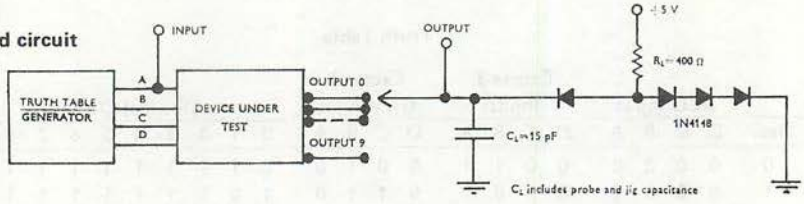


SWITCHING CHARACTERISTICS V_{CC}=5.0 V, T_{AMB}=25°C

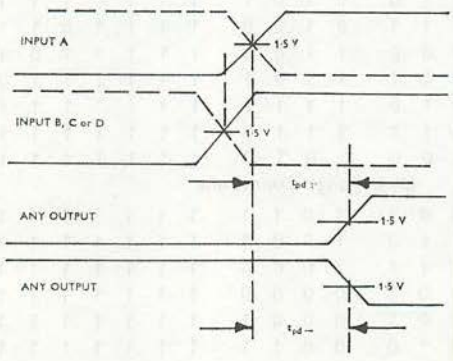
PARAMETER	LIMIT				CONDITIONS
	Min.	Typ.at 25°C	Max.	Units	
t_{pd} + through two logic levels	10	17	25	ns	Use switching load circuit
t_{pd} + through three logic levels		26	35	ns	
t_{pd} – through two logic levels	10	22	30	ns	Use switching load circuit
t_{pd} – through three logic levels		26	35	ns	

Information on the absolute maximum ratings and the other D.C. characteristics of these devices (which are common to other integrated circuits in this series) is stated in the general information section.

Switching load circuit



Waveforms



Truth Table

Generator Characteristics
t_r = 10 ns
t_f = 4 ns
R.F. = 1 MHz
Amplitude = 3.5 V
Z_o = 50 Ω
Transitions on B, C, & D must occur before transition on A.

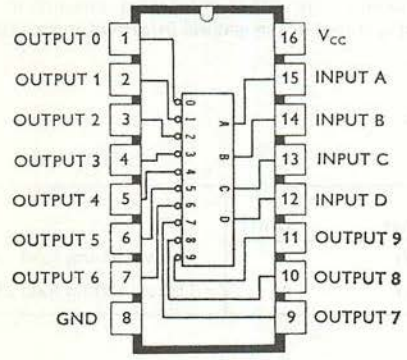
BCD TO DECIMAL DECODER/DRIVER

- **80 mA Output Sink-Current**
- **ITT7445 30 Volt Output**
- **ITT74145 15 Volt Output**
- **Recognition of Invalid Codes**
- **Decoder Excess Three Gray, Gray, Biquinary and**
- **Other Codes**

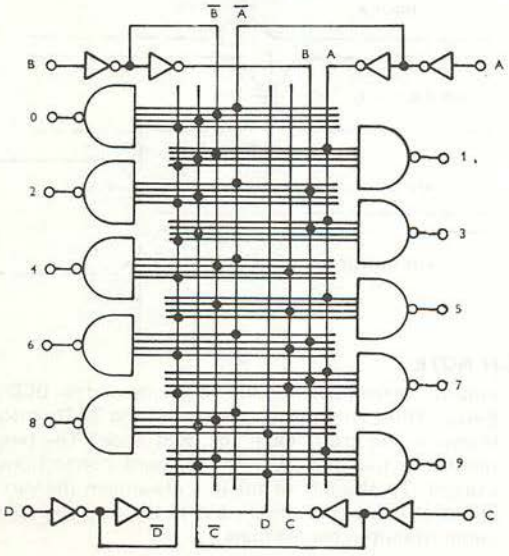
TYPICAL CHARACTERISTICS

Propagation delay . . . . . 35 ns
Power dissipation . . . . . 215 mW
Input loading factor . . . . . 1 unit load
Output voltage rating
ITT7445 . . . . . 30 V
ITT74145 . . . . . 15 V

Pin Configuration



Logic diagram



DESCRIPTION

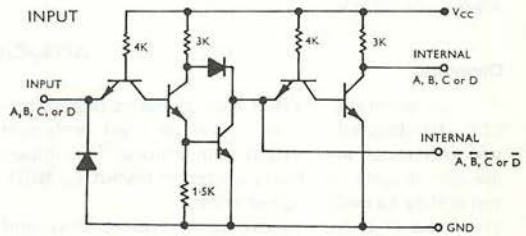
These decoders consist of eight inverters and ten output gates. Each pair of inverters are connected in series to provide true and complement signals of the four inputs. The ten output gates are of special design to enable them to have the high voltage rating and high current capability. These output gates each have four inputs which are used to provide full decoding so that invalid input states give no output.

Truth Table

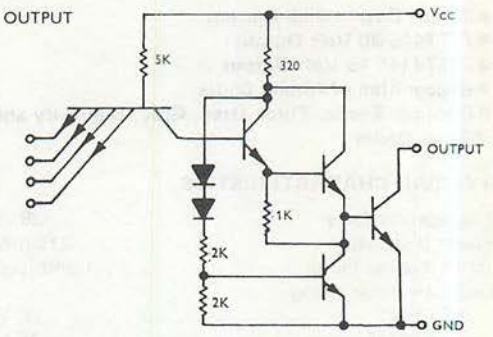
INPUTS				OUTPUTS									
D	C	B	A	0	1	2	3	4	5	6	7	8	9
0	0	0	0	0	1	1	1	1	1	1	1	1	1
0	0	0	1	1	0	1	1	1	1	1	1	1	1
0	0	1	0	1	1	0	1	1	1	1	1	1	1
0	0	1	1	1	1	1	0	1	1	1	1	1	1
0	1	0	0	1	1	1	1	0	1	1	1	1	1
0	1	0	1	1	1	1	1	1	0	1	1	1	1
0	1	1	0	1	1	1	1	1	1	0	1	1	1
0	1	1	1	1	1	1	1	1	1	1	0	1	1
1	0	0	0	1	1	1	1	1	1	1	1	0	1
1	0	0	1	1	1	1	1	1	1	1	1	1	0
OVER RANGE CONDITIONS													
1	0	1	0	1	1	1	1	1	1	1	1	1	1
1	0	1	1	1	1	1	1	1	1	1	1	1	1
1	1	0	0	1	1	1	1	1	1	1	1	1	1
1	1	0	1	1	1	1	1	1	1	1	1	1	1
1	1	1	0	1	1	1	1	1	1	1	1	1	1
1	1	1	1	1	1	1	1	1	1	1	1	1	1

Circuit diagram of typical input and output circuits

Resistance values in ohms



PARAMETER	LIMIT				CONDITIONS
	Min.	Typ.at 25°C	Max.	Units	V_{CC}
I_{CCH} supply current for highest dissipation state					
74 series	43		70	mA	Max. Any valid
54 series	43		62	mA	Max. input code
I_{CCL} supply current for lowest dissipation state					
74 series	31		53	mA	Max. Any invalid
54 series	31		45	mA	Max. input code

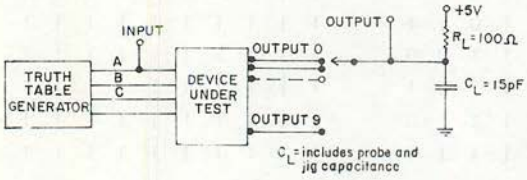


Information on the absolute maximum ratings and the other D.C. characteristics of this device (which are common to other integrated circuits in this series) is stated in the general information section.

SWITCHING CHARACTERISTICS V_{CC}=5.0 V, T_{AMB}=25°C

PARAMETER	LIMIT				CONDITIONS
	Min.	Typ.at 25°C	Max.	Units	
t_{pd}+ propagation delay to logical '1'			50	ns	Use switching load circuit
t_{pd}- propagation delay to logical '0'			50	ns	Use switching load circuit

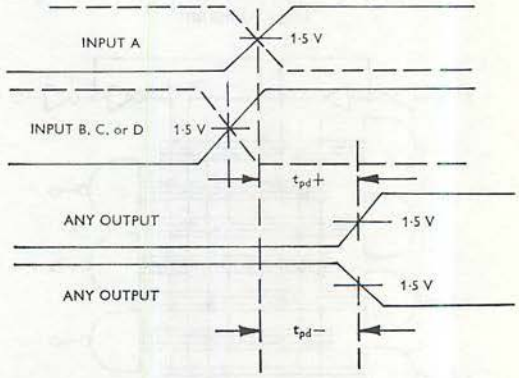
Switching load circuit



Truth Table
Generator Characteristics

t_r = 10 ns
t_f = 4 ns
R.F. = 1 MHz
Amplitude - 3.5 V
Z_O = 50 Ω
Transition on B, C or D must occur before transition on A.

Waveforms



APPLICATION NOTE

Decoding

It is not generally realised that decoders designed as BCD to decimal decoders can be used with non standard input and output connections. This allows the user greater flexibility on board layout for BCD, and ability to decode other codes.
The following charts show some possible input and output connections for the following codes: BCD, Excess Three Gray, Gray, Biquinary and 2421. Also shown is the truth table for each code. The box represents the decoder with standard connections marked. To the left of the box are shown the variations of input connections and to the right the variations of output connections.

BCD

Input a	Input b		Output a	Output b	D	C	B	A	Dec
		0	0	0	0	0	0	0	0
A	A	1	1	1	0	0	0	1	1
		2	2	4	0	0	1	0	2
B	C	3	3	5	0	0	1	1	3
		4	4	2	0	1	0	0	4
C	B	5	5	3	0	1	0	1	5
		6	6	6	0	1	1	0	6
D	D	7	7	7	0	1	1	1	7
		8	8	8	1	0	0	0	8
		9	9	9	1	0	0	1	9

BCD/Decimal Decoder — A, B, C, D

2421

Input a	Input b		Output a	Output b	D	C	B	A	Dec
		0	6	6	0	0	0	0	0
A	A	1	7	7	0	0	0	1	1
		2	4	2	0	0	1	0	2
$\overline{B}$	$\overline{C}$	3	5	3	0	0	1	1	3
		4	2	4	0	1	0	0	4
$\overline{C}$	$\overline{B}$	5	3	5	0	1	0	1	5
		6	0	0	0	1	1	0	6
D	D	7	1	1	0	1	1	1	7
		8	8	8	1	1	1	0	8
		9	9	9	1	1	1	1	9

BCD/Decimal Decoder — A, B, C, D

Excess Three Gray

Input a	Input b		Output a	Output b	D	C	B	A	Dec
		0	1	1	0	0	1	0	0
		1	8	8	0	1	1	0	1
D	D	2	2	4	0	1	1	1	2
		3	7	5	0	1	0	1	3
A	$\overline{B}$	4	4	2	0	1	0	0	4
		5	5	7	1	1	0	0	5
$\overline{B}$	A	6	3	3	1	1	0	1	6
		7	6	6	1	1	1	1	7
$\overline{C}$	$\overline{C}$	8	0	0	1	1	1	0	8
		9	9	9	1	0	1	0	9

BCD/Decimal Decoder — A, B, C, D

Biquinary

Input a	Input b		Output a	Output b	D	C	B	A	Dec
		0	0	0	0	0	0		0
		1	5	5	0	0	0	1	1
D	D	2	1	2	0	0	1	0	2
		3	6	7	0	0	1	1	3
A	B	4	2	1	0	1	0	0	4
		5	7	6	1	0	0	0	5
B	A	6	3	3	1	0	0	1	6
		7	8	8	1	0	1	0	7
C	C	8	4	4	1	0	1	1	8
		9	9	9	1	1	0	0	9

BCD/Decimal Decoder — A, B, C, D

Gray

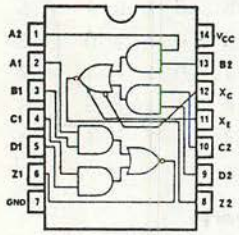
Input a	Input b		Output a	Output b	D	C	B	A	Dec
		0	7	7	0	0	0	0	0
		1	6	6	0	0	0	1	1
A	A	2	4	0	0	0	1	1	2
		3	5	1	0	0	1	0	3
B	$\overline{C}$	4	0	4	0	1	1	0	4
		5	1	5	0	1	1	1	5
$\overline{C}$	B	6	3	3	0	1	0	1	6
		7	2	2	0	1	0	0	7
D	D	8	8	8	1	1	0	0	8
		9	9	9	1	1	0	1	9

BCD/Decimal Decoder — A, B, C, D

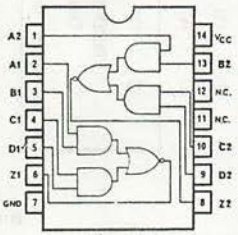
TYPICAL CHARACTERISTICS

Propagation delay . . . . . 9 ns
Power dissipation . . . . . 29 mW (7450, 7451)
(50% duty cycle) . . . . . 23 mW (7453, 7454)
Input loading factor . . . . . 1 unit load
Fan-out . . . . . 1 to 10 unit loads

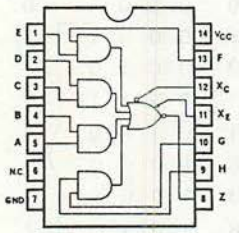
Pin configuration (top views)



ITT7450

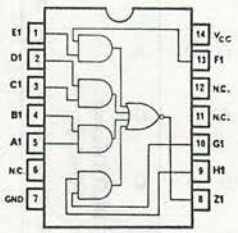


ITT7451



ITT7453

Make no external connection to pins 11 and 12

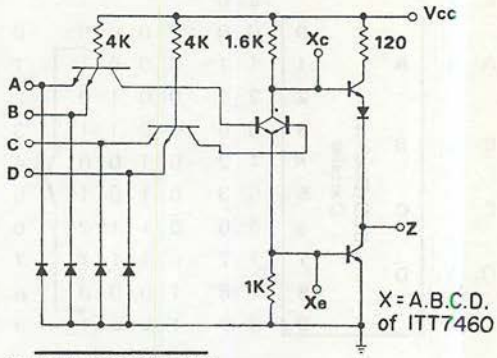


ITT7454

If expander is not used leave pins 11 and 12 open

Circuit diagram of one gate (ITT7450 and ITT7451)

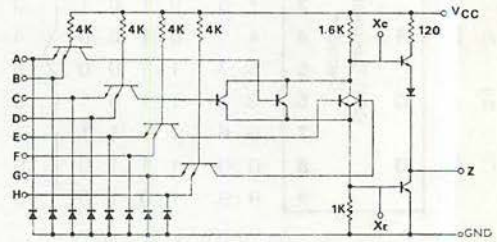
Resistance values in ohms



$Z=\overline{(A.B)+(C.D)+(X)}$

The ITT7451 and ITT7454 do not have the expanding inputs X_E and X_C

Circuit diagram of ITT7453 and ITT7454



$Z=(A.B)+(C.D)+(E.F)+(G.H)+(X)$
where X = A.B.C.D. of ITT7460

PARAMETER	LIMIT				CONDITIONS	
	Min.	Type at 25°C	Max.	Units	V_{CC}	
I_{CCH}						
ITT7450, ITT7451		7.4	14	mA	Max.	V_{IN} on all inputs
ITT7453, ITT7454		5.1	9.5	mA	Max.	5.0 V
I_{CCL}		4.0	8.0	mA	Max.	V_{IN} on all inputs 0V

Information on the absolute maximum ratings and the other D.C. characteristics of these devices (which are common to other integrated circuits in this series) is stated in the general information section.

D.C. CHARACTERISTICS OF ITT7450/3 EXPANDER INPUTS AT 0°C

PARAMETER	LIMIT				CONDITIONS	
	Min.	Type	Max.	Unit	V_{CC}	
I_X expander current			3.1	mA	Min.	V_{CE}=0.4V, I_{OL}=16mA (Note 1)
V_{BE} base emitter voltage of output transistor			1.0	V	Min.	I_{OL}=16mA, R_{CE}=0, I_E=260μA (Note 1)
V_{OH} output high voltage	2.4	3.3		V	Min.	I_{OH}=−400μA, I_E−270μA, I_C−270μA (Note 1)
V_{OL} output low voltage		0.22	0.4	V	Min.	I_{OL}=10mA, I_E=430μA, R_{CE}=130 (Note 1)

D.C. CHARACTERISTICS OF ITT5450/3 EXPANDER INPUTS AT −55°C

PARAMETER	LIMIT				CONDITIONS	
	Min.	Type	Max.	Unit	V_{CC}	
I_X expander current			2.9	mA	Min.	V_{CE}=0.4V, I_{OL}=16mA (Note 1)
V_{BE} base emitter voltage of output transistor			1.0	V	Min.	I_{OL}=16mA, R_{CE}=0, I_E=410μA (Note 1)
V_{OH} output high voltage	2.4	3.3		V	Min.	I_{OH}=−400μA, I_E=150μA, I_C=−150μA (Note 1)
V_{OL} output low voltage		0.22	0.4	V	Min.	I_{OL}=16mA, I_E=300μA, R_{CE}=138 (Note 1)

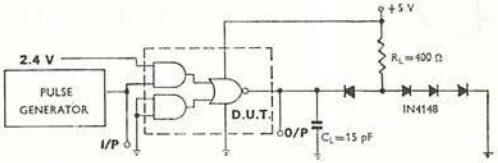
Note 1

V_{CE}, I_E, I_C and R_{CE} refer to voltage, current and resistance on X_E and X_C terminals.

SWITCHING CHARACTERISTICS V_{CC}=5.0 V, T_{AMB}=25°C

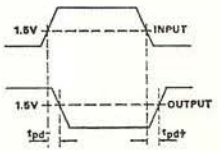
PARAMETER	LIMIT				CONDITIONS
	Min.	Type	Max.	Units	
t_{pd}^+		10	22	ns	See test circuits
t_{pd}^-		8	15	ns	See test circuits

Switching test circuit for ITT7450/1

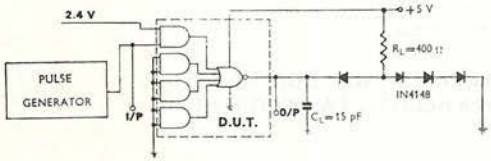


Pulse Characteristics
t_f = 10 ns
t_r = 4 ns
t_c = 500 ns
P.R.F. = 1 MHz
Z_o 50 Ω
Amplitude = 3.5 V

Waveforms



Switching test circuit for ITT7453/4

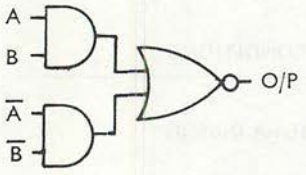


USE OF EXPANDER

The expander points are provided so that the input of the ITT7450 or the ITT7453 can be increased by a maximum of four 4-input NAND gates. Both X_C and X_E expander points must be used to connect to the X_C and X_E outputs of the ITT7460 expander.

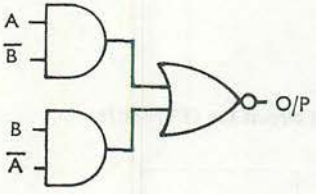
USE AS AN EXCLUSIVE OR GATE

The connections as an exclusive OR gate are shown below with inputs A and B.



A	B	O/P
0	0	0
1	0	1
0	1	1
1	1	0

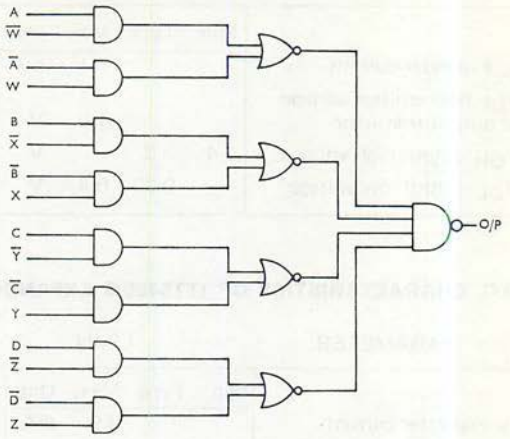
The inverse of exclusive OR function can also be obtained



A	B	O/P
0	0	1
1	0	0
0	1	0
1	1	1

ITT7450 and ITT7451 USED AS A COMPARATOR

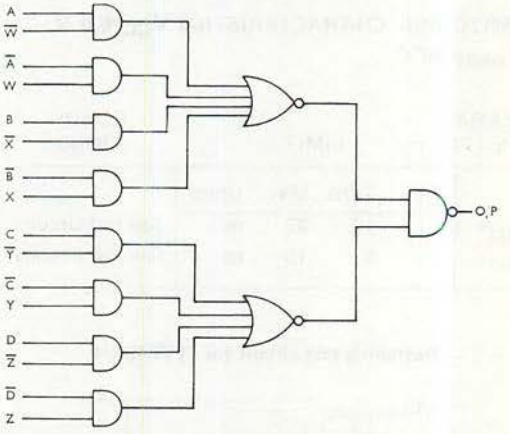
Two binary numbers ABCD and WXYZ.



When ABCD = WXYZ O/P = 0
when ABCD ⟩ or ⟨ WXYZ O/P = 1

ITT7453 and ITT7454 USED AS A COMPARATOR

Two binary numbers ABCD and WYXZ.



When ABCD - WXYZ O/P = 0
when ABCD ⟩ or ⟨ WXYZ O/P = 1

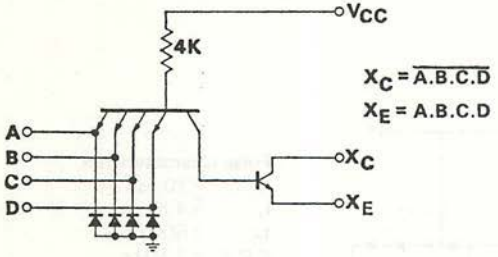
TYPICAL CHARACTERISTICS

Propagation delay . . . . . 13 ns
Power dissipation (50% duty cycle) . . . . . 8 mW
Input loading factor . . . . . 1 unit load

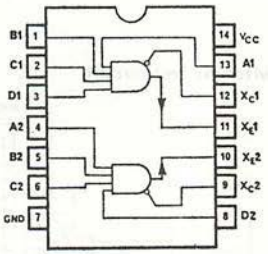
The ITT7460 expander is intended for use with the ITT7450 or 53 AND-OR-INVERT gates. Not more than four expander gates (two packages) should be connected to any AND-OR-INVERT gate. The X_C and X_E outputs of the expander should be connected respectively to X_C and X_F expander inputs of the AND-OR-INVERT gates. Inter-connecting leads should be kept as short as possible.

Circuit diagram of one expander

Resistance values in ohms



Pin configuration



PARAMETER	LIMIT				CONDITIONS	
	Min.	Type at 25°C	Max.	Units	V_{CC}	
V_{ON} on state voltage			0.4	V	Min.	V_E=1V, V_{IH}=2.0V, $R_{C/VCC}$=1.1K, T_{AMB}=Min.
I_{OFF} off-state output current—7460			270	µA	Min.	V_C=v.5V, V_{IL}=0.8V
5460			150	µA	Ma	$R_{E/GND}$=1.2K, T_{AMB}=Min.
I_{ON} on-state output current—7460	–300			µA	Max.	V_{IH}=2.0V, V_E=1.0V
5460	–430			µA		T_{AMB}=Min.
$-I_F$ input forward current		1.0	1.6	mA	Max.	V_F=0.4V
I_R input reverse current			40	µA	Max.	V_R=2.4V
			1.0	mA	Max.	V_R=5.5V

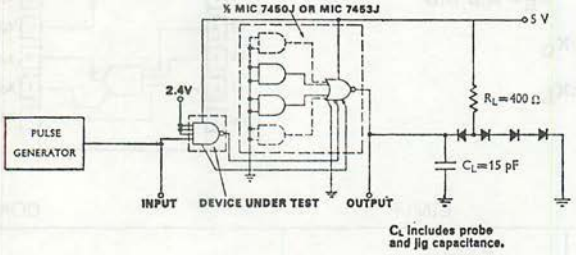
INPUT EXPANDER

PARAMETER	LIMIT				CONDITIONS	
	Min.	Type	Max.	Units	V_{CC}	
I_{CCH} supply current for highest dissipation (off state)		2	4	mA	Max.	V_{IN} on all inputs OV, V_E=0.85V
I_{CCL} supply current for lowest dissipation (on state)		1.2	2.5	mA	Max.	V_{IN} on all inputs 5.0V, V_E=-.85V

Information on the absolute maximum ratings and the other D.C. characteristics of this device (which are common to other integrated circuits in this series) is stated in the general information section.

PARAMETER	LIMIT				CONDITIONS
	Min.	Type	Max.	Units	
t_{pd}+propagation delay to logical '1' (through ITT7450 or ITT7453)		15	30	ns	See test circuits
t_{pd} - propagation delay to logical '0' (through ITT7450 or ITT7453)		10	20	ns	See test circuit

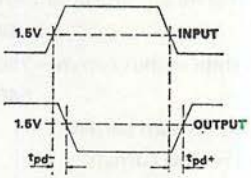
Switching test circuit



Pulse Characteristics

t_f = 10 ns
t_r = 4 ns
t_p = 500 ns
P.R.F. = 1 MHz
Z_o = 50 Ω
Amplitude = 3.5 V

Waveforms



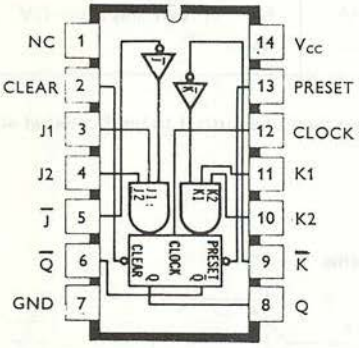
TYPICAL CHARACTERISTICS

Maximum clock frequency	35 MHz
Propagation delay	22 ns
Power dissipation	75 mW
Input loading factor	
Clock and any J or K input	1 unit load
Preset and clear	2 unit loads
Fan out	1 to 10 unit loads
Clock pulse transition time to logical '1'	5 ns to 150 ns
Clock pulse width t_{cp}	20 ns
Preset and clear pulse width t_p	25 ns

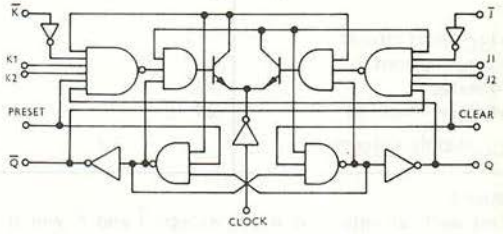
Truth Table

SYNCHRONOUS				ASYNCHRONOUS			
t_n			t_n+1	Preset	Clear	Q	$\bar{Q}$
J	K	Q	Q				
0	0	No change		0	0	0	0
1	0	1	0	1	0	0	1
0	1	0	1	0	1	1	0
1	1	Complement		1	1	No control	

Pin configuration



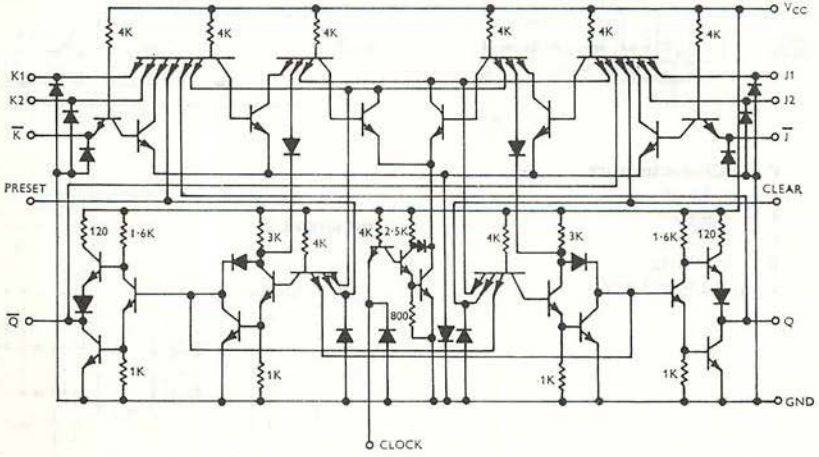
Logic diagram



DESCRIPTION

This device features twin J and K inputs, single $\bar{J}$ and $\bar{K}$ inputs, asynchronous preset and clear inputs and positive edge triggered clock input. At the threshold voltage, on the positive transition of the clock, input information is transferred to the outputs. Above or below the threshold the J and K inputs are disabled. The asynchronous inputs will operate the device only with clock low. The truth table shows the modes of operation.

Circuit diagram (Resistance values in ohms)

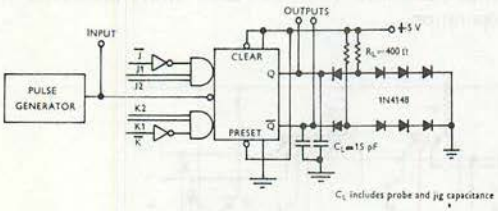


PARAMETER	LIMIT				CONDITIONS
	Min.	Typ. at 25°C	Max.	Units	V_{CC}
$-I_F$ input forward current.					
All J & K inputs and clock		1.0	1.6	mA	Max. V_F=0.4V
Preset and clear		2.0	3.2	mA	Max. Note 1
I_R input reverse current.					
All J & K inputs and clock			40	μA	Max. V_R=2.4V
Preset and clear			80	μA	Max. All other inputs at OV except $\overline{J}$ and $\overline{K}$ which are at 4.5 V
I_R All inputs			1	mA	Max. V_R=5.5V All other inputs at OV except $\overline{J}$ and $\overline{K}$ which are at 4.5V
$-I_{SC}$ short circuit output current					
74 series	18		57	mA	Max. V_{OUT}=OV
54 series (Note 2)	20		57	mA	Max. Preset and clear=OV
I_{CC} supply current		13	26	mA	Max.

Note 1
Test with all inputs at 4.5 V except $\overline{J}$ and $\overline{K}$ which are at OV. When testing J and K inputs all other inputs, to the appropriate input AND gate must be at logical '1'.

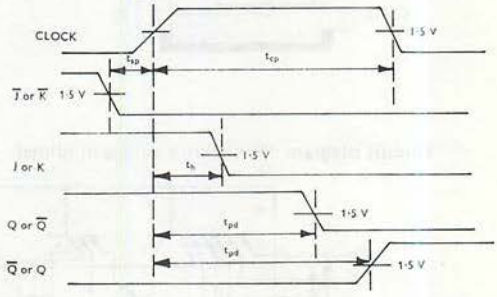
Note 2
Not more than one output to be shorted at any time.

Test circuit 1

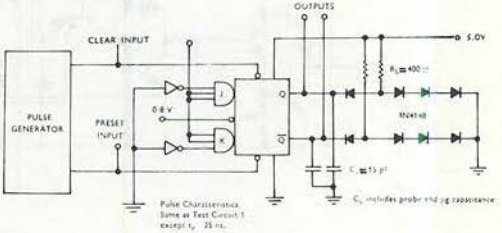


Pulse Characteristics
t_r = 10 ns
t_f = 4 ns
t_{cp} = 20 ns
R.F. = 1 MHz
Amplitude = 3.5 V

Waveforms



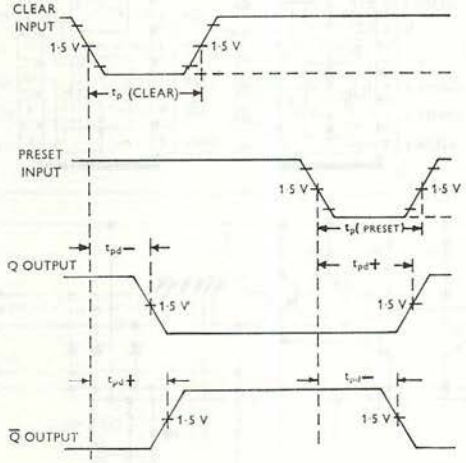
Test circuit 2



SWITCHING CHARACTERISTICS V_{CC}=5.0V, T_{AMB}=25°C

PARAMETER	LIMIT				CONDITIONS
	Min.	Typ.	Max.	Unit	
f_{max} maximum input clock frequency	20	35		MHz	Use test circuit 1. $\overline{J}$ and $\overline{K}$ at OV J1, K1, J2 and K2 at 2.4 V
t_{sp} minimum input set up time at $\overline{J}$ and $\overline{K}$		10	20	ns	Use test circuit 1. $\overline{J}$ or $\overline{K}$ at OV J1, J2, K1 and K2 at 2.4 V
t_h minimum input hold time at J1, J2, K1, K2		0	5	ns	Use test circuit 1. $\overline{J}$ and $\overline{K}$ at OV K1 and K2 or J1 and J2 at 2.4 V
t_{pd}+ propagation delay time to logical '1'					Clock at 0.8 V, $\overline{J}$ and $\overline{K}$ at OV
Clear or preset to output			50	ns	J and K at 2.4 V. Use test circuit 2.
Clock to output	10	27	50	ns	Use test circuit 1. $\overline{J}$ and $\overline{K}$ at OV, J and K as truth table
t_{pd}- propagation delay time to logical '0'					Clock at 0.8 V. $\overline{J}$ and $\overline{K}$ at OV.
Clear or preset to output			50	ns	J and K at 2.4 V. Use test circuit 2.
Clock to output	10	18	50	ns	Use test circuit 1. J and K at OV, J and K as truth table

Waveforms



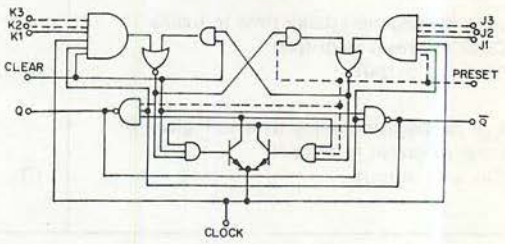
TYPICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

Maximum clock frequency	20 MHz
Propagation delay	20 ns
Power dissipation:	
Single type	50 mW
Dual type	100 mW
Input loading factor:	
J and K inputs	1 unit load
Direct and clock inputs	2 unit loads
Fan-out	1 to 10 unit loads
Clock pulse width t_{cp}	20 ns
Preset and clear pulse width t_p	25 ns
Input set up time t_{sp}	t_{cp}
Input hold time t_h	0 ns

Truth Table

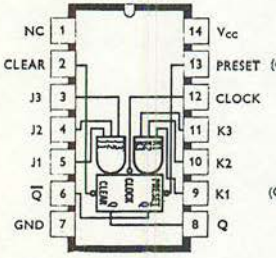
SYNCHRONOUS				ASYNCHRONOUS			
t_n		t_n+1		Preset	Clear	Q	$\overline{Q}$
J	K	Q	$\overline{Q}$	0	0	1	1
0	0	No change		1	0	0	1
1	0	1	0	0	1	1	0
0	1	0	1	1	1	No control	
1	1	Complement					

Logic diagram

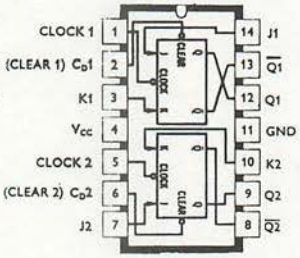


Pin configurations

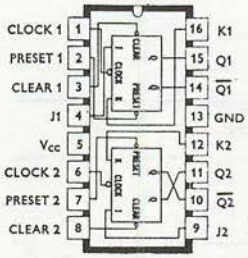
ITT7472



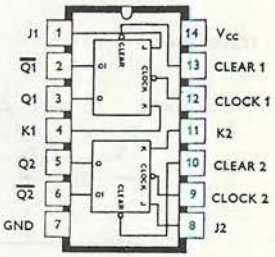
ITT7473



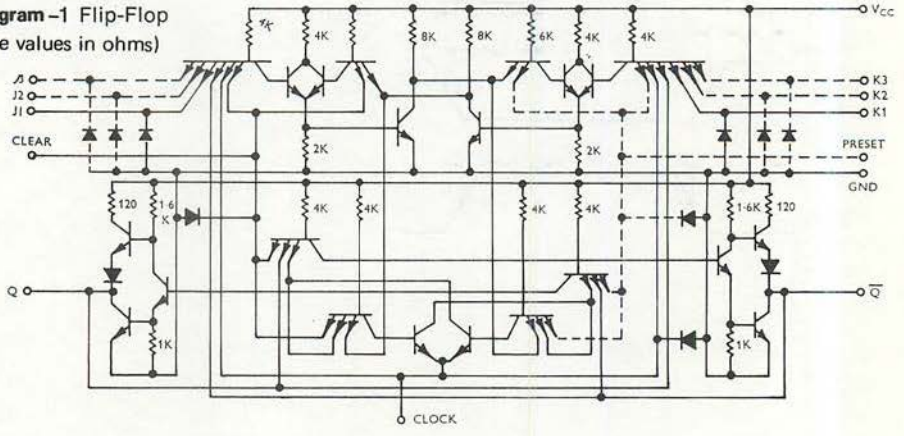
ITT7476



ITT74107



Circuit diagram –1 Flip-Flop
(Resistance values in ohms)



DESCRIPTION

These devices consist of gated Master and slave bistables. The ITT7472 with preset, clear and triple J and K inputs. The ITT7473 and ITT74107 with clear and single J and K inputs. The ITT7476 with preset, clear and single J and K inputs. The direct inputs will operate the device irrespective of the state of clock J or K inputs. The clock input operates as follows, on a positive going transition first the slave bistable is isolated from the master, then information is transferred from the J and K inputs to the master bistable. On a negative going transition first the J and K inputs are disabled then the information is transferred to the slave bistable. Operation will be according to the truth table if J and K information is present before and during the period that the clock is high. Because of the internal feedback from the Q and $\overline{Q}$ outputs to the J and K input AND gates one or other of the gates will have a logical '0' on one internal input. The external inputs cannot affect that gate. The other input AND gate will have a logical '1' on its internal input, if one of the external inputs goes to a logical '1' at any time while the clock is high the master bistable will change state and the Q and $\overline{Q}$ outputs will follow on the negative transition of the clock.

PARAMETER	LIMIT				CONDITIONS	
	Min.	Type at 25°C	Max.	Units	V_{CC}	
$-I_F$ input forward current						
All J and K inputs		1.0	1.6	mA	Max.	V_F=0.4V
Preset, clear and clock		2.0	3.2	mA	Max.	(Note 1)
I_{CC} supply current						
Single type		10	20	mA	Max.	
All dual types		20	40	mA		

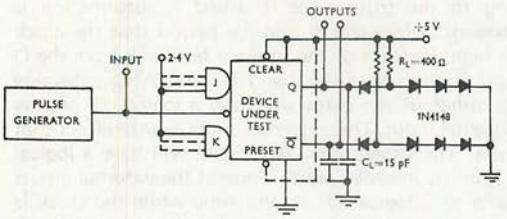
Note 1
Test with all other inputs at 4.5 V. Use preset or clear to set device to appropriate logic state. Clock to be tested for both logic states. When testing J or K inputs all other inputs including internal inputs to the appropriate input AND gate must be at logical '1'.

Information on the absolute maximum ratings and the other D.C. characteristics of this device (which are common to other integrated circuits in this series) is stated in the general information section.

SWITCHING CHARACTERISTICS V_{CC}=5.0V, T_{AMB}=25°C

PARAMETER	LIMIT				CONDITIONS
	Min.	Type	Max.	Units	
f_{max} maximum input clock frequency	15	20		MHz	Use test circuit 1
t_{pd}+ propagation delay time to logical '1'					
Clear or preset to output		16	25	ns	Use test circuit 2
Clock to output	10	16	25	ns	Use test circuit 1
t_{pd}- propagation delay time to logical '0'					
Clear or preset to output		25	40	ns	Use test circuit 2
Clock to output	10	25	40	ns	Use test circuit 1

Test Circuit 1

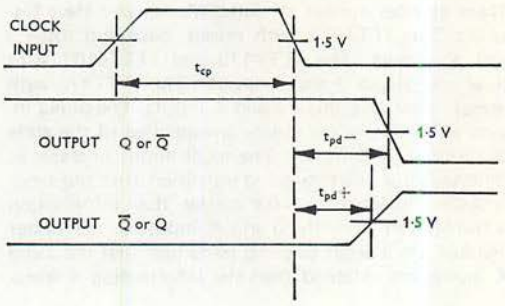


C_L includes probe and jig capacitance

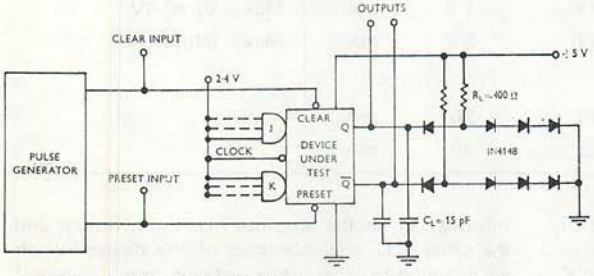
Pulse Characteristics

t_r = 10 ns
t_f = 4 ns
t_{cp} = 20 ns
R.F. = 1 MHz
Amplitude = 3.5 V

Waveforms



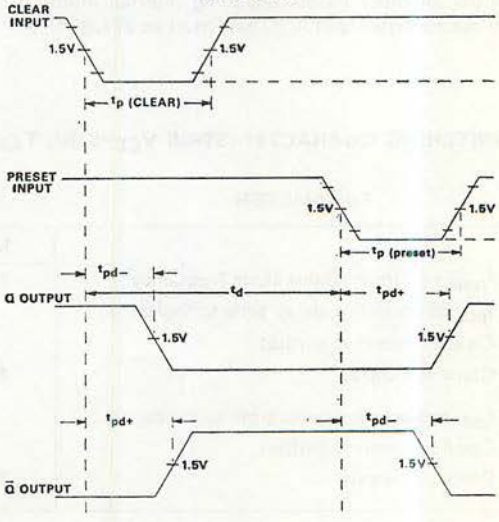
Test circuit 2)



C_L includes probe and jig capacitance

Pulse Characteristics
Same as Test Circuit 1, except t_p = 25 ns.

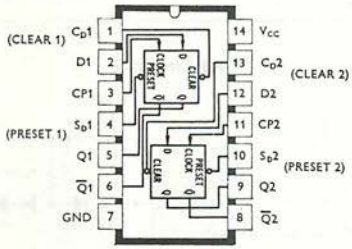
Waveforms



TYPICAL CHARACTERISTICS AND OPERATING CONDITIONS

Maximum clock frequency . . . . . 25 MHz
Propagation delay . . . . . 17 ns
Power dissipation . . . . . 85 mW
Input loading factor:
Preset or data . . . . . 1 unit load
Clear or clock . . . . . 2 unit loads
Fan out . . . . . 1 to 10 unit loads
Clock pulse width t_{cp} . . . . . 30 ns min.
Preset or clear pulse width t_p . . . . . 30 ns min.

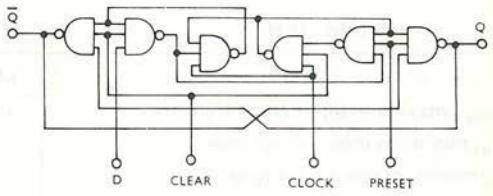
Pin configuration
(top view)



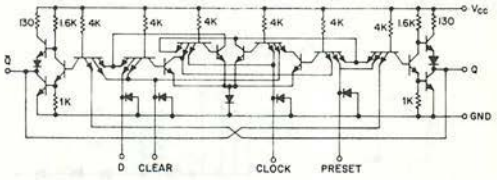
Truth Table

SYNCHRONOUS			ASYNCHRONOUS			
t_n	t_n+1		Preset	Clear	Q	$\overline{Q}$
D Input	Q	$\overline{Q}$	0	0	1	1
0	0	1	1	0	0	1
1	1	0	0	1	1	0
			1	1	No Control	

Logic diagram



Circuit diagram of one flip-flop
Resistance values in ohms



DESCRIPTION

The ITT7474 is an edge triggered D type flip-flop in which the transfer of the D input data takes place during the positive transition of the clock input. When the clock input is above or below the transfer threshold the 'D' input is inhibited. The transfer threshold is not directly related to the transition time of the positive going edge. Preset and clear inputs operate irrespective of the logic state of the clock or D input.

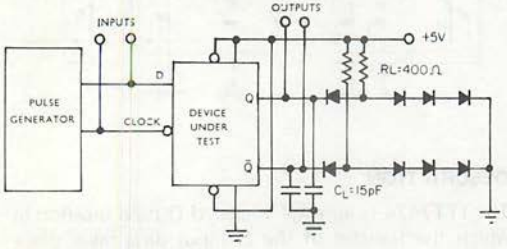
PARAMETER	LIMIT				CONDITIONS	
	Min.	Typ. at 25°C	Max.	Unit	V_{CC}	
$-I_F$ Preset or D input		1.0	1.6	mA	Max.	V_F=0.4V
Clear or clock		2.0	3.2	mA	Max.	V_F=0.4V
I_R D input			40	μA	Max.	V_R=2.4V
Preset or clock			80	μA	Max.	V_R=2.4V
All inputs			1	mA	Max.	V_R-5.5V
Clear			120	μA	Max.	V_R=2.4V
I_{CC}		17	30	mA	Max.	All inputs high

Information on the absolute maximum ratings and the other D.C. characteristics of this device (which are common to other integrated circuits in this series) is stated in the general information section.

SWITCHING CHARACTERISTICS V_{CC}=5.0V, T_{AMB}=25°C

PARAMETER	LIMIT				CONDITIONS
	Min.	Typ.	Max.	Unit	
f_{max} maximum input clock frequency	15	25		MHz	Use test circuit 1
t_{sp} minimum input set up time		15	20	ns	Use test circuit 1
t_h minimum input hold time		2	5	ns	Use test circuit 1
t_{pd+} clear or preset to output			25	ns	Use test circuit 2
t_{pd+} clock to output	10	14	25	ns	Use test circuit 1
t_{pd-} clear or preset to output			40	ns	Use test circuit 2
t_{pd-} clock to output	10	20	40	ns	Use test circuit 1

Test Circuit 1

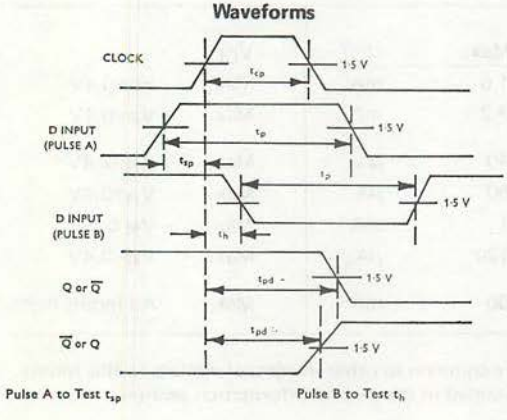


Pulse Characteristics

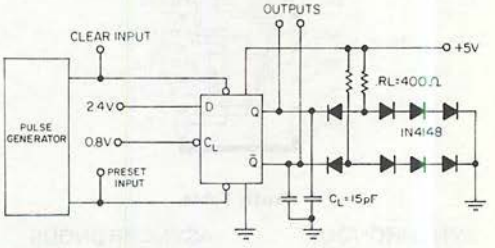
C_L includes probe and jig capacitance

t_r = 10 ns
t_f = 4 ns
t_{cp} = 30 ns
t_p (D input) = 60 ns
R.F. clock = 1 MHz
R.F D input = ½ R.F clock
Amplitude = 3.5 V

Waveforms



Test Circuit 2



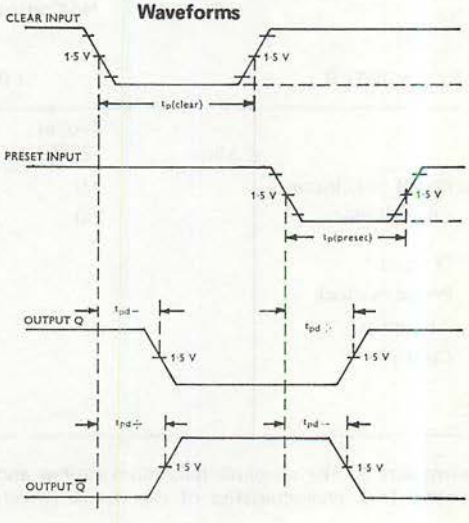
Pulse Characteristics

C_L includes probe and jig capacitance

t_r = 4 ns
t_f = 10 ns
t_p = 25 ns
R.F = 1 MHz

Amplitude = 3.5V

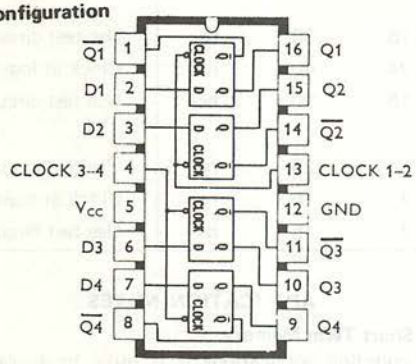
Waveforms



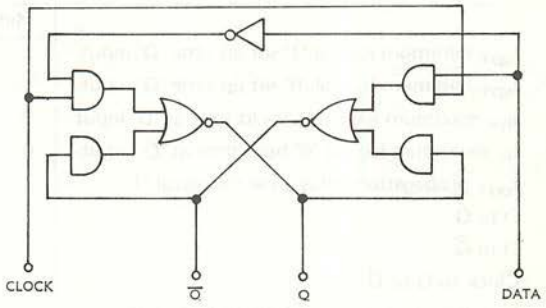
TYPICAL CHARACTERISTICS

Propagation delay . . . . . 12 ns
Power dissipation . . . . . 160 mW
Input loading factor
D input . . . . . 2 unit loads
Clock input. . . . . 4 unit loads
Fan-out . . . . . 1 to 10 unit loads

Pin configuration



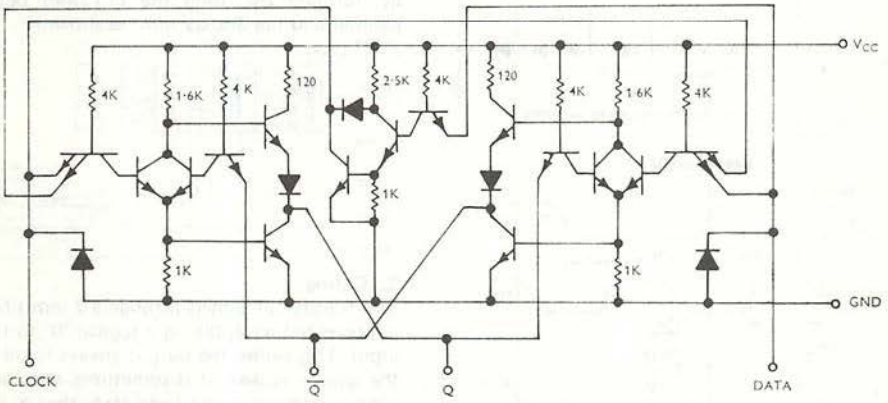
Logic diagram



DESCRIPTION

These latches consist of two cross coupled AND-OR-INVERT gates and one data inverter. When the clock input goes to a logical '0' state the Q output remains in its last logic state. When the clock goes to a logical '1' state the Q output follows the logic state of the D input.

Circuit diagram (Resistance values in ohms)



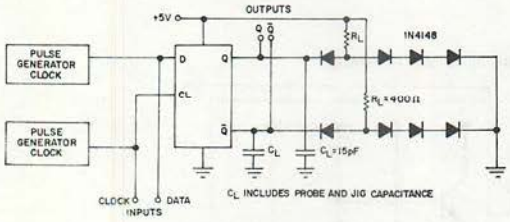
PARAMETER	LIMIT				CONDITIONS	
	Min.	Typ. at 25°C	Max.	Units	V_{CC}	
I_{CCH} supply current highest dissipation state		34		mA	Max.	Clock at logical '0', Data at logical 1'
I_{CCL} supply current lowest dissipation state						
64/7475		28	53	mA	Max.	Clock and data inputs at logical '0'
5475		28	46	mA		

Information on the absolute maximum ratings and the other D.C. characteristics of this device (which are common to other integrated circuits in this series) is stated in the general information section.

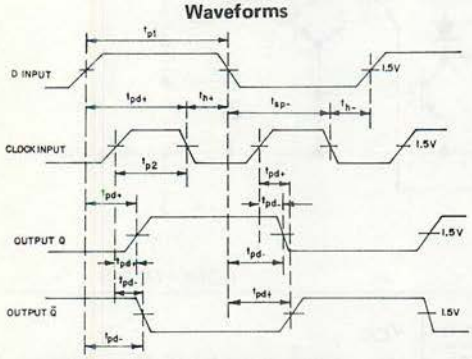
SWITCHING CHARACTERISTICS V_{CC}=5.0V, T_{AMB}=25°C

PARAMETER	LIMIT				CONDITIONS
	Min.	Typ.	Max.	Unit	
t_{sp+} minimum logical '1' set up time 'D' input		7	20	ns	Use test circuit
t_{sp+} minimum logical '0' set up time 'D' input		14	20	ns	Use test circuit
t_{h+} maximum logical '1' hold time at 'D' input	0	−15		ns	Use test circuit
t_{h-} maximum logical '0' hold time at 'D' input	0	−6		ns	Use test circuit
t_{pd+} propagation delay time to logical '1'					
D to Q		16	30	ns	Use test circuit
D to $\bar{Q}$		24	40	ns	Clock at logical 1'
Clock to Q or $\bar{Q}$		16	30	ns	Use test circuit
t_{pd+} propagation delay time to logical '0'					
D to Q		14	25	ns	Use test circuit
D to $\bar{Q}$		7	15	ns	Clock at logical '1'
Clock to Q or $\bar{Q}$		7	15	ns	Use test circuit

Switching test circuit



Waveforms



The pulse generators have the following characteristics

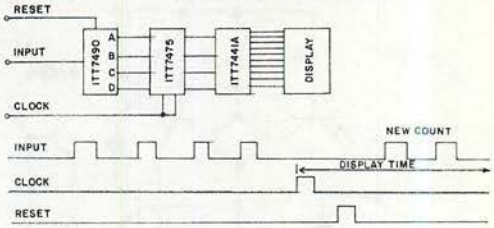
Amplitude	= 3.5 V	R.F data	= ½ clock R.F
t_r	= 10 ns	t_{p1}	= 1 µs
t_f	= 4 ns	t_{p2}	= 500 ns
R.F clock	= 1 MHz		

Phase relation between clock and data signals can be varied to test t_{sp} and t_h.

APPLICATION NOTES

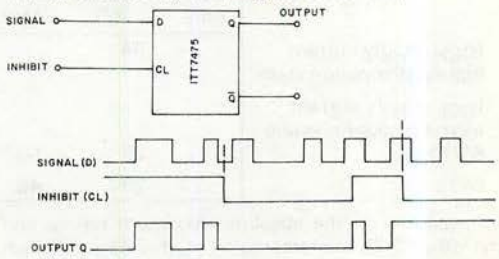
1. Short Term Memory

In counting applications it is usual to display the final count for a period of time, while the counter is counting new information. This requirement is readily fulfilled by using the ITT7445 between the counter and the display unit, as shown.



2. Gating

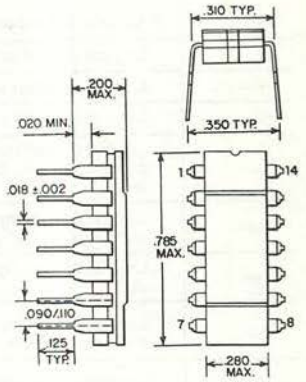
The transfer of signals through a 2 input NAND gate is prevented by applying a logical '0' to the control input. This causes the output always to be high when the gate is closed. It is sometimes required that the output remains in the logic state that is present the instant the inhibit signal is applied. This function is readily achieved by utilizing the ITT7475.



GATED FULL ADDERS

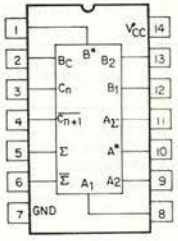
The ITT54/7480J is a single-bit, high-speed, binary full adder with gated complementary inputs, complementary sum (Σ and $\overline{\Sigma}$) outputs and inverted carry output, designed for medium- and high-speed, multiple-bit, parrallel-add/serial-carry applications. The circuit (see schematic diagram) uses diode-transistor logic (DTL) for the gated inputs, and high-speed, high-fan-out transistor-transistor logic (TTL) for the sum and carry outputs. The circuit is entirely compatible with both DTL and TTL logic families. A single-inversion, high-speed, Darlington-connected serial-carry circuit is added to minimize the amount of "look-ahead" and carry cascading circuitry required.

DIMENSIONS



ABSOLUTE MAXIMUM RATINGS

CHARACTERISTICS		UNITS
Supply Voltage V_{CC} (See Note 4)	7	Volts
Input Voltage, V_{in} (See Notes 4 and 5)	5.5	Volts
Operating Case Temperature Range:		
ITT5480J Circuits	−55 to 125	°C
Operating Free-Air Temperature Range:		
ITT5480J, ITT5480J Circuits	−55 to 125	°C
ITT7480J Circuits	0 to 70	°C
Storage Temperature Range	−65 to 150	°C



RECOMMENDED OPERATING CONDITIONS

Supply Voltage V_{CC}:	ITT5480J Circuits	5 Volts ± 10%
	ITT7480J Circuits	5 Volts ± 10%
Fan-Out:	$\overline{C_{n+1}}$, N	1 to 5
	Σ or $\overline{\Sigma}$, N	1 to 10
	A* or B*, N	1 to 3

NOTES:
1. $A = \overline{A^* A_C}$, $B = \overline{B^* B_C}$ where $A^* = \overline{A_1 A_2}$, $B^* = \overline{B_1 B_2}$.
2. When A* or B* are used as inputs, A_1 and A_2 or B_1 and B_2 respectively must be connected to GND.
3. When A_1 and A_2 or B_1 and B_2 are used as inputs, A* or B* respectively must be open or used to perform Dot-OR logic.
4. The voltages are with respect to ground terminal.
5. Input signals must be zero or positive with respect to network ground terminal.

TRUTH TABLE

(See Notes 1, 2, and 3)

C_n	B	A	$\overline{C_{n+1}}$	$\overline{\Sigma}$	Σ
0	0	0	1	1	0
0	0	1	1	0	1
0	1	0	1	0	1
0	1	1	0	1	0
1	0	0	1	0	1
1	0	1	0	1	0
1	1	0	0	1	0
1	1	1	0	0	1

ELECTRICAL CHARACTERISTICS (over operating temperature range unless otherwise noted)

SYMBOL	PARAMETER	TEST FIGURE	MIN	TYP‡	MAX	UNITS	TEST CONDITIONS†
$V_{in(1)}$	Logical 1 input voltage	1 and 2	2			V	V_{CC} = MIN
$V_{in(0)}$	Logical 0 input voltage	1 and 2			0.8	V	V_{CC} = MIN
$V_{out(1)}$	Logical 1 output voltage	2	2.4	3.5		V	V_{CC} = MIN
$V_{out(0)}$	Logical 0 output voltage	1		0.22	0.4	V	V_{CC} = MIN
$I_{in(0)}$	Logical 0 level input current at A_1, A_2, B_1, B_2, A_c or B_c	3			−1.6	mA	V_{CC} = MAX, V_{in} = 0.4 V
$I_{in(0)}$	Logical 0 level input current at A* or B*	4			−2.6	mA	V_{CC} = MAX, V_{in} = 0.4 V
$I_{in(0)}$	Logical 0 level input current at C_n	4			−8	mA	V_{CC} = MAX, V_{in} = 0.4 V
$I_{in(1)}$	Logical 1 level input current at A_1, A_2, B_1, B_2, A_c or B_c	5			15 1	μA mA	V_{CC} = MAX, V_{in} = 2.4 V V_{CC} = MAX, V_{in} = 5.5 V
$I_{in(1)}$	Logical 1 level input current at C_n	6			200 1	μA mA	V_{CC} = MAX, V_{in} = 2.4 V V_{CC} = MAX, V_{in} = 5.5 V
I_{OS}	Short-circuit output current at Σ or Σ§	7		−20 −18	−57 −57	mA mA	V_{CC} = MAX ITT5480J ITT7480J
I_{OS}	Short-circuit output current at C_{n+1}§	7		−20 −18	−70 −70	mA mA	V_{CC} = MAX ITT5480J ITT7480J
I_{CC}	Supply current	8		21 21	31 35	mA mA	V_{CC} = MAX ITT5480J ITT7480J

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Not more than one output should be shorted at a time.

SWITCHING CHARACTERISTICS, V_{CC} = 5 V, T_A = 25°C

PARAMETER¶	FROM INPUT	TO OUTPUT	FIGURE 9 TEST NO.	MIN	TYP	MAX	UNITS	TEST CONDITIONS
t_{pd1}	C_n	$\overline{C_{n+1}}$	1		13	17	ns	C_L = 15 pF, R_L = 780 Ω
t_{pd0}			2		8	12	ns	C_L = 15 pF, R_L = 780 Ω
t_{pd1}	B_C	$\overline{C_{n+1}}$	3		18	25	ns	C_L = 15 pF, R_L = 780 Ω
t_{pd0}			4		38	55	ns	C_L = 15 pF, R_L = 780 Ω
t_{pd1}	A_C	Σ	5		52	70	ns	C_L = 15 pF, R_L = 400 Ω
t_{pd0}			6		62	80	ns	C_L = 15 pF, R_L = 400 Ω
t_{pd1}	B_C	$\overline{\Sigma}$	7		38	55	ns	C_L = 15 pF, R_L = 400 Ω
t_{pd0}			8		56	75	ns	C_L = 15 pF, R_L = 400 Ω
t_{pd1}	A_I	A*	9		48	65	ns	C_L = 15 pF
t_{pd0}			10		17	25	ns	C_L = 15 pF
t_{pd1}	B_I	B*	11		48	65	ns	C_L = 15 pF
t_{pd0}			12		17	25	ns	C_L = 15 pF

¶ t_{pd1} is propagation delay time to logical 1 level. t_{pd0} is propagation delay time to logical 0 level.

TYPICAL APPLICATIONS

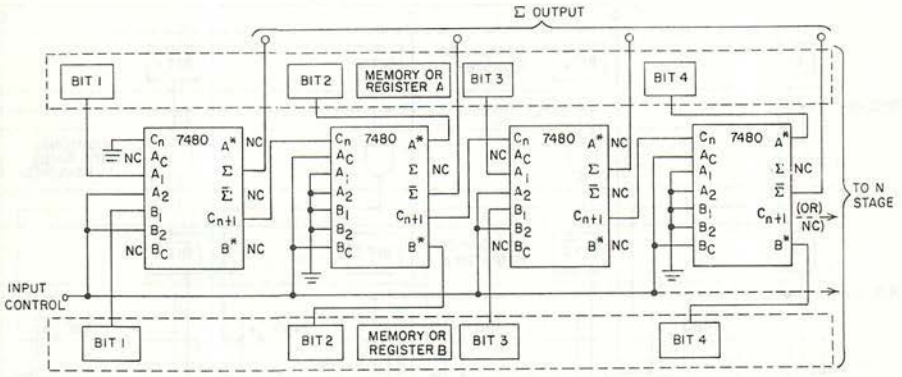
n-bit binary adder or subtractor (see figures A and B)

The ITT7480J is designed specifically for N-bit adder or subtractor operations without external gates or inverters. In both applications, the sum or difference functions are generated in parallel while the carry functions are obtained serially. When the number of stages is small, the add or subtract time determines the maximum system clock rate. However, as the number of bits increases, the time required for the carry function to ripple through each bit becomes the limiting factor. Normally the ripple time of adders built with standard integrated circuits is excessive, and the resulting system speed is so slow that other more complex methods are required to perform these functions.

In the ITT7480J, two methods are used to reduce the carry delay. The carry circuit employs a high-speed Darlington output, and the logic gating has only one inversion between the C_n input and the C_{n+1} output. This logic configuration results in an inverted carry output, and consequently an inverted carry input to the succeeding stage. To counteract this inverted input without sacrificing propagation time through the carry, gates are provided within the circuit to invert the A and B inputs and the resulting sum or difference output. This interconnection method is illustrated by bit 2 and bit 4 of the adder (Figure A). The inverted carry output is a true carry from bit 2 and bit 4, enabling the use of noninverted A and B inputs for the odd-numbered bits.

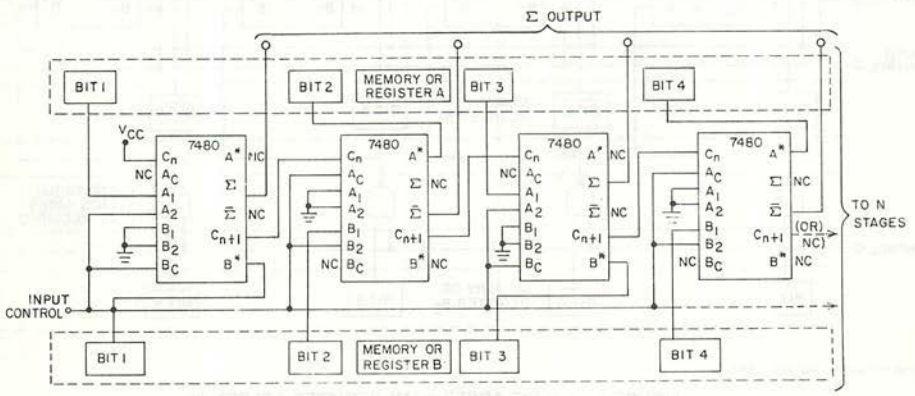
When performing subtraction (Figure B) the C_n input to bit 1 is connected to a logical 1 and input bits and input control functions for the subtrahend (memory or register B) are effectively inverted.

The input control is used to disable the A and B inputs when memory or register information is being shifted. A logical 0 applied to this line will bring each sum or difference output to a logical 0 condition and maintain this level regardless of the state of the input information into each bit. For the adder (Figure A), input control is applied to A_2 and B_2 of odd-numbered bits and to A_C and B_C of even numbered bits. For the subtractor (Figure A), input control is applied to A_2 and B_C of the odd-numbered bits and to A_C and B_2 of the even-numbered bits. These alternating patterns are necessary to complement the varying input sequence which they control.



NOTE: Functions noted as NC are open.

FIGURE A — N-BIT BINARY ADDER



NOTE: Functions noted as NC are open.

FIGURE B — N-BIT BINARY SUBTRACTOR

TYPICAL APPLICATIONS

n-bit binary adder with register selection (see figure C)

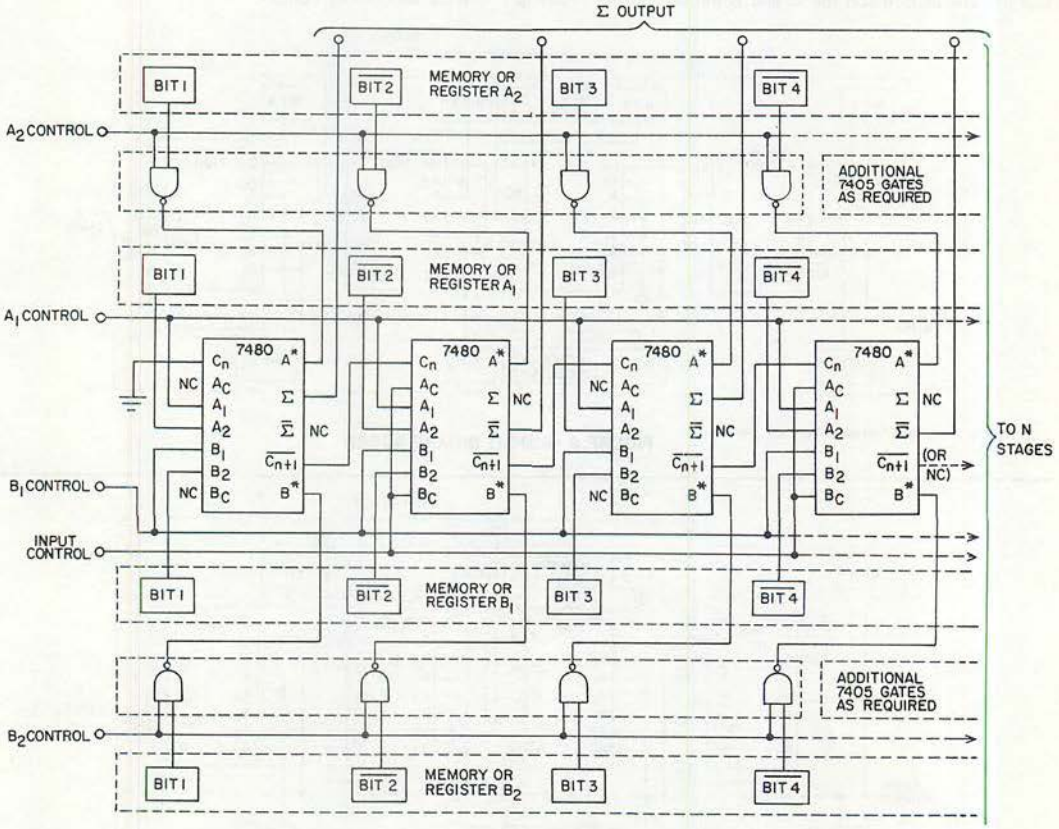
This application fully utilizes the flexibility of the input gating available with the ITT7480J. Two "A" registers and two "B" registers drive a single adder for each bit required. Register selection is performed internally for registers A_1 and B_1, and externally by a type ITT7405J TTL gate for registers A_2 and B_2. Dot-OR logic is performed at the A* and B* nodes within the adder when the register selection is made.

Operation is as follows: To add the contents of Register A_1 to Register B_1, A_2 and B_2 control lines are brought to the logical 0 state. In similar fashion, the contents of register A_1 are added to register B_2 by holding A_2 and B_1 control lines at a logical 0. Four register combinations may be used. Even-numbered input ibts from each register must be inverted since the A* and B* inputs are being used to perform Dot-OR logic. This is not a configuration restriction for flip-flop type registers and memories, but may require additional logic elements if other storage configurations are used as inputs.

The input control function is available as in the previous application and is implemented by bringing all four register control lines and the input control line to a logical 0 level. This condition ensures a logical 0 at each Σ output regardless of "A" and "B" register logic levels.

Up to four "A" registers and four "B" registers may be implemented in a fashion analogous to that shown in Figure C. Inputs from the register-control gates (ITT7405J) of the additional registers would be Dot-OR connected with A_2 and B_2 registers at the A* and B* inputs.

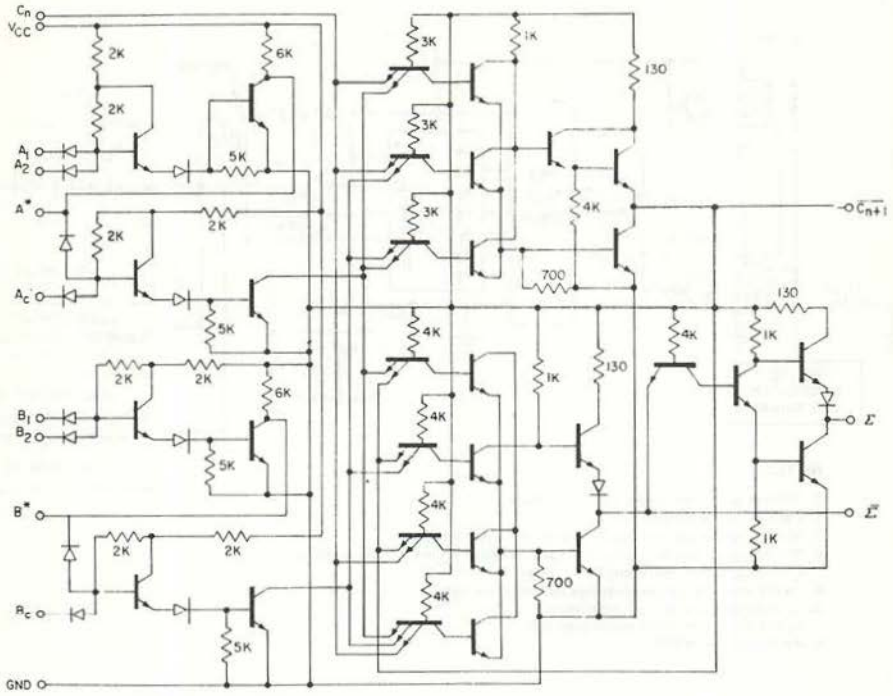
To perform N-bit subtraction, the C_n input at bit 1 is connected to a logical 1 and bit inputs from each register or memory used as a subtrahend must consist of the complement of bit inputs shown for the adder addend. Input control remains the same.



NOTE: Functions noted as NC are open.

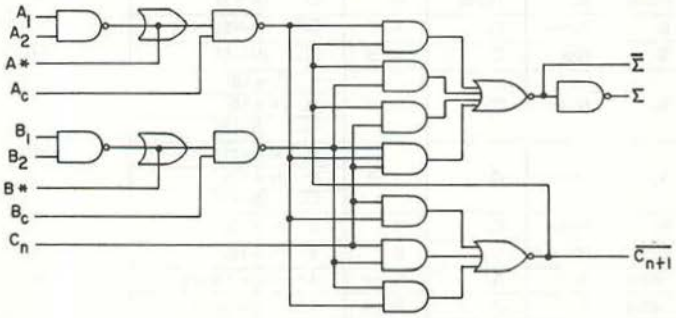
FIGURE C — N-BIT ADDER WITH REGISTER SELECTION

SCHEMATIC



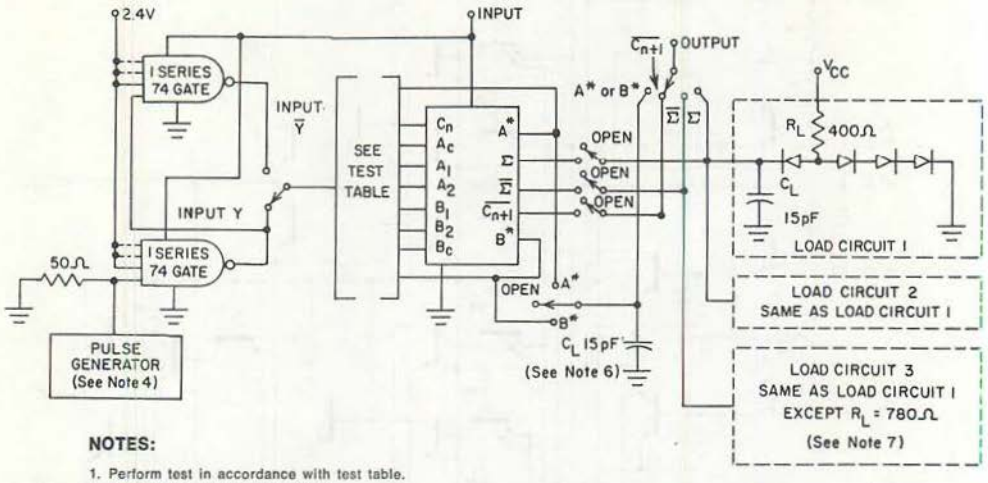
Component values shown are nominal.
Resistor values are in ohms.

FUNCTIONAL BLOCK DIAGRAM



PARAMETER MEASUREMENT INFORMATION

SWITCHING CHARACTERISTICS

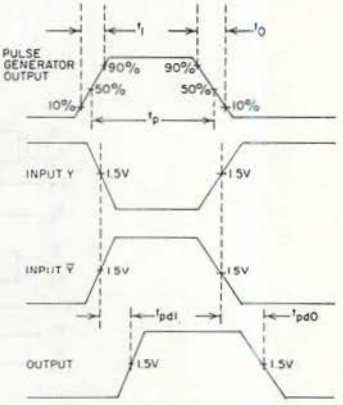


NOTES:

1. Perform test in accordance with test table.
2. Each output is tested separately.
3. Voltage values are with respect to network GND terminal.
4. The generator has the following characteristics: V_{gen} = 3 V, $t_r = t_f \leq$ 15 ns, t_p = 0.5 μs, PRR = 1 MHz, and Z_{out} ≈ 50 Ω.
5. Inputs and outputs not otherwise specified are open.
6. C_L includes probe and jig capacitance.
7. Load circuit 2 simulates output load of 5.
8. All diodes are 1N3064.

TEST TABLE (See Note 5)

TEST NO.	OUTPUT UNDER TEST	APPLY INPUT Y TO	APPLY INPUT Y TO	APPLY +2.4 V TO	APPLY GND TO	APPLY OUTPUT LOADING TO
1	$\overline{C_{n+1}}$	None	C_n	None	B_1	$\overline{C_{n+1}}$ (N = 5)
2	$\overline{C_{n+1}}$	None	C_n	None	B_1	$\overline{C_{n+1}}$ (N = 5)
3	$\overline{C_{n+1}}$	B_C	None	C_n	A_1, B_1	$\overline{C_{n+1}}$ (N = 5)
4	$\overline{C_{n+1}}$	B_C	None	C_n	A_1, B_1	$\overline{C_{n+1}}$ (N = 5)
5	Σ	A_C	None	C_n	A_1, B_1	Σ (N = 10) Σ (N = 10) $\overline{C_{n+1}}$ (N = 5)
6	Σ	A_C	None	C_n	A_1, B_1	Σ (N = 10) Σ (N = 10) $\overline{C_{n+1}}$ (N = 5)
7	$\overline{\Sigma}$	B_C	None	C_n	B_1	$\overline{\Sigma}$ (N = 10)
8	$\overline{\Sigma}$	B_C	None	C_n	B_1	$\overline{\Sigma}$ (N = 10)
9	A*	None	A_1	A_2	None	A* (C_L = 15 pF)
10	A*	None	A_1	A_2	None	A* (C_L = 15 pF)
11	B*	None	B_1	B_2	None	B* (C_L = 15 pF)
12	B*	None	B_1	B_2	None	B* (C_L = 15 pF)



VOLTAGE WAVEFORMS

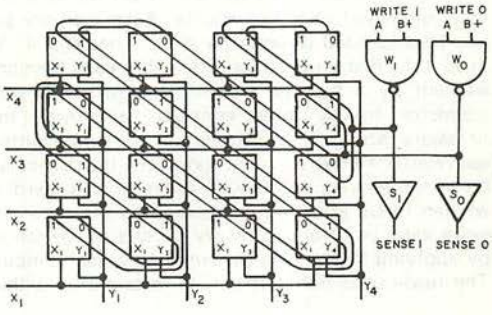
FIGURE 9 — SWITCHING TIMES

ITT7481 DIRECT WRITE INPUT
ITT7484 STROBED WRITE INPUT

TYPICAL CHARACTERISTICS

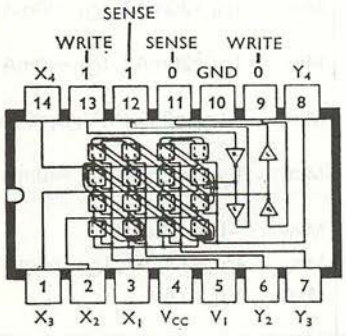
Power dissipation	275 mW
Read time	20 ns
Fan-in	See D.C. tests
Fan-out	See D.C. tests

Logic diagram

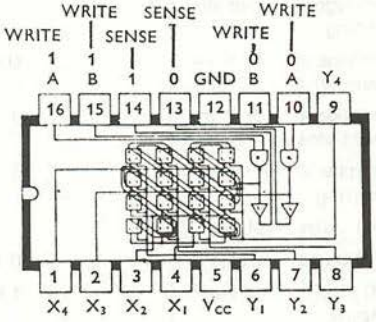


Pin configurations (top view)

ITT7481

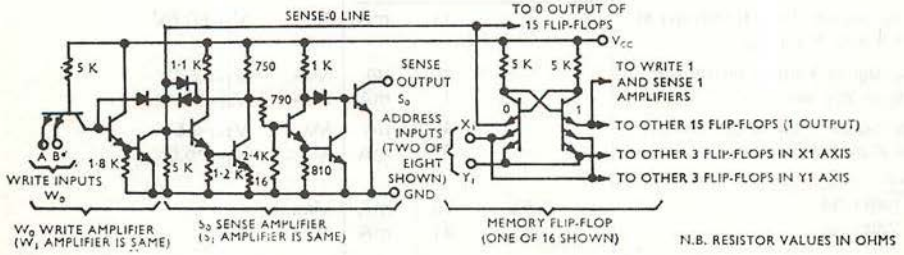


ITT7484



ITT7484 only

Circuit diagram showing one memory element and sense/write '0' amplifier



†The ITT7484 is the same as the ITT7481, but with the addition of strobed write inputs (as shown above).

Note: Sense outputs, S_0 and S_1, are open-collector outputs.

DESCRIPTION

The ITT7481 and ITT7484 are 16-bit memory circuits organized in a 4x4 matrix. Each memory bit can be addressed directly by 4 'X' lines and 4 'Y' lines. Information is contained within each memory element by a bistable transistor circuit, with each transistor having three emitters to provide the necessary gating. The information contained within each element is written in by addressing the particular bit at the address inputs with a logical 1. A 'Zero' is written in by applying a logical 1 to the common write zero input and similarly, a 'one' is written in by applying logical 1 to the common write '1' input. The read-out is non-destructive. Information within each element is read-out by addressing each bit using the appropriate address inputs X_{1-4} and Y_{1-4}. The read output signal is obtained at the output of the sense amplifiers as a logical '0' on the sense 1 or sense 0 outputs depending upon whether there is a logic '1' or '0' stored in the bit.

The information in the memory is destroyed when supply voltage is removed, i.e. it is volatile.

The store can be considered as 16 words of only one bit. A larger scratch pad memory can be constructed by using many of these devices with the appropriate common address lines. Alternatively, the store can be used as a single 16-bit memory with serial write-in and read-out.

PARAMETER	LIMIT				CONDITIONS	
	Min.	Typ.at 25°C	Max.	Unit	V_{CC}	
V_{IH} input voltage at X or Y inputs to ensure writing or sensing	2.1			V	Min.	I_{OL}=20mA*, I_{OL}=40mAt, V_{OL} 0.4V
V_{IH} input voltage at W_0 or W_1 to ensure writing	2			V	Min.	I_{OL}=20mA*, I_{OL}=40mA†, V_{OL} < 0.4V
V_{IL} input voltage at X or Y inputs to prevent writing			0.8	V	Min.	I_{OL}=20mA*, I_{OL}=40mA†, V_{OL} < 0.4V
V_{IL} input voltage at X or Y inputs to prevent sensing			1	V	Min.	$-I_{OH}$=250μA, V_{OH}=5.5V
V_{IL} input voltage at W_0 or W_1 to prevent writing			1	V	Min.	I_{OL}=20mA*, I_{OL}=40mA†, V_{OL} < 0.4V
V_{OH} logical 1 output voltage	5.5			V	Min.	$-I_{OH}$=250μA
V_{OL} logical 0 output voltage			0.4	V	Min.	I_{OL}=20mA*, I_{OL}=40mA†
$-I_F$ logical 0 input current at W_0 or W_1 inputs			1.6	mA	Max.	V_{IL}=0.4V

PARAMETER	LIMIT				CONDITIONS	
	Min.	Typ.at 25°C	Max.	Unit	V_{CC}	See Test Circuit
$-I_F$ logical 0 input current at all X and Y inputs			11	mA	Max.	V_{IL}=0.4V
I_R logical 1 input current at W_0 or W_1 inputs			40	μA	Max.	V_{IH}-2.4V
			1	mA	Max.	V_{IH}-5.5V
I_R logical 1 input current at all X and Y inputs			400	μA	Max.	V_{IH}-4.5V
			3	mA	Max.	V_{IH}=5.5V
I_{CC}						
5481-84		55	78	mA	Max.	
7481-84		55	91	mA	Max.	

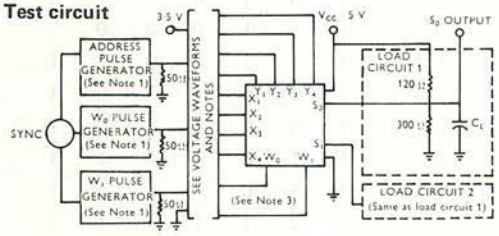
*ITT5481, ITT5484 only.
†ITT7481, ITT7484 only.

Information on the absolute maximum ratings of these devices is stated in the general information section.

SWITCHING CHARACTERISTICS V_{CC}=5V, T_{AMB}=25°C

PARAMETER	LIMIT			CONDITIONS
	Min.	Max.	Unit	
t_{pd-} propagation delay from address inputs	22	45	ns	Address each memory bit C_L=15pF
To sense outputs	27	55	ns	C_L=200pF
t_{pd+} propagation delay from address inputs	15	25	ns	Address each memory bit C_L=15pF
To sense outputs	20	35	ns	C_L=200pF
t_{pd-} propagation delay from address inputs to sense outputs	20	30	ns	C_L=15pFY, locations only addressed. Address X1 to X4
t_{WR} write recovery time	30	60	ns	Address each memory bit C_L=15pF

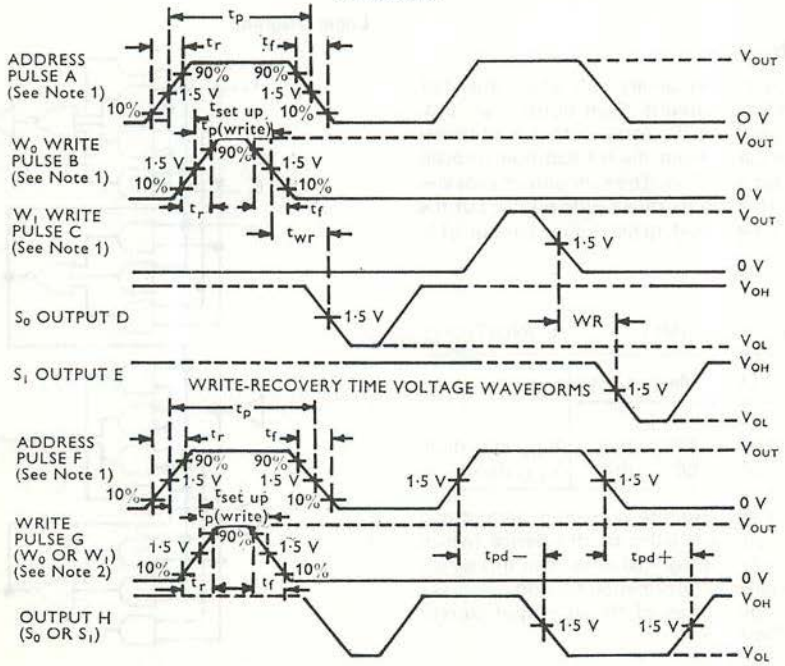
Test circuit



NOTES:

1. The pulse generators have the following characteristics: V_{OUT}=3V, t_r=t_f=10ns, t_{setup}=0 to 10ns. For the address pulse generator, t_p=100ns and P.R.F.=2MHz. For the W_0 and W_1 pulse generators, t_p=25ns and P.R.F.=1MHz.
2. C_L includes probe and jig capacitance.
3. For the ITT7484, unused W_0 and W_1 inputs are 3.5V.

Waveforms

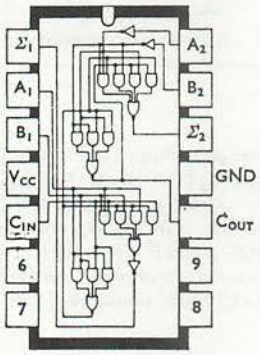


ITT7482
TWO BIT BINARY FULL ADDER

TYPICAL CHARACTERISTICS

Carry propagation delay . . . . . 15 ns
Power dissipation . . . . . 175 mW
Input loading factor at
A_1 B_1 C_{IN} inputs . . . . . 4 unit loads
Input loading factor at A_2 B_2 inputs . . 1 unit load
Maximum fan out Σ_1 Σ_2 output 10
Maximum fan out C_{OUT} output 5

Pin configuration
(top view)



Truth Table

Input				Output					
				When C_{IN}=0			When C_{IN}=1		
A_1	B_1	A_2	A_2	Σ_1	Σ_2	C_{OUT}	Σ_1	Σ_2	C_{OUT}
0	0	0	0	0	0	0	1	0	0
1	0	0	0	1	0	0	0	1	0
0	1	0	0	1	0	0	0	1	0
1	1	0	0	0	1	0	1	1	0
0	0	1	0	0	1	0	1	1	0
1	0	1	0	1	1	0	0	0	1
0	1	1	0	1	1	0	0	0	1
1	1	1	0	0	0	1	1	0	1
0	0	0	1	0	1	0	1	1	0
1	0	0	1	1	1	0	0	0	1
0	1	0	1	1	1	0	0	0	1
1	1	0	1	0	0	1	1	0	1
0	0	1	1	0	0	1	1	0	1
1	0	1	1	1	0	1	0	1	1
0	1	1	1	1	0	1	0	1	1
1	1	1	1	0	1	1	1	1	1

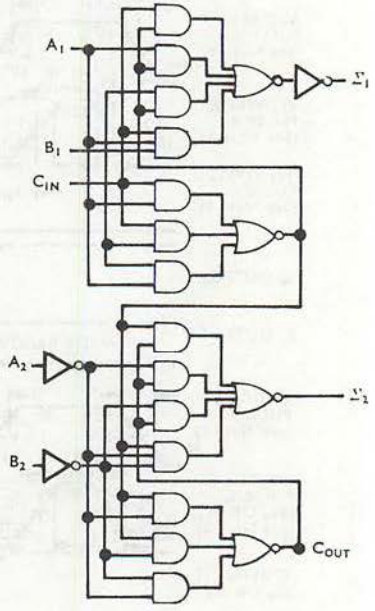
DESCRIPTION

The ITT7482 is a 2-bit binary full adder intended for parallel addition circuits. Sum outputs are provided for each bit and the carry output is obtained by routing the carry from the bit addition through to the second bit addition. The sum output provides full fan-out of 10 from its totem pole output but the carry output is restricted to maximum fan-out of 5.

PARAMETER	LIMIT			CONDITIONS
	Min.	Typ.	Max.	Units	
I_{CCH}					
7482		35	58	mA	V_{CC} maximum
5482		35	50	mA	V_{CC} maximum

Information on the absolute maximum ratings and the other D.C. characteristics of this device (which are common to other integrated circuits in this series) is stated in the general information section.
The maximum limit of short circuit output current at C_{OUT} is −70mA.

Logic Diagram

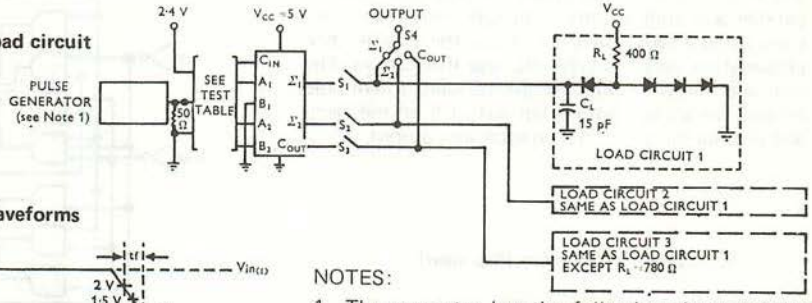


SWITCHING CHARACTERISTICS V_{CC}=5V, T_{AMB}=25°C

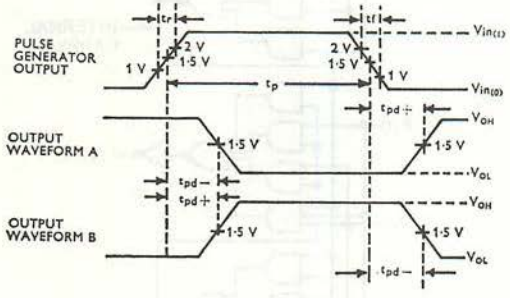
PARAMETER			LIMITS				CONDITIONS		
	From input	To output	Min.	Typ. at 25°C	Max.	Units	V_{CC}		Test No.
t_{pc+}	C_{IN}	Σ_1			34	ns	5V	*	1
t_{pd-}	C_{IN}	Σ_1			40	ns	5V	*	2
t_{pd+}	C_{IN}	Σ_2			38	ns	5V	*	3
t_{pd-}	C_{IN}	Σ_2			42	ns	5V	*	4
t_{pd+}	B_2	Σ_2			40	ns	5V	*	5
t_{pd-}	B_2	Σ_2			35	ns	5V	*	6
t_{pd+}	C_{IN}	C_{OUT}		17	27	ns	5V	*	7
t_{pd-}	C_{IN}	C_{OUT}		12	19	ns	5V	*	8

*As test circuit with C_L=15 pF R_L=400 Ω

Switching test load circuit



Waveforms



NOTES:

1. The generator has the following characteristics: $V_{in(1)} \geq 2.4V$, $V_{in(0)} \leq 0.4V$, t_r = 8 15 ns, t_f = 3 to 5 ns, PRF = 1 MHz, t_p = 200 ns, and $Z_{out} \approx 50\ \Omega$.
2. Perform test in accordance with test table.
3. Each output is tested separately.
4. Voltage values are with respect to network ground terminal.
5. C_L includes probe and jig capacitance.

All diodes are IN4148.

Test Table

Test No.	Parameter	Apply pulse Generator Output to	Output under Test (S4)	Apply 2.4 V to	Apply GND to	S1	S2	S3
1	t_{pd+}	C_{IN}	Σ_1	A_1	A_2,B_1,B_2	Closed	Open	Open
2	t_{pd-}		(Waveform A)					
3	t_{pd+}	C_{IN}	Σ_2	A_1,A_2	B_1,B_2	Open	Closed	Closed
4	t_{pd-}		(Waveform A)					
5	t_{pd+}	B_2	Σ_2	None	A_1,B_1,A_2 and C_{IN}	Open	Closed	Open
6	t_{pd-}		(Waveform B)					
7	t_{pd+}	C_{IN}	C_{OUT}	A_1,A_2	B_1,B_2	Open	Open	Closed
8	t_{pd-}		(Waveform B)					

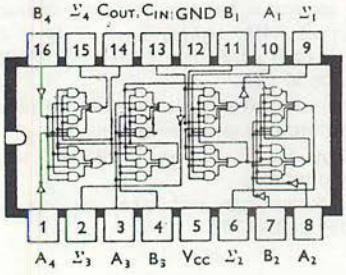
TYPICAL CHARACTERISTICS

Carry propagation delay . . . . . 29 ns
Power dissipation . . . . . 390 mW
Input loading factor (inputs A_1, B_1, A_3, B_3, C_{IN}) . . . . . 4 unit loads
Input loading factor (inputs A_2, B_2, A_4, B_4) . . . . . 1 unit load
Maximum fan out Σ_1 Σ_2 Σ_3 and Σ_4 . . . . . 10 unit loads
Maximum fan out C_{OUT} . . . . . 5 unit loads

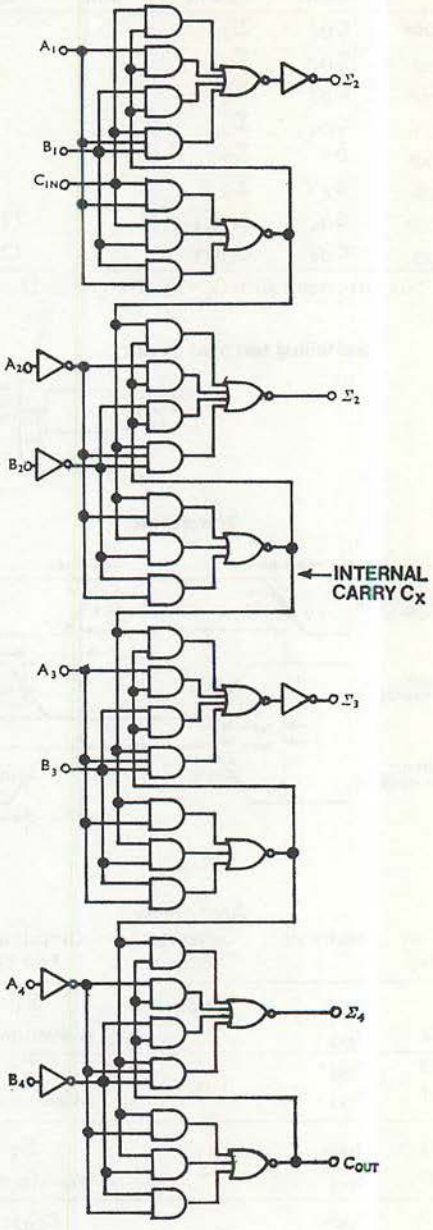
DESCRIPTION

The ITT7483 is a 4 bit binary full adder suitable for parallel add applications. Although the circuit functions using a serial carry technique the overall carry propagation delay is typically less than 30 ns. The sum and carry outputs are the standard totem pole output circuit but with a fan out of 5 on the carry and the full fan out of 10 on each sum output.

Pin configuration (top view)



Logic diagram



First Addition									
Inputs				C_{in}=0			C_{in}=1		
A_1	B_1	A_2	B_2	Σ_1	Σ_2	C_X	Σ_1	Σ_2	C_X

Second Addition									
Inputs				C_X=0			C_X=1		
A_3	B_3	A_4	B_4	Σ_3	Σ_4	C_{OUT}	Σ_3	Σ_4	C_{OUT}
0	0	0	0	0	0	0	1	0	0
1	0	0	0	1	0	0	0	1	0
0	1	0	0	1	0	0	0	1	0
1	1	0	0	0	1	0	1	1	0
0	0	1	0	0	1	0	1	1	0
1	0	1	0	1	1	0	0	0	1
0	1	1	0	1	1	0	0	0	1
1	1	1	0	0	0	1	1	0	1
0	0	0	1	0	1	0	1	1	0
1	0	0	1	1	1	0	0	0	1
0	1	0	1	1	1	0	0	0	1
1	1	0	1	0	0	1	1	0	1
0	0	1	1	0	0	1	1	0	1
1	0	1	1	1	0	1	0	1	1
0	1	1	1	1	0	1	0	1	1
1	1	1	1	0	1	1	1	1	1

Truth Table

The truth table considers only half of the operation of this full adder – the sum of two bits with the carry input (A_1, A_2 with B_1, B_2). Using the truth table the sum of the first two bits with the carry input (C_{IN}) can be determined giving the first two bits of the sum output (Σ_1 and Σ_2) and an internal carry (C_X). This internal carry is added to the last two bits of the binary input signal (A_3, A_4 with B_3, B_4) to give the last two bits of the sum output (Σ_3 and Σ_4) and the carry output (C_{OUT}). By using the truth table again for the second addition the outputs can be determined for any condition of the inputs.

PARAMETER	LIMITS				CONDITIONS
	Min.	Typ.at 25°C	Max.	Units	V_{CC}
I_{CCH}					
7483		78	128	mA	Max. V_{IN}=4.5V
5483		78	110	mA	Max. V_{IN}=4.5V

Information on the absolute maximum ratings and the other D.C. characteristics of this device (which are common to other integrated circuits in this series) is stated in the general information section.

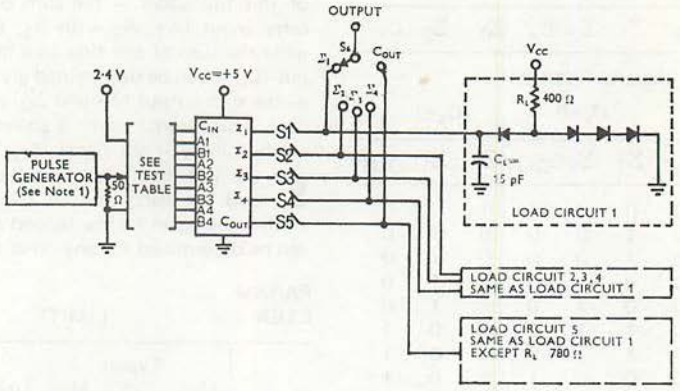
The maximum limit of short circuit output current at C_{OUT} is −70 mA.

SWITCHING CHARACTERISTICS V_{CC}=5V, T_A=25°C

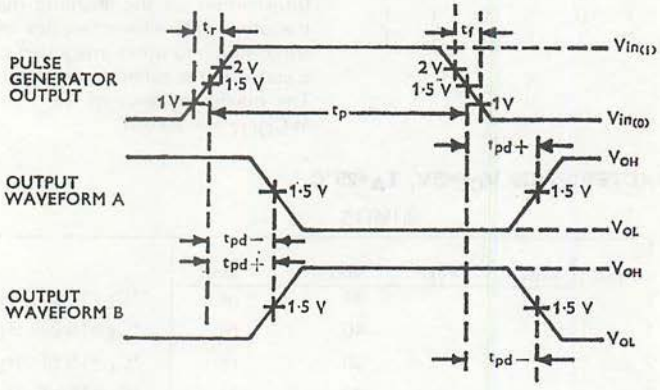
PARAMETER			LIMITS				CONDITIONS	
	From input	To output	Min.	Typ.	Max.	Unit		Test No.
t_{pd+}	C_{IN}	1			34	ns	*C_L=15 pF, R_L=400 Ω	1
t_{pd-}	C_{IN}	1			40	ns	*C_L=15 pF, R_L=400 Ω	2
t_{pd+}	C_{IN}	2			38	ns	*C_L=15 pF, R_L=400 Ω	3
t_{pd-}	C_{IN}	2			42	ns	*C_L=15 pF, R_L=400 Ω	4
t_{pd+}	C_{IN}	3			50	ns	*C_L=15 pF, R_L=400 Ω	5
t_{pd-}	C_{IN}	3			60	ns	*C_L=15 pF, R_L=400 Ω	6
t_{pd+}	C_{IN}	4			55	ns	*C_L=15 pF, R_L=400 Ω	7
t_{pd-}	C_{IN}	4			55	ns	*C_L=15 pF, R_L=400 Ω	8
t_{pd+}	C_{IN}	C_{OUT}		35	48	ns	*C_L=15 pF, R_L=780 Ω	9
t_{pd-}	C_{IN}	C_{OUT}		22	32	ns	*C_L=15 pF, R_L=780 Ω	10
t_{pd+}	A_2 or B_2	2			40	ns	*C_L=15 pF, R_L=400 Ω	11,13
t_{pd-}	A_2 or B_2	2			35	ns	*C_L=15 pF, R_L=400 Ω	12,14
t_{pd+}	A_4 or B_4	4			40	ns	*C_L=15 pF, R_L=400 Ω	15,17
t_{pd-}	A_4 or B_4	4			35	ns	*C_L=15 pF, R_L=400 Ω	16,18

*See switching test circuit and test table.

Switching test circuit



Waveforms



Notes:

1. Pulse generator output characteristics: $V_{in(1)} \geq$ 2.4 V, $V_{in(0)} \leq$ 0.4 V, t_r = 8 to 15 ns, t_f = 3 to 5 ns, P.R.F. = 1 MHz, tp = 200 ns, and $Z_{out} \backsimeq 50\ \Omega$.
2. Perform test in accordance with test table.
3. Each output is tested separately.
4. Voltage values are with respect to network ground terminal.
5. C_L includes probe and jig capacitance.
6. All diodes are IN4148.

Test Table

Parameter	Apply pulse generator output to	Output under test (S6)	Apply 2.4V to	Apply GND to	S1	S2	S3	S4	S5	Test No.
t_{pd+}	C_{IN}	Σ_1 (Waveform A)	A_1	B_1, A_2, and B_2	Closed	Open	Open	Open	Open	1
t_{pd-}										2
t_{pd+}	C_{IN}	Σ_2 (Waveform A)	A_1 and A_2	B_1 and B_2	Open	Closed	Open	Open	Open	3
t_{pd-}										4
t_{pd+}	C_{IN}	Σ_3 (Waveform A)	A_1, A_2, and A_3	B_1, B_2, and B_3	Open	Open	Closed	Open	Open	5
t_{pd-}										6
t_{pd+}	C_{IN}	Σ_4 (Waveform A)	A_1, A_2, A_3, and A_4	B_1, B_2, B_3, and B_4	Open	Open	Open	Closed	Open	7
t_{pd-}										8
t_{pd+}	C_{IN}	C_4 (Waveform A)	A_1, A_2, A_3, and A_4	B_1, B_2, B_3, and B_4	Open	Open	Open	Open	Closed	9
t_{pd-}										10
t_{pd+}	A_2	Σ_2 (Waveform A)	A_1, B_1, B_2, None	A_1, B_1, B_2, and C_{IN}	Open	Closed	Open	Open	Open	11
t_{pd-}										12
t_{pd+}	B_2	Σ_2 (Waveform B)	None	A_1, B_1, A_2, and C_{IN}	Open	Closed	Open	Open	Open	13
t_{pd-}										14
t_{pd+}	A_4	Σ_4 (Waveform B)	None	A_3, B_3, and B_4	Open	Open	Open	Closed	Open	15
t_{pd-}										16
t_{pd+}	B_4	Σ_4 (Waveform B)	None	A_3, B_3, and A_4	Open	Open	Open	Closed	Open	17
t_{pd-}										18

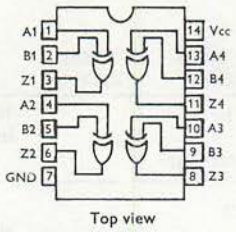
Inputs not specified are open

ITT7486
QUAD 2 INPUT EXCLUSIVE OR GATE

TYPICAL CHARACTERISTICS

Propagation Delay . . . . . 12 ns
Power Dissipation . . . . . 150 mW
Input Loading Factor . . . . . 1 unit load
Fan-out:
Logical '0' . . . . . 1 to 10 unit loads
Logical '1' . . . . . 1 to 20 unit loads

Pin Configuration



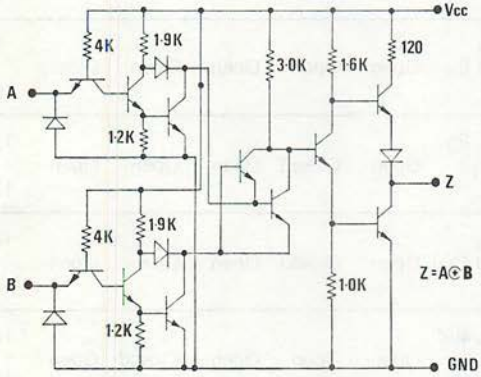
Top view

Truth Table

Inputs		Output
A	B	Z
0	0	0
0	1	1
1	0	1
1	1	0

DESCRIPTION

The 'Exclusive OR' function is correctly represented in Boolean Expressions as Z = AB + AB but is often abbreviated to Z = A ⊕ B. The operation is also represented in the truth table shown above, a convenient memory aid is to consider the device as a One Bit adder without carry. The fan-out of 20 provided in the logical '1' state is to facilitate the connection of unused inputs to used inputs.



Circuit diagram of one gate

Resistance values in ohms

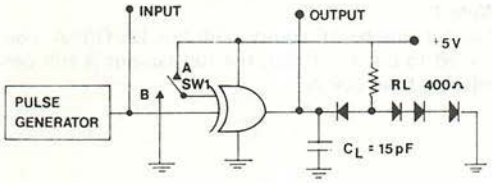
PARAMETER	LIMIT				CONDITIONS	
	Min.	Typ.at 25°C	Max.	Units	V_{CC}	
I_{CCH} supply current highest dissipation state						
74 series		30	50	mA	Max.	All inputs at logical '0'
54 series		30	43	mA	Max.	
I_{CCL} supply current lowest dissipation state						
74 series		26		mA	Max.	One input at 0 and
54 series		26		mA	Max.	one at '1' on each gate

Information on the absolute maximum ratings and the other D.C. characteristics of this device (which are common to other integrated circuits in this series) is stated in the general information section.

SWITCHING CHARACTERISTICS V_{CC}=5.0V, T_{AMB}=25°C

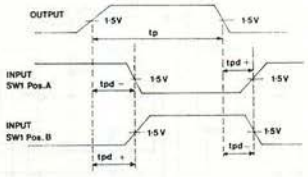
PARAMETER	LIMIT				CONDITIONS
	Min.	Typ.	Max.	Units	
t_{pd+} propagation delay time to logical '1'		15	23	ns	
other input low		15	23	ns	Use switching load
other input high		18	30	ns	circuit
t_{pd-} propagation delay time to logical '0'					
other input low		11	17	ns	Use switching load
other input high		13	22	ns	circuit

Switching load circuit



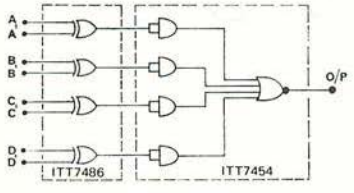
Pulse Characteristics
Amplitude = 3.5 V
t_r = 10 ns
t_f = 4 ns
R.F = 1 MHz
t_p = 500 ns

Waveforms



APPLICATION NOTE

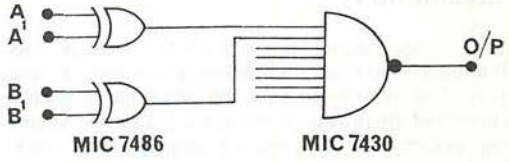
Comparator



The above circuit shows a two 4 bit number comparator which requires only the true signal of each number. When $A=A^1$, $B=B^1$, $C=C^1$, $D=D^1$ the ITT7453 output is a logical '1'.

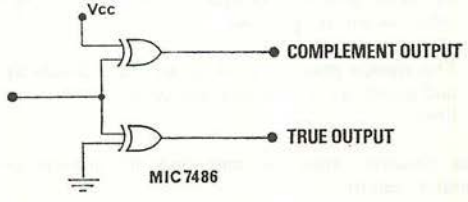
Comparator

This comparator uses the true signal of one number and the complement of the other, it can be conveniently extended to compare two 8 bit numbers. When $A=A^1$, $B=B^1$, $C=C^1$, $D=D^1$, $E=E^1$, $F=F^1$, $G=G^1$, $H=H^1$, the output will be at logical '0'.



20 MHz Phase Splitter

At high frequency it is difficult to produce a complement of a signal with inverse mark space ratio equal to that of the true signal and without phase delay. The circuit shown produces true and complement outputs with one transition of each almost simultaneous. On the other transitions there is up to a 5 ns difference depending to some extent on fan-out loading.



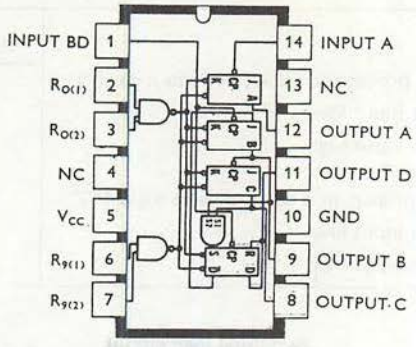
ITT7490
ASYNCHRONOUS DECADE COUNTER

- **Divide by 2**
- **Divide by 5**
- **Divide by 10**
- **BCD or Symmetrical Divide by 10 Count**

TYPICAL CHARACTERISTICS

Propagation delay (ripple delay)	60 ns
Max. clock frequency	18 MHz
Power dissipation (over full count sequence)	135 mW
Input loading factor	
$R_{0(1)}$, $R_{0(2)}$, $R_{9(1)}$, $R_{9(2)}$	1 unit load
Clock A input	2 unit loads
Clock BD input	4 unit loads
Fan-out from each output (Note 1)	10 unit loads
Clock pulse width	50 ns min.
Reset pulse width	50 ns min.

Pin configuration
(top view)



Note 1
For a divide by 10 count, with Pin 12, O/P A, connected to pin 1, I/P BD, the full fan-out is still permissible from O/P A.

DESCRIPTION

The decade counter consists of four master slave flip-flops. Flip-flop 'A' provides a divide-by-2 function. The remaining three flip-flops are internally connected to provide a divide-by-5 counter. Counting occurs on the negative edge of the clock. Inputs $R_{0(1)}$ and $R_{0(2)}$ are gated to provide reset to zero, and inputs $R_{9(1)}$ and $R_{9(2)}$ are gated to provide reset to BCD count of nine. All inputs have input clamping diodes and outputs are standard 7400 series configuration.

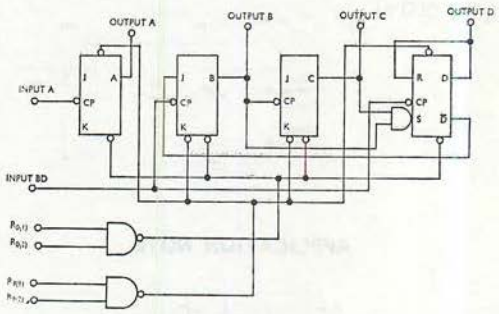
Because output A is not internally connected to the succeeding flip-flops three count modes are available:

1. BCD mode is obtained by externally connecting A output (pin 12) to clock BD input (pin 1).
2. A symmetrical divide by 10 count is obtained by externally connecting D output (pin 11) to clock A input (pin 14).
3. The device may be used as separate divide-by-2 and divide-by-5 counters but with common reset lines.

The counters may be cascaded to provide any number count.

DECADE COUNTER

Logic Diagram



Truth Table

BCD COUNT SEQUENCE

Count	Outputs			
	D	C	B	A
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1

RESET/COUNT

Reset Inputs				Outputs			
$R_{0(1)}$	$R_{0(2)}$	$R_{9(1)}$	$R_{9(2)}$	D	C	B	A
1	1	0	X	0	0	0	0
1	1	X	0	0	0	0	0
0	X	1	1	1	0	0	1
X	0	1	1	1	0	0	1
1	1	1	1	1	0	0	1*
X	0	0	X	Count			
0	X	X	0	Count			
0	X	0	X	Count			
X	0	X	0	Count			

X indicates that logical '1' or logical '0' may be present.

*When resuming the count mode $R_{0(1)}$ or $R_{0(2)}$ must be switched to logical '0' before $R_{9(1)}$ or $R_{9(2)}$ are switched to logical '0' to ensure that the counter remains at BCD count of 9.

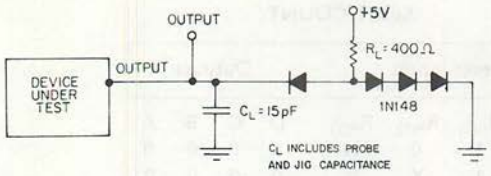
PARAMETER	LIMIT				CONDITIONS	
	Min.	Typ. at 25°C	Max.	Units	V_{CC}	
I_{CCH}						All outputs at 0
						R_0 and R_9 at 0
7490		32	53	mA	Max.	V_{IN} = 5.0V
5490		32	46	mA		
I_{CCL}						BCD count of 7
7490		21	35	mA	Max.	V_{IN} = 5.0V
5490		21	30	mA		

Information on the absolute maximum ratings and the other D.C. characteristics of this device (which are common to other integrated circuits in this series) is stated in the general information section.

SWITCHING CHARACTERISTICS V_{CC}=5.0V, T_{AMB}=25°C

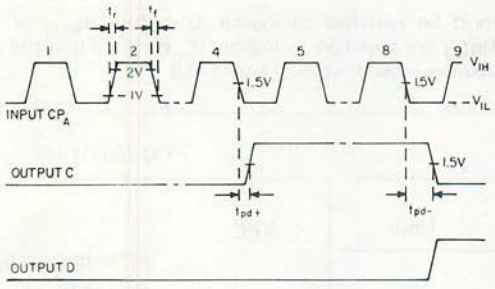
PARAMETER	LIMIT				CONDITIONS
	Min.	Typ.	Max.	Unit	
f_{max}	10	18		MHz	Load circuit on each output
t_{pd+} From input 'A' to output 'C'		60	100	ns	Load circuit on each output
t_{pd-} From input 'A' to output 'C'		60	100	ns	Load circuit on each output

Switching load circuit



Waveforms

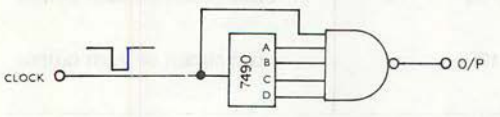
CP_A INPUT PULSE CHARACTERISTICS
Amplitude 3·5 V
tr = 10ns tf = 4 ns
P.R.F. = 1 MHz duty cycle = 50%



APPLICATION NOTES

1. Ripple Delay

In asynchronous counters ripple delay always occurs. It is defined as the time interval between the clock pulse edge at the first stage and the instant a succeeding stage changes state. When decoding the outputs of the counter false outputs can occur at the transitions from an odd count state to an even count state. The false output will always represent a lower count than the true state. When using the counter with decoding the possibility of such false outputs can be prevented by inhibiting the decode gate with the clock signal.

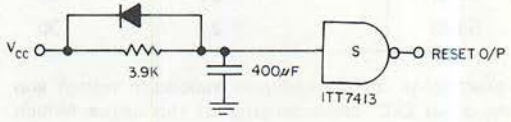


2. Count Range, Less Than Ten

Typically when feeding back outputs signals from the counter by direct connection from outputs to reset inputs $R_{0(1)}$ and $R_{0(2)}$ the counter will reset and start a new count sequence. Feedback can be obtained in this manner from all count states except 7 which will require a three input NAND gate and an inverter in the feedback loop. Under extreme worst case conditions of direct feedback it is possible that not all stages will reset; correct resetting can be ensured by using external gating for all count states. When resetting in either manner the reset count state will be on the outputs for the time it takes for resetting to occur.

3. Illegal Start Up States

On application of supply voltage each flip-flop in a counter may start up in either state. It is, therefore, possible for the counter to assume any one of the 16 possible states. With any type of counter which uses internal gating to restrict the count sequence, the 7490 being no exception, the illegal states (BCD 10 to 15), could be obtained. If this is the case, application of clock pulses will enable the counter to count out of this state, after which normal operation will follow. If, however, it is essential that such conditions are avoided arrangements should be made to provide a reset signal during initial application of supply voltage. A circuit which will generally prove satisfactory is shown below.

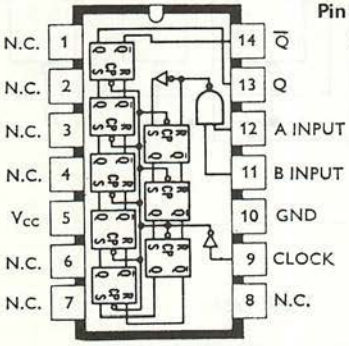


For further details see ITT7413

- **Gated Serial Input**
- **True and Complement Serial Output**

TYPICAL CHARACTERISTICS

Maximum clock frequency	18 MHz
Propagation delay	26 ns
Power dissipation	175 mW
Input loading factor	1 unit load
Fan-out	1 to 10 unit loads
Clock pulse width t_{cp}	25 ns min.
Serial input set up time t_{sp}	25 ns min.
Serial input hold time t_h	0 ns

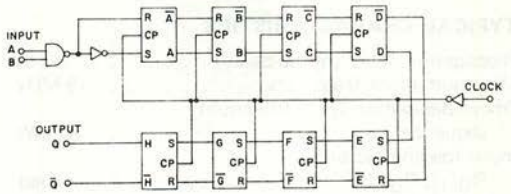


Pin configuration
(top view)

PARAMETER	LIMIT				CONDITIONS
	Min.	Typ.at .25°C	Max.	Units	V_{CC}
I_{CC}					
7491A	35		58	mA	Max. All inputs
5491A	35		50	mA	at logical '0'

Information on the absolute maximum ratings and the other D.C. characteristics of this device (which are common to other integrated circuits in this series) is stated in the general information section.

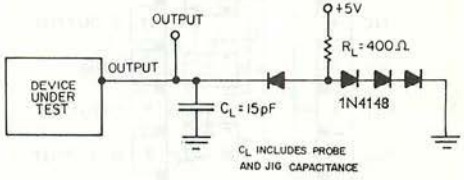
Logic diagram



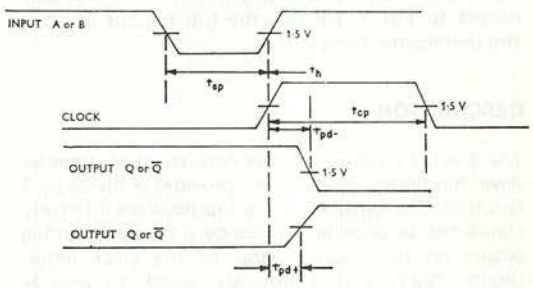
DESCRIPTION

The ITT7491A consists of eight master slave flip-flops connected to form an 8 bit shift register. The last stage has standard TTL outputs for both Q and $\overline{Q}$. Gated serial input function is provided by a 2 input NAND gate and an inverter. The common clock input has an inverting buffer to maintain a fan-in of unity. Information in the register is shifted on the positive edge of the clock. All inputs are provided with input clamping diodes. These registers may be cascaded to form any length of shift register.

Switching load circuit



Waveforms



SWITCHING CHARACTERISTICS, V_{CC} = 5.0 V, T_{AMB} = 25°C

PARAMETER	LIMIT				CONDITIONS
	Min.	Typ.	Max.	Unit	
f_{max}	10	18		MHz	Use switching load circuit on each output
t_{pd+}		24	40	ns	Clock to output
t_{pd-}		27	40	ns	Clock to output

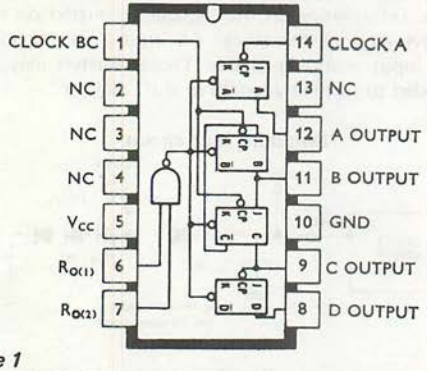
ITT7492
ASYNCHRONOUS DIVIDE BY TWELVE COUNTER

Divide by 2 • Divide by 3 • Divide by 6 • Divide by 12

TYPICAL CHARACTERISTICS

Propagation delay (ripple delay) . . . . . 60 ns
Maximum clock frequency . . . . . 18 MHz
Power dissipation (over full count sequence) . . . . . 124 mW
Input loading factor:
$R_{0(1)}$, $R_{0(2)}$ . . . . . 1 unit load
Clock A input . . . . . 2 unit loads
Clock BC input . . . . . 4 unit loads
Fan-out from each output (Note 1) $\leq$ 10 unit loads
Clock pulse width . . . . . 50 ns min.
Reset pulse width . . . . . 50 ns min.

Pin configuration (top view)



Note 1
For a divide by 12 count, with pin 12, O/P A connected to Pin 1, I/P BC, the full fan-out of 10 is still permissible from O/P A.

DESCRIPTION

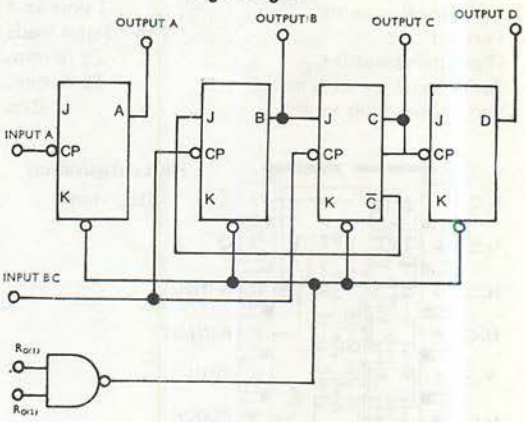
The divide-by-twelve counter consists of four master slave flip-flops. Flip-flop 'A' provides a divide-by-2 function. The remaining three flip-flops are internally connected to provide a divide-by-6 count. Counting occurs on the negative edge of the clock input. Inputs $R_{0(1)}$ and $R_{0(2)}$ are gated to provide reset to zero. All inputs have input clamping diodes and outputs are standard 74 series configuration.

Because output A is not internally connected to the succeeding flip-flops there are two count modes available:

1. Divide-by-twelve mode is obtained by externally connecting A output (pin 12) to clock BC input (pin 1). Outputs A, C and D give simultaneous division by 2, 6 and 12 respectively.
2. The device may be used as separate divide-by-2 and divide-by-6 counters but with common reset lines. Outputs C and D give simultaneous division by 3 and 6 respectively.

The counters may be cascaded to provide any number count.

Logic diagram



Truth Table

COUNT SEQUENCE

Count	Outputs			
	D	C	B	A
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	1	0	0	0
7	1	0	0	1
8	1	0	1	0
9	1	0	1	1
10	1	1	0	0
11	1	1	0	1

RESET/COUNT

To Count:
Either $R_{0(1)}$ or $R_{0(2)}$ or both reset inputs must be at logical '0'.

To Reset:
Both $R_{0(1)}$ and $R_{0(2)}$ must be at logical '1'.

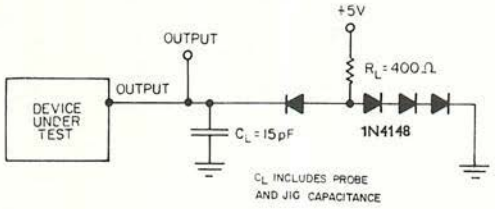
PARAMETER	LIMIT				CONDITIONS	
	Min.	Typ. at 25°C	Max.	Units	V_{CC}	
I_{CCH}						All inputs at 0, R_0 at 0
7492		31	51	mA	Max.	V_{IN} = 5.0 V
5492		31	44	mA		
I_{CCL}						Count of 9 or 11
7492		20		mA	Max.	V_{IN} = 5.0 V
5492		20		mA		

Information on the absolute maximum ratings and the other D.C. characteristics of this device (which are common to other integrated circuits in this series) is stated in the general information section.

SWITCHING CHARACTERISTICS V_{CC}=5.0V, T_{AMB}=25°C

PARAMETER	LIMIT				CONDITIONS
	Min.	Typ.	Max.	Unit	
f_{max}	10	18		MHz	Load circuit on each output
t_{pd+} From input 'A' to output 'D'		60	100	ns	Load circuit on each output
t_{pd-} From input 'A' to output 'D'		60	100	ns	Load circuit on each output

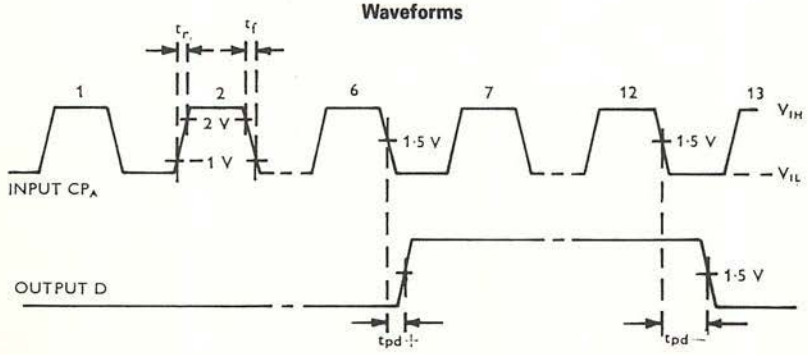
Switching load circuit



CP_A INPUT PULSE CHARACTERISTICS

Amplitude = 3.5 V
t_r = 10 ns
t_f = 4 ns
P.R.F. = 1 MHz
duty cycle = 50%

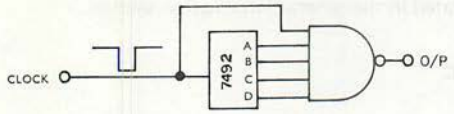
Waveforms



APPLICATION NOTES

1. Ripple Delay

In asynchronous counters ripple delay always occurs. It is defined as the time interval between the clock pulse edge at the first stage and the instant a succeeding stage changes state. When decoding the outputs of the counter, false outputs can occur at the transition from an odd count state to an even count state. The false output will always represent a lower count than the true state. When using the counter with decoding the possibility of such false outputs can be prevented by inhibiting the decode gate with the clock signal.

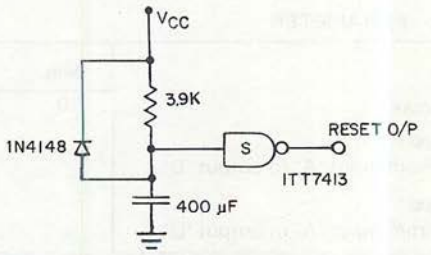


2. Count Range, Less Than Twelve

Typically when feeding back output signals from the counter by direct connection from outputs to reset inputs $R_{0(1)}$ and $R_{0(2)}$ the counter will reset and start a new count sequence. Feedback can be obtained in this manner from all count states except 9 and 11 which will require a three input NAND gate and an inverter as the feedback loop. Under extreme worst case conditions of direct feedback it is possible that not all stages will reset, correct resetting can be ensured by using external gating for all count states. When resetting in either manner the reset count will be on the outputs for the time it takes for resetting to occur.

3. Illegal Start-up States

On application of supply voltage each flip-flop in a counter may start-up in either state. It is, therefore, possible for the counter to assume any one of the 16 possible states. With any type of counter, which uses internal gating to restrict the count sequence, the 7492 being no exception, the illegal states (12 to 15), could be obtained. If this is the case, application of clock pulses will enable the counter to count off this state, after which normal operation will follow. If, however, it is essential that such conditions are avoided arrangements should be made to provide a reset signal during initial applications of supply voltage. A circuit which will generally prove satisfactory is shown below.



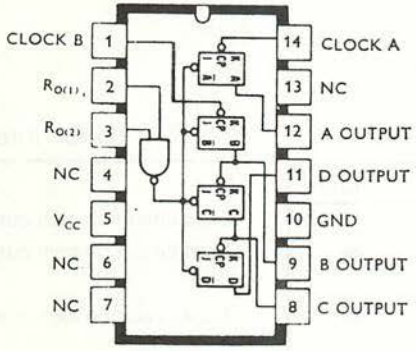
For further details see ITT7413 data sheet.

Divide by 2 ●Divide by 4 ●Divide by 8 ●Divide by 16

TYPICAL CHARACTERISTICS

Propagation delay (ripple delay) . . . . . 75 ns
Maximum clock frequency. . . . . .18 MHz
Power dissipation (over full count sequence). . . . . 120 mW
Input loading factor:
$R_{0(1)}$, $R_{0(2)}$ . . . . . 1 unit load
Clock A and B inputs. . . . . 2 unit loads
Fan-out from each output (Note 1) . . 10 unit loads
Clock pulse width . . . . . 50 ns min.
Reset pulse width . . . . . 50 ns min.

Pin configuration (top view)



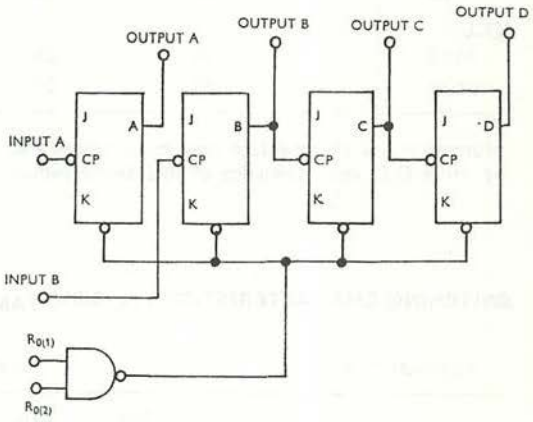
Note 1
For a divide by 16 count, with pin 12, O/P A, connected to pin 1, I/P B, the full fan-out of 10 is still permissible from O/P A.

DESCRIPTION

The 4 bit binary counter consists of four master slave flip-flops. Flip-flop 'A' provides a divide-by-2 function. The remaining three flip-flops are internally connected by provide a divide-by-8 counter. Counting occurs on the negative edge of the clock input. Inputs $R_{0(1)}$ and $R_{0(2)}$ are gated to provide reset to zero. All inputs have input clamping diodes and outputs are standard 74 series configurations.
Because O/P 'A' is not internally connected to the succeeding flip-flops, there are two count modes available:

1. Divide-by-16 mode is obtained by externally connecting A output (Pin 12) to clock B input (pin 1). Outputs A, B, C, and D give simultaneous division by 2, 4, 8 and 16 respectively.
2. The device may be used as separate divide-by-2 and divide-by-8 counters but with common reset lines.

Logic Diagram



Truth Table

COUNT SEQUENCE

Count	Outputs				Count	Outputs			
	D	C	B	A		D	C	B	A
0	0	0	0	0	8	1	0	0	0
1	0	0	0	1	9	1	0	0	1
2	0	0	1	0	10	1	0	1	0
3	0	0	1	1	11	1	0	1	1
4	0	1	0	0	12	1	1	0	0
5	0	1	0	1	13	1	1	0	1
6	0	1	1	0	14	1	1	1	0
7	0	1	1	1	15	1	1	1	1

RESET/COUNT

To Count:
Either $R_{0(1)}$ or $R_{0(2)}$ or both reset inputs must be at logical '0'.

To Reset:
Both $R_{0(1)}$ and $R_{0(2)}$ must be at logical '1'.

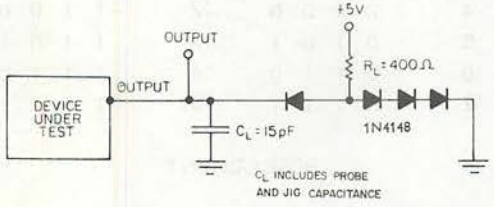
PARAMETER	LIMIT				CONDITIONS	
	Min.	Typ. at 25°C	Max.	Units	V_{CC}	
I_{CCH}						All outputs at 0, R_0 at 0
7493		31	51	mA	Max.	V_{IN} = 50V
5493		31	44	mA		
I_{CCL}						Count of 15
7493		16	25	mA	Max.	V_{IN} - 5.0V
5493		16	22	mA		

Information on the absolute maximum ratings and the other D.C. characteristics of this device (which are common to other integrated circuits in this series) is stated in the general information section.

SWITCHING CHARACTERISTICS V_{CC}=5.0V, T_{AMB}=25°C

PARAMETER	LIMIT				CONDITIONS
	Min.	Typ.	Max.	Unit	
f_{max}	10	18		MHz	Load circuit on each output
t_{pd+} From input 'A' to output 'D'		75	135	ns	Load circuit on each output
t_{pd-} From input 'A' to output 'D'		75	135	ns	Load circuit on each output

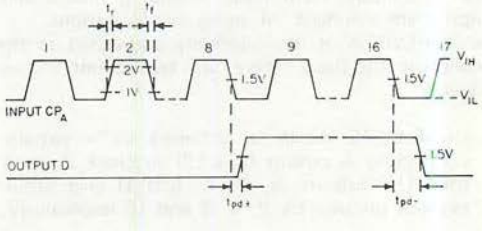
Switching load circuit



Waveforms

CP_A INPUT PULSE CHARACTERISTICS

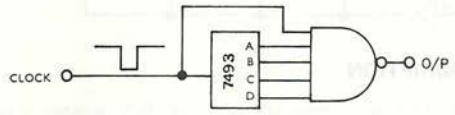
Amplitude = 3.5 V
t_r = 10 ns
t_f = 4 ns
P.R.F. = 1 MHz
duty cycle = 50%



APPLICATION NOTES

1. Ripple Delay

In asynchronous counters ripple delay always occurs. It is defined as the time interval between the clock pulse edge at the first stage and the instant a succeeding stage changes state. When decoding the outputs of the counter false outputs can occur at the transition from an odd state to an even count state. The false output will always represent a lower count than the true state. When using the counter with decoding the possibility of such false outputs can be prevented by inhibiting the decode gate with the clock signal.

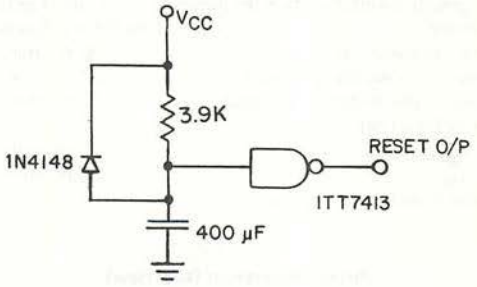


2. Count Range, Less Than Sixteen

Typically when feeding back output signals from the counter by direct connection from outputs to reset inputs $R_{0(1)}$ and $R_{0(2)}$ the counters will reset and start a new count sequence. Feedback can be obtained in this manner from all count states which have codes with only one or two logic '1' states. Others will require a three or four input NAND gate and an inverter as the feedback loop. Under extreme worst case conditions of direct feedback it is possible that not all stages will reset, correct resetting can be ensured by using external gating for all count states. When resetting in either manner the reset count state will be on the outputs for the time it takes for resetting to occur.

3. Illegal Start Up States

On application of supply voltage each flip-flop in a counter may start up in either state. It is, therefore, possible for the counter to assume any one of the 16 possible states. If, however, it is essential that start up conditions give zero count, arrangements should be made to provide a reset signal during initial application of supply voltage. A circuit which will generally prove satisfactory is shown below.



For further details see ITT7413 data sheet.

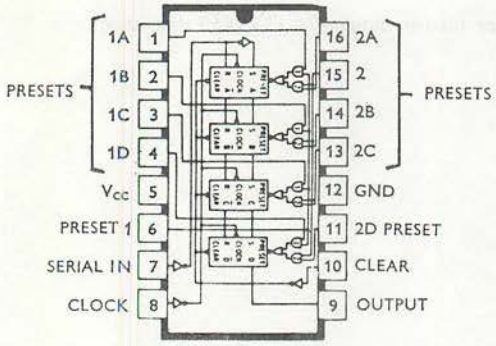
ITT7494
4 BIT SHIFT REGISTER

- **Preset Parallel Input**
- **Parallel or Serial Input**
- **Dual Source Parallel Input with Strobe**
- **Serial Output**
- **Buffered Clear, Clock and Serial Inputs**
- **Dual Source Parallel to Serial Converter**

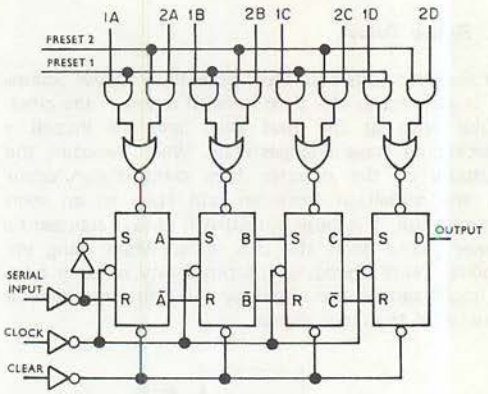
TYPICAL CHARACTERISTICS

Propagation delay . . . . . 25 ns
Power dissipation . . . . . 175 mW
Input loading factor,
all inputs except: preset 1 or 2
(A, B, C, D). . . . . 1 unit load
preset 1 and 2 (common inputs) . . 4 unit loads
Fan-out . . . . . 1 to 10 unit loads
Clock pulse width t_{cp} . . . . . 35 ns, min.
Clear pulse width t_p (clear) . . . . . 30 ns, min.
Preset pulse width t_p (preset) . . . . . 30 ns, min.
Serial input set up time:
t_{sp+} . . . . . 35 ns, min.
t_{sp-} . . . . . 25 ns, min.
Serial input hold time t_h . . . . . 0 ns

Pin configuration (top view)



Logic diagram



DESCRIPTION

The ITT7494 consists of four R-S master slave flip-flops connected to form a four bit shift register. The clock, clear and serial inputs are buffered by four inverters. The two sets of preset inputs 1A to 1D and 2A to 2D are selected by a logical '1' voltage applied to preset 1 and preset 2 inputs respectively, using four AND-OR-INVERT gates. A logical '1' voltage on the preset inputs (1A to 1D or 2A to 2D) will set the flip-flops to a logical '1' state, when selected by the preset 1 or 2 inputs, irrespective of the logic state of the clock, clear and serial inputs. Application of a logical '1' voltage to the clear input will set all four stages to logical '0' state irrespective of the logic state of the clock and serial inputs. Serial shift occurs on the positive edge of the clock, the preset 1 and 2 and clear inputs must all be at logical '0' voltage and the serial input data must be present prior to the clock edge. All inputs have clamping diodes and outputs are standard 74 series configuration.
The registers may be cascaded to provide any length register or any number of bits parallel to serial converter.

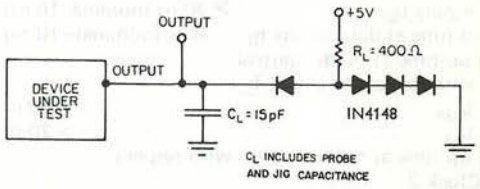
PARAMETER	LIMIT				CONDITIONS	
	Min.	Typ. at 25°C	Max.	Unit	V_{CC}	
I_{CCH}						
7494		35	58	mA	Max.	Preset and clear inputs at logical '0'
5494		35	50	mA		clock and serial inputs at logical '1'
I_{CCL}						
7494		30	50	mA	Max.	All inputs at logical '0'
5494		30	43	mA		

SWITCHING CHARACTERISTICS V_{CC}=5.0V, T_{AMB}=25°C

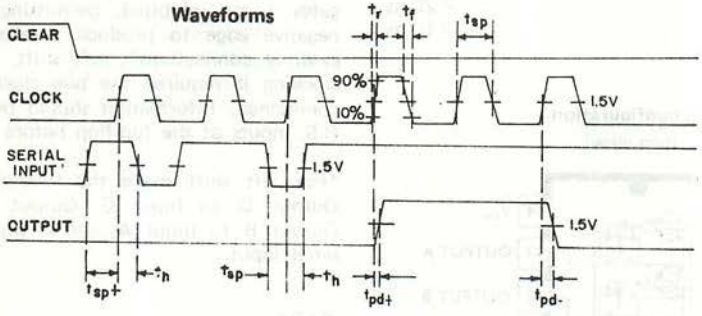
PARAMETER	LIMIT				CONDITIONS
	Min.	Typ.	Max.	Unit	
f_{max}	10			MHz	Use switching load circuit
t_{pd+} propagation delay to logical '1':					
from clock		25	40	ns	Use switching load circuit
from preset			35	ns	
t_{pd-} propagation delay to logical '0':					
from clock		25	40	ns	Use switching load circuit
from preset			40	ns	

Information on the absolute maximum ratings and the other D.C. characteristics of this device (which are common to other integrated circuits in this series) is stated in the general information section.

Switching load circuit



Waveforms



PARALLEL INPUT OPERATION

There are basically two forms of parallel input shift registers. The preset parallel input type such as the ITT7494 and ITT7496, and the clocked parallel input type such as the ITT7495.

The inputs of the preset types are taken to the flip-flop preset inputs via appropriate gating. The application of a logical '1' voltage to the input will set the flip-flop to logical '1' state, but the application of a logical '0' voltage will then have no effect. To set flip-flop to logical '0' state the clear input must be used.

The inputs of the clocked type are taken to the R S flip-flop inputs via appropriate gating. The application of a logical '1' voltage at the input prior to clocking will set the flip-flop to a logical '1' state similarly the application of a logical '0' voltage at the input will set the flip-flop to a logical '0' state.

The clocked parallel input register is, therefore, most suitable for applications where the parallel data is applied for a predetermined time as is the case for the accumulator of a multiplier. The preset parallel input register is more suitable for applications where the input data arrives randomly or is present for a very short time as can be the case in some types of analogue to digital conversion systems.

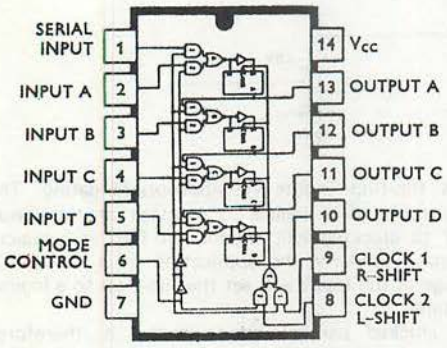
ITT7495
4 BIT SHIFT RIGHT, SHIFT LEFT REGISTER

- **Clocked Parallel Entry**
- **Parallel to Serial Converter**
- **Serial to Parallel Converter**
- **Mode Control with Single or Dual Clock**

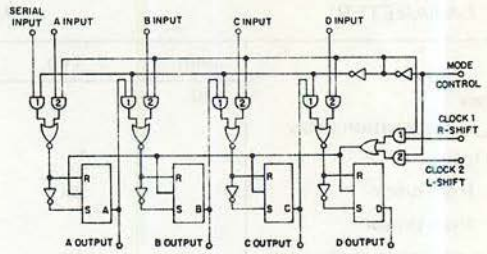
TYPICAL CHARACTERISTICS

Maximum clock frequency	31 MHz
Propagation delay	25 ns
Power dissipation	200 mW
Input loading factor:	
(not mode control)	1 unit load
(mode control)	2 unit loads
Fan-out from each output	10 unit loads
Clock pulse width t_{cp}:	
74 series	> 15 ns (nominal 10 ns)
54 series	> 20 ns (nominal 10 ns)
Set up time at data inputs t_{sp}	> 20 ns (nominal 10 ns)
Hold time at data inputs t_h	.0 ns (nominal–10 ns)
Set up time at mode control with respect to Clock 1	
t_{sp+}	> 10 ns
t_{sp-}	> 20 ns
Set up time at mode control with respect to Clock 2	
t_{sp+}	> 20 ns
t_{sp-}	> 10 ns

Pin configuration
(top view)



Logic diagram



DESCRIPTION

The shift register consists of four master slave flip-flops. The outputs of these flip-flops, the R.S. inputs, the parallel inputs, the mode control and the serial input are all inter-connected by four AND-OR-INVERT gates and six INVERTERS. The two clock inputs are selected by the mode control via an AND-OR gate. When the mode control is at logical '0' it enables AND gates 1 and inhibits AND gate 2, thus permitting clock 1 on a negative edge to produce right shift. When mode control is at logical '1', AND gates 2 are enabled and AND gates 1 are inhibited, permitting clock 2 on a negative edge to produce parallel shift or with external connections*, left shift. If single source clocking is required the two clock inputs can be commoned. Information should be present at the R.S. inputs of the flip-flop before clocking occurs.

*For left shift make the following connections: Output D to Input C, Output C to Input B, Output B to Input A, and D input becomes the serial input.

PARAMETER	LIMITS				CONDITIONS
	Min.	Typ.at 25°C	Max.	Units	V_{CC}
I_{CC}					
7495		40	66	mA	Max.
5495		40	58	mA	

SWITCHING CHARACTERISTICS V_{CC}=5.0V, T_{AMB}=25°C

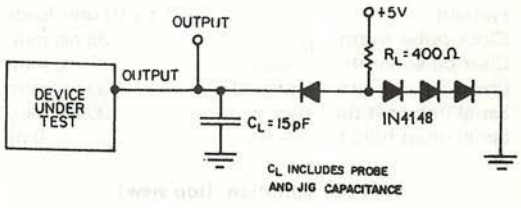
PARAMETER	LIMIT				CONDITIONS
	Min.	Typ. at 25°C	Max.	Unit	
f_{max}	20	31		MHz	Switching load circuit on each output
t_{pd}- propagation delay to logical '1' from either clock		26	35	ns	Switching load circuit on each output
t_{pd}- propagation delay to logical '0' from either clock		24	35	ns	Switching load circuit on each output

Information on the absolute maximum ratings and the other D.C. characteristics of this device (which are common to other integrated circuits in this series) is stated in the general information section.

Clock Pulse Characteristics

t_r = 10 ns; t_f = 4 ns; R.F = 1 MHz; Z_o = 50 Ω; Amplitude - 3.5 V

Switching load circuit



APPLICATION NOTE

Parallel Input Operation

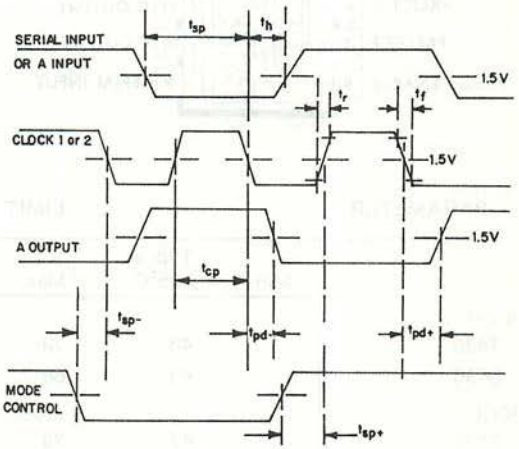
There are basically two forms of parallel input shift registers. The preset parallel input type such as the ITT7494 and ITT7496 and the clocked parallel input type such as the ITT7495.

The inputs of the preset type are connected to the flip-flop preset inputs via appropriate gating. The application of a logical '1' voltage to the input sets the flip-flop to logical '1' state, but the application of a logical '0' voltage then has no effect. To set flip-flops to logical '0' state the clear input must be used.

The inputs of the clocked type are connected to the R.S. flip-flop inputs via appropriate gating. The application of a logical '1' voltage at the input prior to clocking sets the flip-flops to a logical '1' state similarly the application of a logical '0' voltage at the input sets the flip-flops to a logical '0' state.

The clocked parallel input register is, therefore, most suitable for applications where the parallel data is applied for a predetermined time as is the case for the accumulator of a multiplier. The preset parallel input register is more suitable for applications where the input data arrives randomly or is present for a very short time as can be the case in some types of analogue to digital conversion systems.

Waveforms



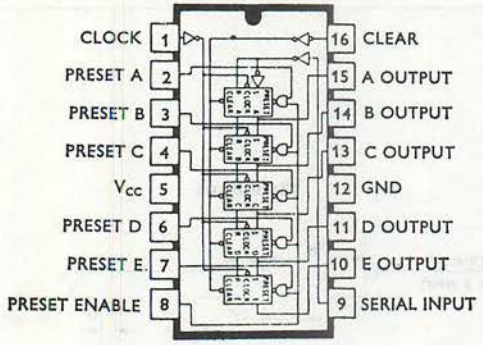
ITT7496
5 BIT SHIFT REGISTER

- **Preset Parallel Input**
- **Parallel or Serial Input**
- **Parallel and Serial Output**
- **Buffered Clear, Clock and Serial Inputs**
- **Serial to Parallel/Parallel to Serial Converter**

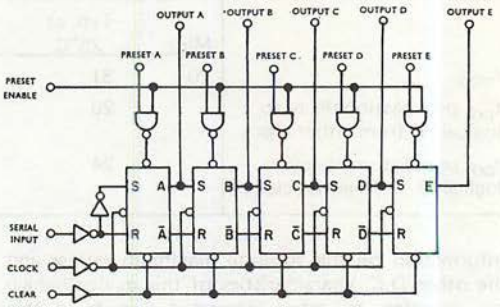
TYPICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

Propagation delay . . . . . 25 ns
Power dissipation . . . . . 215 mW
Input loading factor:
  All inputs except preset . . . . . 1 unit load
  Preset (pin 8) . . . . . 5 unit loads
Fan-out . . . . . 1 to 10 unit loads
Clock pulse width t_{cp} . . . . . 35 ns, min.
Clear pulse width t_p (clear) . . . . . 30 ns, min.
Preset pulse width t_p (preset) . . . . . 30 ns, min.
Serial input set time t_{sp} . . . . . 30 ns, min.
Serial input hold time t_h . . . . . 0 ns

Pin configuration (top view)



Logic Diagram



DESCRIPTION

The ITT7496 consists of five R-S master slave flip-flops connected to form a five bit shift register. The clock, clear and serial inputs are buffered by four inverters. The preset inputs A to E are connected to the flip-flop preset inputs via five two-input NAND gates. The second input of each gate is connected to the common preset input, which when at logical '1' enables all preset inputs. A logical '1' on these inputs sets the flip-flops to the logical '1' state. A logical '1' on the clear input sets all flip-flops to the logical '0' state simultaneously. Right shift in the register occurs on the positive edge of the clock pulse. The serial input data must be present prior to the clock edge. All inputs have clamping diodes and outputs are standard 74 series configuration.
The registers may be cascaded to provide any length of register.

PARAMETER	LIMIT				CONDITIONS	
	Min.	Typ. at 25°C	Max.	Units	V_{CC}	
I_{CCH}						Clock and clear at logical '1'
7496		43	79	mA	Max.	Serial and preset input at logical '0'
5496		43	68	mA		
I_{CCL}						
7496		42	78	mA	Max.	All at 0
5496		42	67	mA		

Information on the absolute maximum ratings and the other D.C. characteristics of this device (which are common to other integrated circuits in this series) is stated in the general information section.

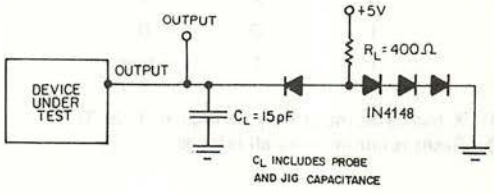
SWITCHING CHARACTERISTICS V_{CC}=5.0V, T_{AMB}=25°C

PARAMETER	LIMIT				CONDITIONS
	Min.	Typ.	Max.	Unit	
f_{max}	10			MHz	Use switching load circuit on each output
t_{pd+}					
Clock to output		25	40	ns	Use switching load circuit
Preset to output			35	ns	on each output
t_{pd-}					
Clock to output		25	40	ns	Use switching load circuit
Clear to output			55	ns	on each output

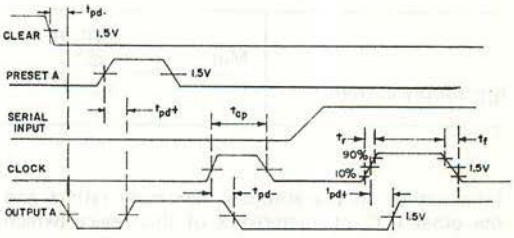
Parallel Input Operation

There are basically two forms of parallel input shift registers. The preset parallel input type such as the ITT7494 and ITT7496 and the clocked parallel input type such as the ITT7495.
The inputs of the preset type are connected to the flip-flop preset inputs via appropriate gating. The application of a logical '1' voltage to the input sets the flip-flop to logical '1' state but the application of a logical '0' voltage then has no effect. To set flip-flops to logical '0' state the clear input must be used.
The inputs of the clocked type are connected to the R-S flip-flop inputs via appropriate gating. The application of a logical '1' voltage at the input prior to clocking sets the flip-flops to a logical '1' state. Similarly the application of a logical '0' voltage at the input sets the flip-flops to a logical '0' state. Hence the clocked parallel register is most suitable for applications where the parallel data is applied for a predetermined time as is the case for the accumulator of a multiplier. The preset parallel input register is more suitable for applications where the input data arrives randomly or is present for a very short time as can be the case in some types of analogue to digital conversion systems.

Switching load circuit



Waveforms

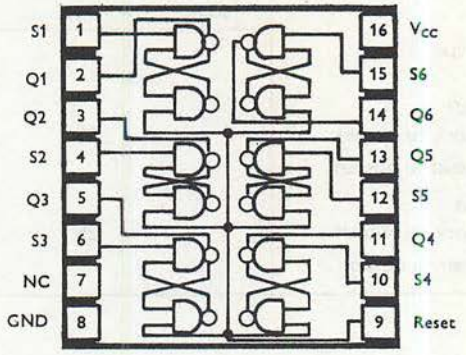


ITT74118
HEX SET-RESET LATCH

TYPICAL CHARACTERISTICS

Power dissipation . . . . . 150 mW
Input loading factor:
Set . . . . . 1 unit load
Reset . . . . . 5 unit loads
Maximum fan-out . . 20 unit loads (high logic level)
10 unit loads (low logic level)
Mean set time . . . . . 14 ns

Pin configuration
(top view)



DESCRIPTION

The ITT74118 consists of six cross coupled NAND gates each forming a simple bistable circuit. A reset line is common to all six latches. Information is stored within a latch when both the set line and the common reset line are held at logical '1'. The state of each bistable can be changed by taking either the set or reset to logical '0' as shown in the truth table.

Truth Table

S	Reset	Q
0	X	1
1	0	0
1	1	Store

1. X Indicates input may be logical '1' or '0'.
2. Reset is common to all latches.

D.C. CHARACTERISTICS

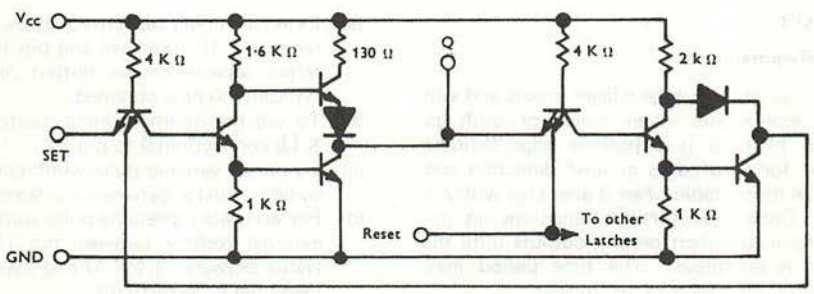
PARAMETER	LIMITS				CONDITIONS
	Min.	Typ. at 25°C	Max.	Units	V_{CC}
I_{CC} supply current		30	60	mA	50% duty cycle

Information on the absolute maximum ratings and the other D.C. characteristics of this device (which are common to other integrated circuits in this series) is stated in the general information section.

SWITCHING CHARACTERISTICS V_{CC}=5V, T_{AMB}=25°C

PROPAGATION DELAY TIME	LIMIT				CONDITIONS
	Min.	Typ.	Max.	Unit	
t_{pd+} to logical '1' level from set		18	29	ns	Fan out = 10
t_{pd-} to logical '0' level from set		10	17	ns	Standard load circuit C_L - 15 pF
t_{pd-} to logical '0' level from reset		18	29	ns	R_L = 400 Ω

Circuit diagram



ITT74121

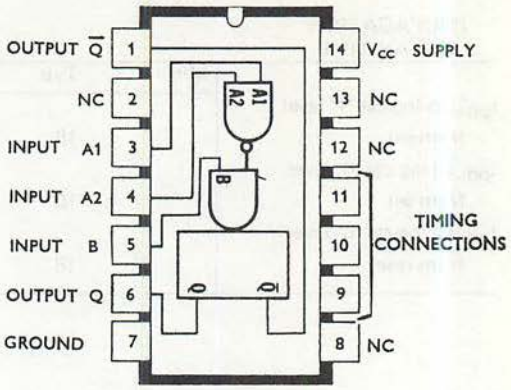
MONOSTABLE MULTIVIBRATOR

Pulse Width 30 ns to 40 s • Schmitt Trigger Input

TYPICAL CHARACTERISTICS

Propagation delay	45 ns
Power dissipation (50% duty cycle)	90 mW
Input loading factor:	
Inputs A_1 and A_2	1 unit load
Input B	2 unit loads
Maximum fan-out	10 unit loads
B input transition time	1 V/s max.
A_1, A_2 input transition time	1 V/μs max.
Input pulse width	50 ns, min.
External timing resistance R_t	1.4 K Ω min.
74 series	40 K Ω max.
54 series	30 K Ω max.
Timing capacitor C_T	1,000 μF max.
Duty cycle:	
R_T = 2 K Ω	67%
R_T = max. value	90%
Output pulse width	0.695 $C_T R_T$

Pin Configuration (top view)



DESCRIPTION

Input Pulse Requirements

A1 and A2 are negative edge trigger inputs and will trigger the monostable when either or both go low with B high. B is a positive edge Schmitt trigger input for slow edges or level detection and will trigger the monostable when B goes high with A1 or A2 low. Once fired further transitions on the inputs will have no effect on the outputs until the time period is completed. The time period may be varied with components as follows:

(a) External timing capacitor may be connected between pin 10 (positive) and pin 11. With no external capacitance an output pulse width of typically 30 ns is obtained.

(b) To use the internal timing resistor (normally 2 K Ω) connect pin 9 to pin 14.

(c) To obtain variable pulse width connect external variable resistor between pins 9 and 14.

(d) For accurate repeatable pulse widths connect an external resistor between pin 11 and pin 14 (value between 1.4 K Ω and maximum value). Leave pin 9 open-circuit.

D.C. CHARACTERISTICS

PARAMETER	LIMIT				CONDITIONS	
	Min.	Typ. at 25°C	Max.	Unit	V_{CC}	
V_{T+} positive edge threshold voltage						
At input A		1.4	2	V	Min.	Note 1
At input B		1.55	2	V	Min.	
V_{T-} negative edge threshold voltage						
At input A	0.8	1.4		V	Min.	Note 1
At input B	0.8	1.35		V	Min.	
I_{CC} supply current						
Quiescent state		13	25	mA	Max.	Note 3
Fired state		23	40	mA	Max.	

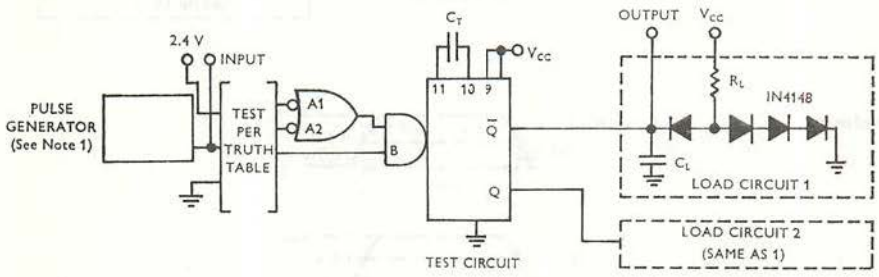
Notes

1. Use external C = 1,000 pF, R = 10 K Ω.
2. To measure I_{SC} on Q ground all inputs Pin 11 and Pin 10. Pin 10 must be grounded last. To measure I_{SC} on $\overline{Q}$ leave Pin 10 and 11 open.
3. Use external C = 1,000 pF; Ground A_1, A_2; Pulse B according to truth table.

SWITCHING CHARACTERISTICS V_{CC}=5.0V, T_{AMB}=25°C

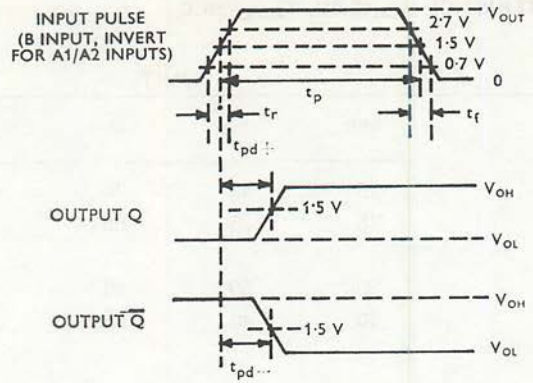
PARAMETER	LIMIT				CONDITIONS
	Min.	Typ.	Max.	Unit	
t_{pd+}					
From A_1 or A_2 to Q	25	45	70	ns	Use test circuit (1)
From B to Q	15	35	55	ns	
t_{pd-}					
From A_1 or A_2 to $\overline{Q}$	30	50	80	ns	Use test circuit (1)
From B to $\overline{Q}$	20	40	65	ns	
t_{po} output pulse width					
R_T = internal					
C_T = 0	20	30	50	ns	Use test circuit (2)
R_T = internal					
C_T = 80 pF	70	110	150	ns	
R_T = 10 K Ω					
C_T = 100 pF	600	700	800	ns	
R_T = 10 K C_T = 1 μF	6	7	8	ms	
t_{min} min. width trigger pulse B input		30	50	ns	Use test circuit (2)

Test circuit (1)

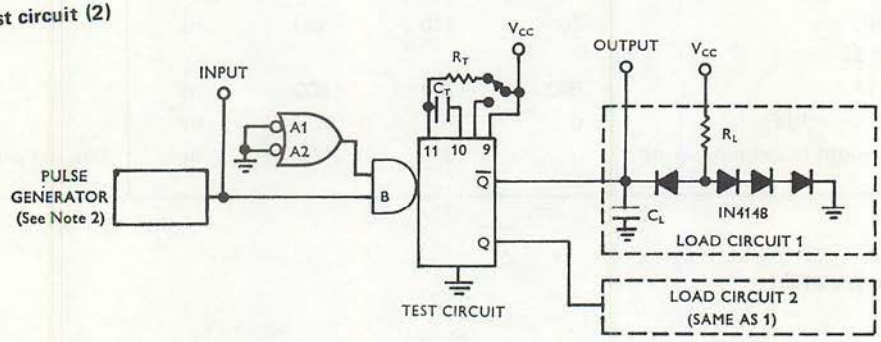


Note 1:
The pulse generator has the following characteristics:
V_{OUT} = 3.5V, t_f = 5 ns, t_r = 10 ns, t_p = 50 ns,
PRF = 1 MHz, and Z_{OUT} = 50 Ω.

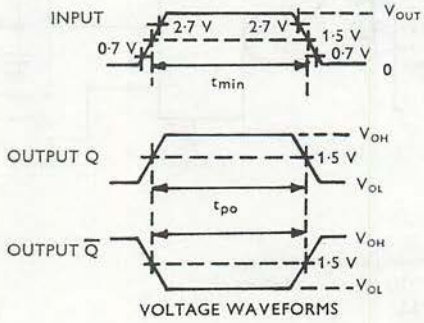
Waveforms



Test circuit (2)



Waveforms



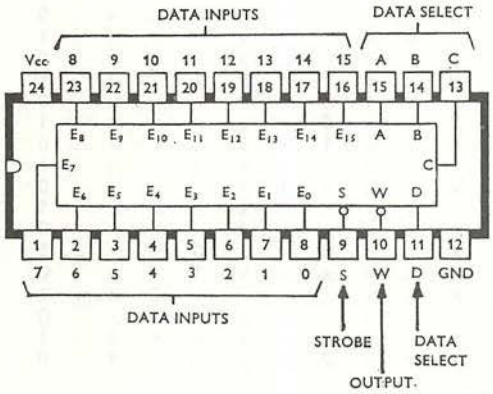
Note 2:
The pulse generator has the following characteristics:
V_{OUT} = 3.5 V, t_f = 5 ns, t_r = 10 ns, $t_p \geq 50$ ns,
PRF = 1 MHz and $Z_{OUT} \approx 50\ \Omega$.

TYPICAL CHARACTERISTICS

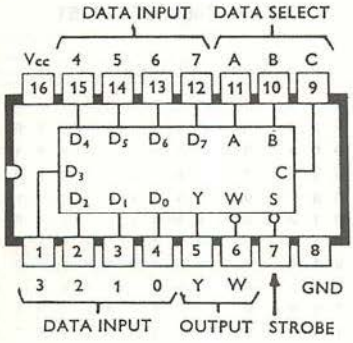
Propagation delay from
data inputs to the output . . . . . 10 ns
Power dissipation:
ITT74150 . . . . . 200 mW
ITT74151 . . . . . 145 mW
Input loading factor . . . . . 1 unit load
Maximum fan-out . . 20 unit loads (high logic level)
10 unit loads (low logic level)

Pin configurations
(top views)

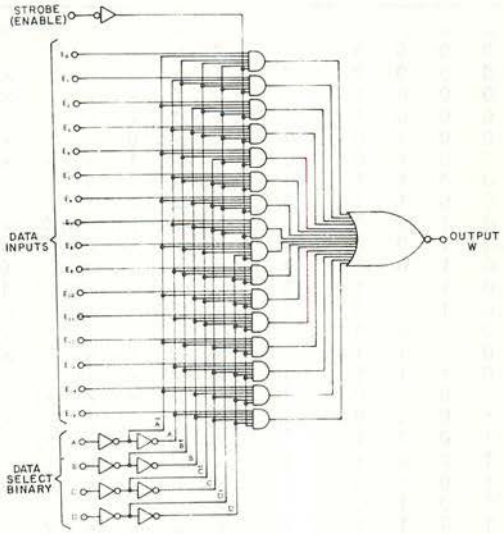
ITT74150



ITT74151



Logic diagram, ITT74150



DESCRIPTION

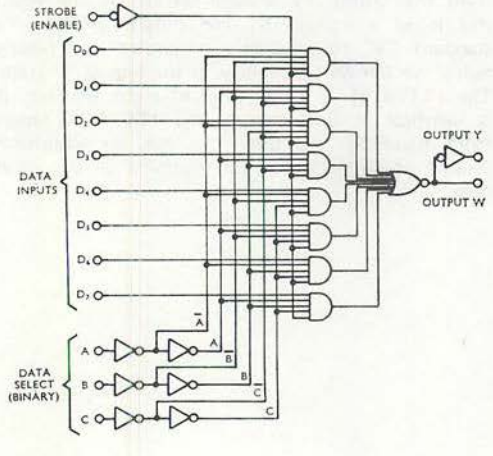
Both circuits convert parallel binary information to a serial form by means of a select signal. The ITT74150 can select one line of sixteen and route this information to the output in the inverted form. Each line is selected by a binary coded number presented to four data select lines. All the information on the data inputs can be inhibited from the output by a common strobe line when this is at a logical '1'. The output circuit is a standard TTL totem pole configuration but having twice the fan out capability in the logical '1' state. The ITT74151 is a one line of eight selector. It is identical in operation to the ITT74150 (apart from handling less bits) but has an additional output which provides non inversion of the input data.

Truth Table, ITT74150

Inputs																			Output
D	C	B	A	Strobe	E_0	E_1	E_2	E_3	E_4	E_5	E_6	E_7	E_8	E_9	E_{10}	E_{11}	E_{12}	E_{13}	E_{14}	E_{15}	W
X	X	X	X	1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	1
0	0	0	0	0	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	1
0	0	0	0	0	1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	0
0	0	0	1	0	X	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	1
0	0	0	1	0	X	1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	0
0	0	1	0	0	X	X	0	X	X	X	X	X	X	X	X	X	X	X	X	X	1
0	0	1	0	0	X	X	1	X	X	X	X	X	X	X	X	X	X	X	X	X	0
0	0	1	1	0	X	X	X	0	X	X	X	X	X	X	X	X	X	X	X	X	1
0	0	1	1	0	X	X	X	1	X	X	X	X	X	X	X	X	X	X	X	X	0
0	1	0	0	0	X	X	X	X	0	X	X	X	X	X	X	X	X	X	X	X	1
0	1	0	0	0	X	X	X	X	1	X	X	X	X	X	X	X	X	X	X	X	0
0	1	0	1	0	X	X	X	X	X	0	X	X	X	X	X	X	X	X	X	X	1
0	1	0	1	0	X	X	X	X	X	1	X	X	X	X	X	X	X	X	X	X	0
0	1	1	0	0	X	X	X	X	X	X	0	X	X	X	X	X	X	X	X	X	1
0	1	1	0	0	X	X	X	X	X	X	1	X	X	X	X	X	X	X	X	X	0
0	1	1	1	0	X	X	X	X	X	X	X	0	X	X	X	X	X	X	X	X	1
0	1	1	1	0	X	X	X	X	X	X	X	1	X	X	X	X	X	X	X	X	0
1	0	0	0	0	X	X	X	X	X	X	X	X	0	X	X	X	X	X	X	X	1
1	0	0	0	0	X	X	X	X	X	X	X	X	1	X	X	X	X	X	X	X	0
1	0	0	1	0	X	X	X	X	X	X	X	X	X	0	X	X	X	X	X	X	1
1	0	0	1	0	X	X	X	X	X	X	X	X	X	1	X	X	X	X	X	X	0
1	0	1	0	0	X	X	X	X	X	X	X	X	X	X	0	X	X	X	X	X	1
1	0	1	0	0	X	X	X	X	X	X	X	X	X	X	1	X	X	X	X	X	0
1	0	1	1	0	X	X	X	X	X	X	X	X	X	X	X	0	X	X	X	X	1
1	0	1	1	0	X	X	X	X	X	X	X	X	X	X	X	1	X	X	X	X	0
1	1	0	0	0	X	X	X	X	X	X	X	X	X	X	X	X	0	X	X	X	1
1	1	0	0	0	X	X	X	X	X	X	X	X	X	X	X	X	1	X	X	X	0
1	1	0	1	0	X	X	X	X	X	X	X	X	X	X	X	X	X	0	X	X	1
1	1	0	1	0	X	X	X	X	X	X	X	X	X	X	X	X	X	1	X	X	0
1	1	1	0	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	0	X	1
1	1	1	0	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	1	X	0
1	1	1	1	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	0	1
1	1	1	1	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	1	0

When used to indicate an input condition, X = Logical '1' or Logical '0'

Logic diagram, ITT74151



Truth Table, ITT74151

Inputs												Outputs	
C	B	A	Strobe	D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7	Y	W
X	X	X	1	X	X	X	X	X	X	X	X	0	1
0	0	0	0	0	X	X	X	X	X	X	X	0	1
0	0	0	0	1	X	X	X	X	X	X	X	1	0
0	0	1	0	X	0	X	X	X	X	X	X	0	1
0	0	1	0	X	1	X	X	X	X	X	X	1	0
0	1	0	0	X	X	0	X	X	X	X	X	0	1
0	1	0	0	X	X	1	X	X	X	X	X	1	0
0	1	1	0	X	X	X	0	X	X	X	X	0	1
0	1	1	0	X	X	X	1	X	X	X	X	1	0
1	0	0	0	X	X	X	X	0	X	X	X	0	1
1	0	0	0	X	X	X	X	1	X	X	X	1	0
1	0	1	0	X	X	X	X	X	0	X	X	0	1
1	0	1	0	X	X	X	X	X	1	X	X	1	0
1	1	0	0	X	X	X	X	X	X	0	X	0	1
1	1	0	0	X	X	X	X	X	X	1	X	1	0
1	1	1	0	X	X	X	X	X	X	X	0	0	1
1	1	1	0	X	X	X	X	X	X	X	1	1	0

D.C. CHARACTERISTICS

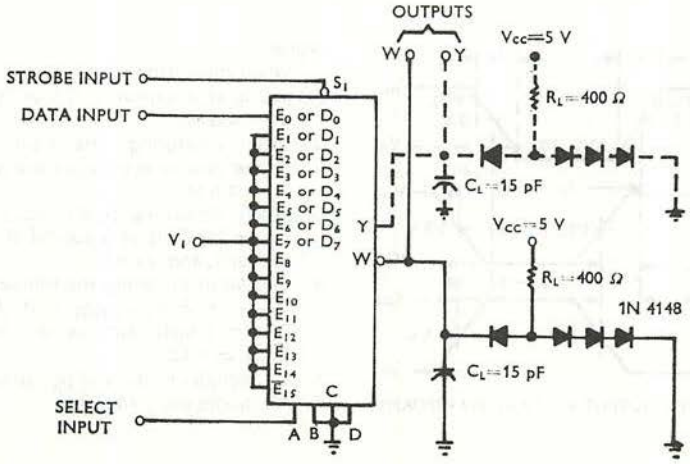
PARAMETER		LIMITS				CONDITIONS	
		Min.	Typ. at 25°C	Max.	Units	V_{CC}	
I_{CCH}	ITT74150		40	68	mA	Max.	V_{strobe} = 0 V, V_{IN} = 4.5 V
	ITT74151		29	48	mA	Max.	(All data inputs logical '1')
I_{CCL}	ITT74150		35	60	mA	Max.	V_{IN} = 0
	ITT74151		22	38	mA	Max.	(All data inputs logical '0')

Information on the absolute maximum ratings and the other D.C. characteristics of these devices (which are common to other integrated circuits in this series) is stated in the general information section.

SWITCHING CHARACTERISTICS V_{CC}=5V, T_{AMB}=25°C, FOR THE ITT74150

PARAMETER			LIMITS				CONDITIONS
	From	To	Min.	Typ.	Max.	Units	
t_{pd+}	A, B, C, or D	W		23	35	ns	V_{CC} = 5V See test circuit
t_{pd-}	A, B, C, or D	W		22	33	ns	V_{CC} = 5V See test circuit
t_{pd+}	Strobe	W		15.5	24	ns	V_{CC} = 5V See test circuit
t_{pd-}	Strobe	W		21	30	ns	V_{CC} = 5V See test circuit
t_{pd+}	E_0 to E_{15}	W		13	20	ns	V_{CC} = 5V See test circuit
t_{pd-}	E_0 to E_{15}	W		8.5	14	ns	V_{CC} = 5V See test circuit

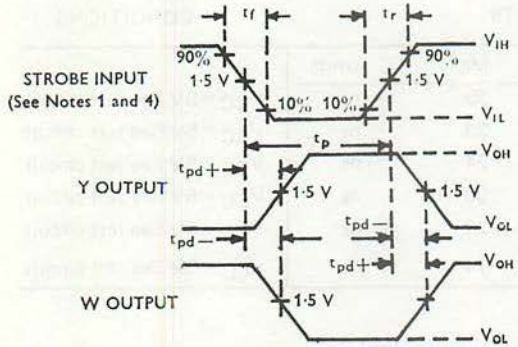
Test circuit for ITT74150 and ITT74151



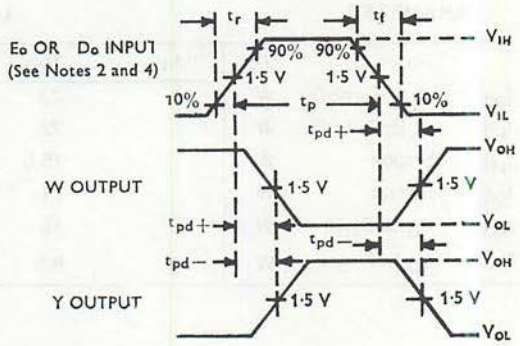
SWITCHING CHARACTERISTICS V_{CC}=5V, T_{AMB}=25°C, FOR THE ITT74151

PARAMETER			LIMITS				CONDITIONS
	From	To	Min.	Typ.	Max.	Units	
t_{pd+}	A, B or C	Y		35	52	ns	V_{CC}=5.0V See test circuit
t_{pd-}	A, B or C	Y		20	30	ns	V_{CC}=5.0V See test circuit
t_{pd+}	Strobe	Y		35	52	ns	V_{CC}=5.0V See test circuit
t_{pd-}	Strobe	Y		19	30	ns	V_{CC}=5.0V See test circuit
t_{pd+}	D_0 to D_7	Y		19	29	ns	V_{CC}=5.0V See test circuit
t_{pd-}	D_0 to D_7	Y		16	24	ns	V_{CC}=5.0V See test circuit

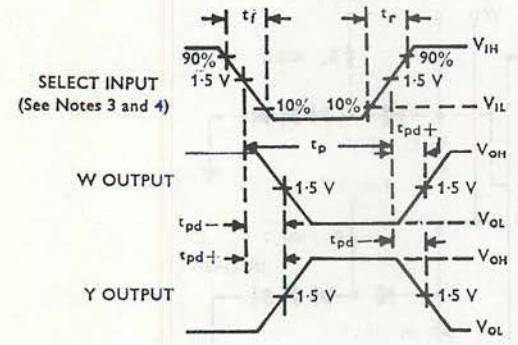
Waveforms for ITT74150 and ITT74151



STROBE-TO-OUTPUT VOLTAGE WAVEFORMS



DATA INPUT-TO-OUTPUT VOLTAGE WAVEFORMS



SELECT INPUT-TO-OUTPUT VOLTAGE WAVEFORMS

Notes:

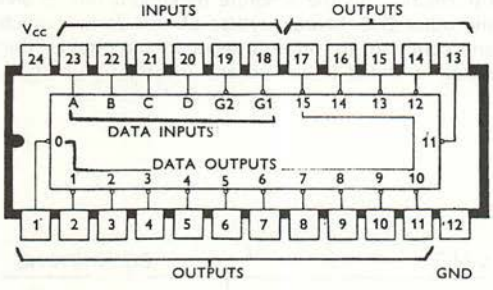
1. When measuring strobe to output times select input is at a logical 0, E_0 or D_0 is at a logical 1, V_1 = 4.5 V.
2. When measuring data input to output times strobe and select inputs are at a logical 0, and V_1 = 4.5 V.
3. When measuring select input to output times strobe input is at a logical 0, data input is at a logical 1, and V_1 = 0.
4. The input pulse has the following characteristics: $V_{in(1)}$ = 3 V, $V_{in(0)}$ = 0 V. t_r = t_f = 10 ns, PRF = 1 MHz, duty cycle = 50%, and generator $Z_{out} \approx 5\ \Omega$
5. C_L includes probe and jig capacitance
6. All diodes are 1N4148

- **4-Line-to-16-Line Decoder**
- **Demultiplexing Capability**

TYPICAL CHARACTERISTICS

Propagation delay (through 3 levels of logic)	23 ns
Power dissipation	170 mW
Input loading factor	1 unit load
Maximum fan-out	10 unit loads (low state)
	20 unit loads (high state)

Pin configurations
(top view)



DESCRIPTION

The ITT74154 can be used as a 4-line-to-16-line decoder or a 1-line-to-16-line demultiplexer.

In use as a decoder, one of the 16 output NAND gates assumes its low state when enabled by the strobe inputs G_1, G_2, and the appropriate binary combination from the four binary-coded inputs A, B, C and D.

The output gates are inhibited by a high strobe input. Therefore to demultiplex, data is entered on a strobe input with the other strobe input low and the four other inputs addressing the appropriate data output line.

The most significant input, D, produces a useful inhibit function when the ITT74154 is used as a 1-line-to-8-line demultiplexer or a 4-line to 8-line decoder.

Be selecting appropriate outputs, any BCD code can be decoded using a ITT74154 element. See truth table and application note for further details.

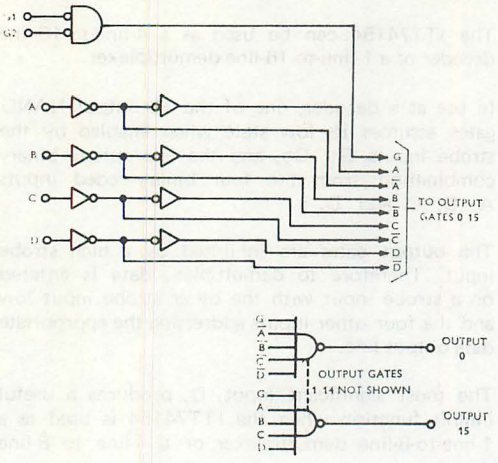
Buffers are incorporated on the inputs to reduce input loading.

Truth Table

INPUTS						OUTPUTS															
G1	G2	D	C	B	A	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
L	L	L	L	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	H	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	H	L	L	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H
L	L	L	H	L	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H
L	L	L	H	H	L	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H
L	L	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H
L	L	H	L	L	L	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H
L	L	H	L	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H
L	L	H	L	H	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H
L	L	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H
L	L	H	H	L	L	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H
L	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H
L	L	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H
L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L
L	H	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
H	L	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
H	H	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H

H=high, L=low, X=irrelevant

Logic diagram



PARAMETER	LIMIT				CONDITIONS
	Min.	Typ.at 25°C	Max.	Unit	V_{CC}
I_{CC}					
74154		34	56	mA	Max.
54154		34	49	mA	Max.

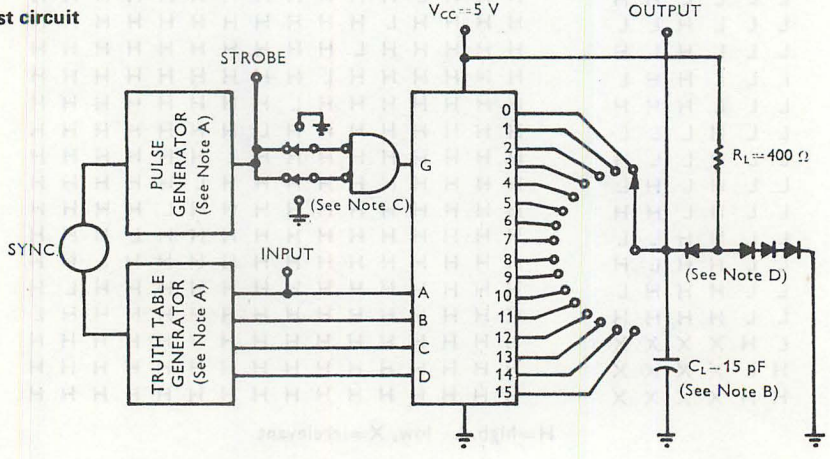
For $-I_{SC}$ maximum limit = 57 mA, for 74154

Information on the absolute maximum ratings and the other D.C. characteristics of this device (which are common to other integrated circuits in this series) is stated in the general information section.

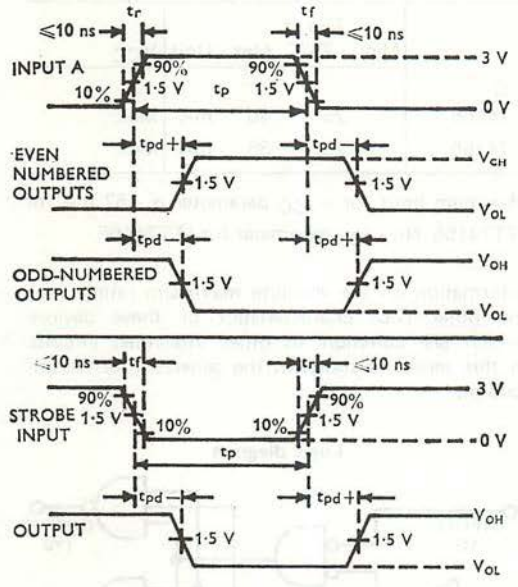
SWITCHING CHARACTERISTICS V_{CC}=5V, T_A=25°C

PARAMETER	LIMIT				CONDITIONS
	Min.	Typ.	Max.	Unit	
t_{pd+} from A, B, C, or D inputs through 3 levels of logic		24	36	ns	SEE TEST CIRCUIT
t_{pd-} from A, B, C, or D inputs through 3 levels of logic		22	33	ns	
t_{pd+} from either strobe input		20	30	ns	
t_{pd-} from either strobe input		18	27	ns	

Test circuit



Waveforms



Notes:

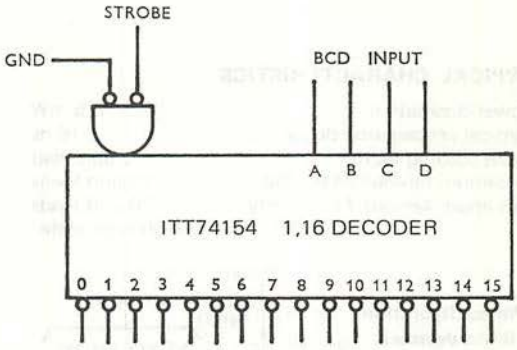
A. The truth table generator and the pulse generator have the following characteristics: P.R.F.=1 MHz, Z_{out}=50 Ω, t_p=100 ns.

B. C_L includes probe and jig capacitance.

C. When measuring select input to output times the strobe inputs are grounded. When measuring strobe input to output times, the untested strobe input is grounded. Select inputs determining output under test through truth table generator.

D. All diodes are 1N4149.

APPLICATION NOTE



Output Selection BCD Code

Decimal Digit	8421	5421	Excess 3	Gray
0	0	0	3	0
1	1	1	4	1
2	2	2	5	3
3	3	3	6	2
4	4	4	7	6
5	5	8	8	7
6	6	9	9	5
7	7	10	10	4
8	8	11	11	12
9	9	12	12	13

DECODE ANY BCD CODE

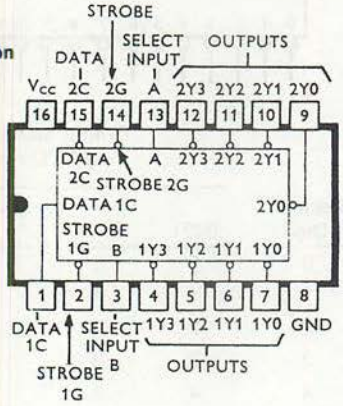
Decode any BCD code using a 74154 element. Any 4 bit BCD code may be decoded by selecting outputs, examples are shown in the table.

TYPICAL CHARACTERISTICS

Power dissipation . . . . . 125 mW
Typical propagation delay . . . . . 16 ns
Input loading factor . . . . . 1 unit load
Maximum fan-out 74155/56 . . . . . 10 unit loads
Maximum fan-out 74155 only . . . . . 20 unit loads
(high logic state)

Pin configuration (both devices)

(top view)



DESCRIPTION

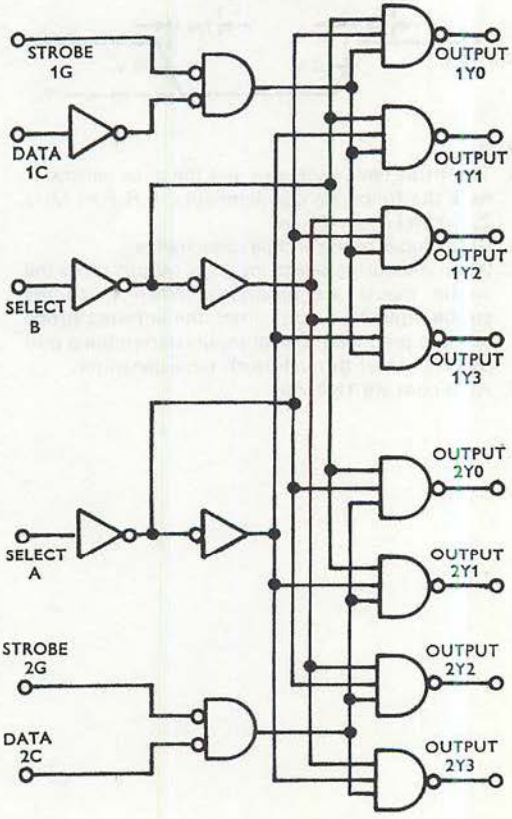
Both ITT74155 and ITT74156 have the same logic function. They can either be connected as a 2-line-to-4-line decoder using the select inputs. A and B, or as a 3-line-to-8-line decoder by using inputs A, B, and a common shorted connection 1C to 2C. The outputs only respond to the data select inputs when either the strobe and/or data inputs go from logical '1' to '0'. In which case the appropriate output will change from logical '1' to '0'.
If the data is applied to strobe/data inputs, the select inputs address the data to the appropriate output. Both devices form either a dual 1-line-to-4-line demultiplexer with common address input or a 1-line-to-8-line demultiplexer.
When using this device it should be noticed that the two functional halves of this circuit are logically coupled from the select inputs, but are independent from the strobe or data inputs.
The ITT74155 has totem pole outputs, while the ITT74156 has standard open collector outputs, so that several circuits can be easily 'Wired-ORed' for demultiplexing from more lines.
See truth tables for more detailed operation of these devices.

PARAMETER	LIMIT				CONDITIONS
	Min.	Typ.at 25°C	Max.	Unit	V_{CC}
I_{CC}					
74155		25	40	mA	Max.
74156		25	35	mA	Max.

Maximum limit for $-I_{SC}$ parameter is –57 mA for ITT74155. No $-I_{SC}$ parameter for ITT74156.

Information on the absolute maximum ratings and the other D.C. characteristics of these devices (which are common to other integrated circuits in this series) is stated in the general information section.

Logic diagram



SWITCHING CHARACTERISTICS V_{CC}=5V, T_A=25°C

PARAMETER			LIMIT				CONDITIONS
	From input	To output	Min.	Typ. at 25°C	Max.	Unit	
t_{pd+}	A, B, 2C						
74155	1G or	Y		13	20	ns	
74156	2G			15	23	ns	
t_{pd-}	A, B, 2C						
74155	1G or	Y		18	27	ns	
74156	2G			20	30	ns	
t_{pd+}							
74155	A or B	Y		21	32	ns	INPUTS
74156				23	34	ns	AS PER
t_{pd-}							TRUTH
74155	A or B	Y		21	32	ns	TABLE
74156				23	34	ns	
t_{pd+}							
74155	1C	Y		16	24	ns	
74156				18	27	ns	
t_{pd-}							
74155	1C	Y		20	30	ns	
74156				22	33	ns	

Truth Tables

(X = Don't Care, H = Logical 1 State, L = Logical 0 State)

(A) 2-4 Line Decoder or 1-4 Line Demultiplexer

2G = X, 2C = X

INPUTS				OUTPUTS			
Select		Strobe	Data				
B	A	1G	1C	1Y0	1Y1	1Y2	1Y3
X	X	H	X	H	H	H	H
L	L	L	H	L	H	H	H
L	H	L	H	H	L	H	H
H	L	L	H	H	H	L	H
H	H	L	H	H	H	H	L
X	X	X	L	H	H	H	H

1G = X, 1C = X

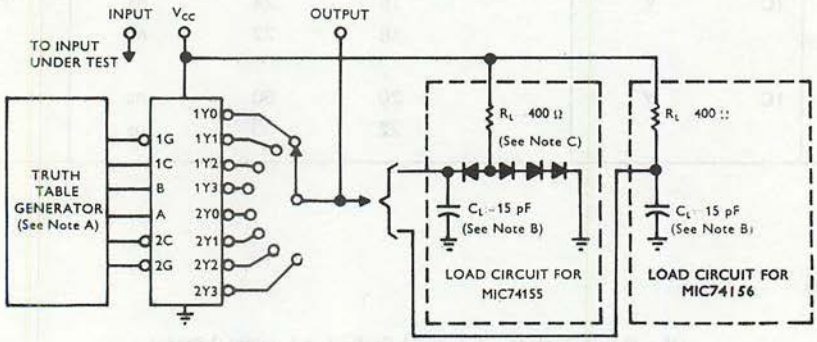
INPUTS				OUTPUTS			
Select		Strobe	Data				
B	A	2G	2C	2Y0	2Y1	2Y2	2Y3
X	X	H	X	H	H	H	H
L	L	L	L	L	H	H	H
L	H	L	L	H	L	H	H
H	L	L	L	H	H	L	H
H	H	L	L	H	H	H	L
X	X	X	H	H	H	H	H

(B) 3-8 Line Decoder or 1-8 Line Demultiplexer

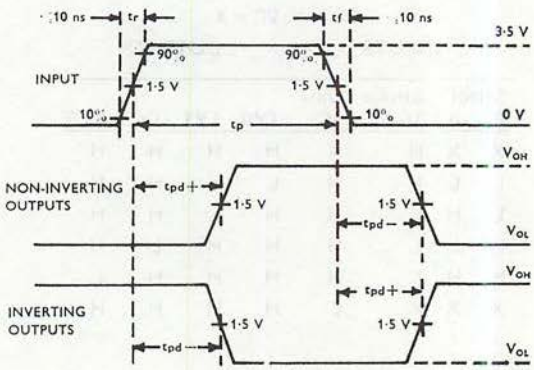
INPUTS				OUTPUTS							
Select			Strobe or Data	(0)	(1)	(2)	(3)	(4)	(5)	(6)	(7)
C*	B	A	G†	2Y0	2Y1	2Y2	2Y3	1Y0	1Y1	1Y2	1Y3
X	X	X	H	H	H	H	H	H	H	H	H
L	L	L	L	L	H	H	H	H	H	H	H
L	L	H	L	H	L	H	H	H	H	H	H
L	H	L	L	H	H	L	H	H	H	H	H
L	H	H	L	H	H	H	L	H	H	H	H
H	L	L	L	H	H	H	H	L	H	H	H
H	L	H	L	H	H	H	H	H	L	H	H
H	H	L	L	H	H	H	H	H	H	L	H
H	H	H	L	H	H	H	H	H	H	H	L

*Connect inputs 1C and 2C together.
†Connect inputs 1G and 2G together.

Test Circuit



Waveforms



NOTES:
A. The truth table generator has the following characteristics: PRF = 1 MHz, $Z_{out} \approx 50\ \Omega$, tp = 100 ns.
B. C_L includes probe and jig capacitance.
C. All diodes are IN4149.

TYPICAL CHARACTERISTICS

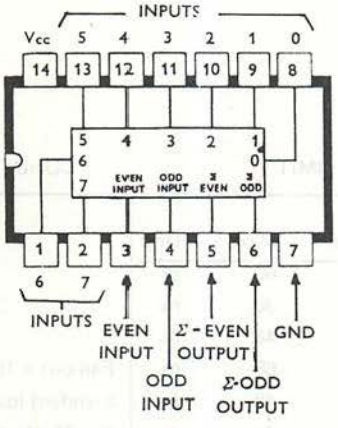
Propagation delay (depending upon input states) . . . . . 36 ns
Power dissipation . . . . . 170 mW
Input loading factor:
Data inputs . . . . . 1 unit load
Odd or even inputs . . . . . 2 unit loads
Maximum fan-out . . 20 unit loads (high logic state)
10 unit loads (low logic state)

Truth Table

INPUTS			OUTPUTS	
Σ OF 1's AT 0 THRU 7	EVEN	ODD	Σ EVEN	Σ ODD
EVEN	1	0	1	0
ODD	11	0	0	1
EVEN	0	1	0	1
ODD	0	1	1	0
X	1	1	0	0
X	0	0	1	1

X = 'Don't care'

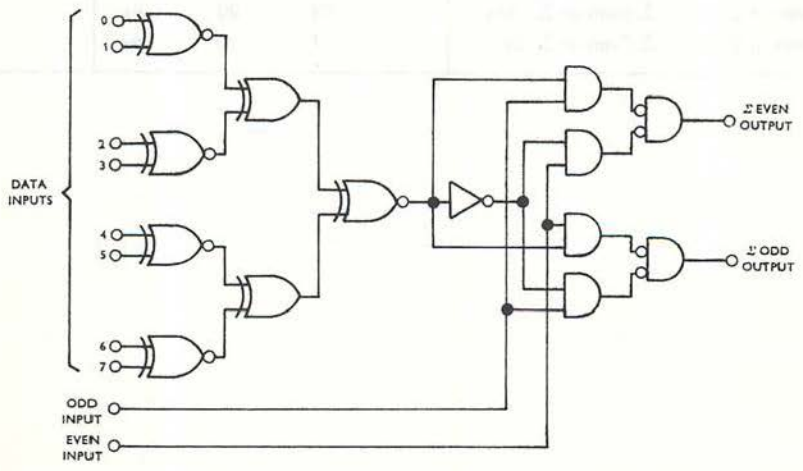
Pin configuration
(top view)



DESCRIPTION

This device is specifically designed for error checking systems. The ITT74180 sums the 8 bits of binary information at the data inputs and gives outputs depending upon whether the sum is even or odd. Additional inputs 'even' and 'odd' can reverse the sense of the summing and also enables the ITT74180 to be cascaded to increase the word length of the data.

Logic diagram

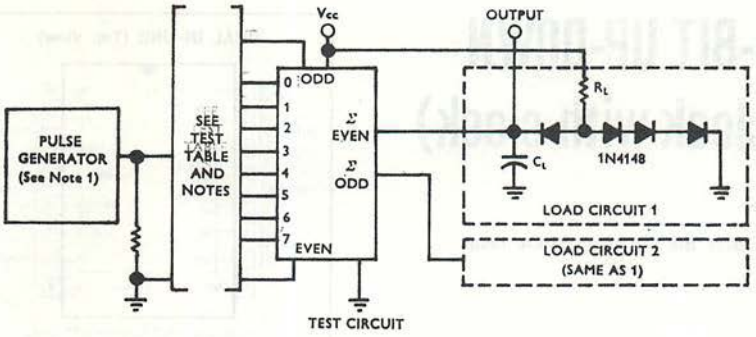


PARAMETER	LIMIT				CONDITIONS	
	Min.	Typ. at 25°C	Max.	Unit	V_{CC}	
I_{CC} supply current						
74 series		34	56	mA	Max.	Data input open with
54 series		34	49	mA	Max.	even and odd inputs both zero or both 2.4V

Information on the absolute maximum ratings and the other D.C. characteristics of this device (which are common to other integrated circuits in this series) is stated in the general information section.

SWITCHING CHARACTERISTICS V_{CC}=5V, T_{AMB}=25°C

PROPAGATION DELAY TIME			LIMIT				CONDITIONS
	From (input)	To (output)	Min.	Typ.	Max.	Unit	
t_{pd+}	Data	Σ Even		40	60	ns	
t_{pd-}	Data	Σ Even		25	38	ns	
t_{pd+}	Data	Σ Odd		32	48	ns	
t_{pd-}	Data	Σ Odd		45	68	ns	Fan-out = 10
t_{pd+}	Data	Σ Even		32	48	ns	Standard load circuit
t_{pd-}	Data	Σ Even		45	68	ns	C_L=15 pF, R_L=
t_{pd+}	Data	Σ Odd		40	60	ns	400 Ω and see test
t_{pd-}	Data	Σ Odd		25	38	ns	table
t_{pd+}	Even or Odd	Σ Even or Σ Odd		13	20	ns	
t_{pd-}	Even or Odd	Σ Even or Σ Odd		7	10	ns	

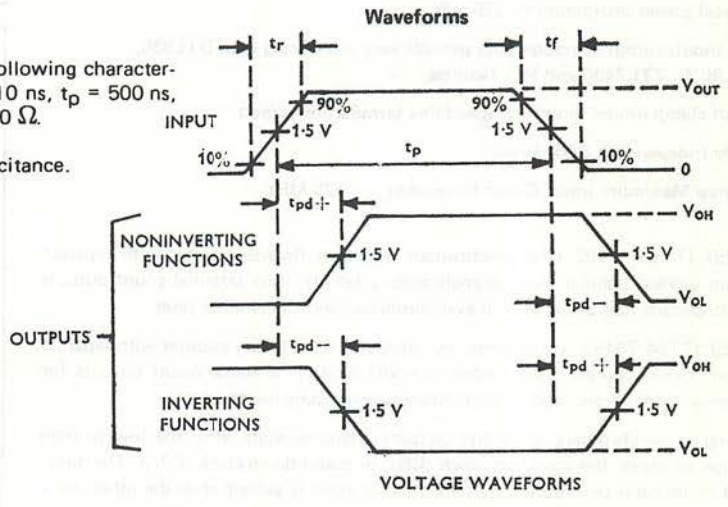


Switching load circuit

NOTES:

1. The pulse generator has the following characteristics: V_{OUT} = 3V, $t_r = t_f$ = 10 ns, t_p = 500 ns, PRF = 1 MHz, and Z_{OUT} 50 Ω.
2. Inputs not specified are open.
3. C_L includes probe and jig capacitance.

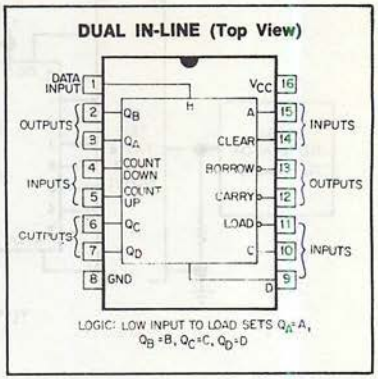
Waveforms

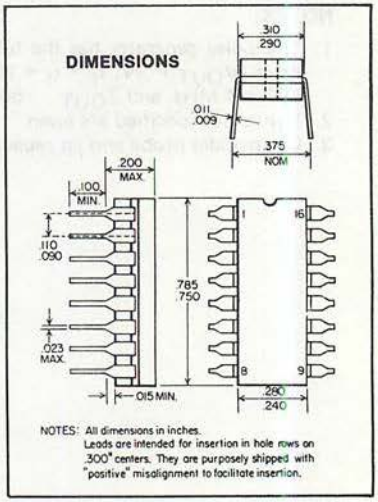


Test Table

INPUT PULSE	CONDITIONS GND	OUTPUT TESTED	INPUT PULSE	CONDITIONS GND	OUTPUT TESTED
0	ODD	ΣEVEN	2	ODD	ΣODD
1	ODD	ΣEVEN	3	ODD	ΣODD
2	ODD	ΣEVEN	4	ODD	ΣODD
3	ODD	ΣEVEN	5	ODD	ΣODD
4	ODD	ΣEVEN	6	ODD	ΣODD
5	ODD	ΣEVEN	7	ODD	ΣODD
6	ODD	ΣEVEN	EVEN	NONE	ΣEVEN
7	ODD	ΣEVEN	ODD	0	ΣEVEN
0	ODD	ΣODD	EVEN	0	ΣODD
1	ODD	ΣODD	ODD	NONE	ΣODD

SYNCHRONOUS 4-BIT UP-DOWN COUNTER (dual clock with clock)





- **Cascading Circuitry Provided Internally**
- **Guaranteed fanout of 10 TTL loads over the full temperature range and supply voltage ranges.**
- **High capacitive drive capability.**
- **Individual Preset to Each Flip Flop.**
- **Typical power dissipation of 325 mW**
- **The input/output characteristics provide easy interfacing with DTL930, TTL9000, TTL7400 and MSI families.**
- **Input clamp diodes limit high speed line termination effects**
- **Fully Independent Clear Input**
- **Typical Maximum Input Count Frequency . . . . 25 MHz**

The MSI ITT54/74192 is a synchronous up/down decade counter with separate up/down clocks, parallel load (asynchronous) facility, two terminal count outputs for multi-decade operation, and an asynchronous overriding master reset.

The MSI ITT54/74193 is a synchronous up/down 4-bit binary counter with separate up/down clocks, parallel load (asynchronous) facility, terminal count outputs for multi-decade operations, and an asynchronous overriding master reset.

Counting is synchronous, with the outputs changing state after the low to high transition of either the count-up clock (CPu) or count-down clock (CP_D). The direction of counting is determined by which clock input is pulsed while the other clock input is high. (Incorrect counting will occur if both the count-up clock and count-down clock inputs are pulsed simultaneously.) The counter will respond to a clock pulse on either input by changing to the next appropriate state of a binary sequence.

The counter has a parallel load (asynchronous) facility which permits the counter to be reset. Whenever the data enable ($\overline{PL}$) input is low, the information present on the parallel data inputs (P_A, P_B, P_C, P_D,) will be loaded into the counter and appear on the outputs independent of the conditions of the clock inputs. When the data enable input goes lows, this information is stored in the counter and when the counter is clocked it changes to the next appropriate state in the counts sequence. The data inputs are inhibited when the data enable is high and have no effect on the counter.

The terminal count-up ($\overline{TC_U}$) and terminal count-down ($\overline{TC_D}$) outputs (Carry and Borrow respectively) allow multistage binary counter operations without additional logic. The counters are cascaded by feeding the terminal count-up output to the count-up clock input and the terminal count-down output to the count-down input of the following counter.

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

CHARACTERISTICS		UNITS
Storage Temperature	−65°C to +150	°C
Temperature (Ambient) Under Bias	−55°C to +125	°C
V_{CC} Pin Potential to Ground Pin	−0.5V to +7	Volts
Voltage Applied to Outputs for high output state	−0.5V to V_{CC}	value
Input Voltage (D.C.)	−0.5V to +5.5	Volts

RECOMMENDED OPERATING CONDITIONS

	ITT54192, ITT54193 MIN	NOM	MAX	ITT74192, ITT74193 MIN	NOM	MAX	UNIT
Supply voltage V_{CC}	4.5	5	5.5	4.75	5	5.25	V
Normalized fan-out from each output, N			10			10	
Input count frequency, f_{count}	0		25	0		25	MHz
Width of any input pulse, t_w	20			20			ns
Data setup time, t_{setup} (see Figure 7 and Note 2)	20			20			ns
Data hold time, t_{hold} (see Note 3)	0			0			ns
Operating free-air temperature range, T_A	-55	25	125	0	25	70	°C

NOTES: 2. Setup time is the interval immediately preceding the positive-going edge of the load pulse during which interval the data to be recognized must be maintained at the input to ensure its recognition.

3. Hold time is the interval immediately following the positive-going edge of the load pulse during which interval the data to be recognized must be maintained at the input to ensure its recognition.

ELECTRICAL CHARACTERISTICS OVER RECOMMENDED OPERATING FREE-AIR TEMPERATURE RANGE (unless otherwise noted)

SYMBOL	CHARACTERISTICS	TEST FIGURE	ITT54192, ITT54193 MIN	TYP‡	MAX	ITT74192, ITT74193 MIN	TYP‡	MAX	UNITS	CONDITIONS†
V_{IH}	High-level input voltage	1 and 2	2			2			V	
V_{IL}	Low-level input voltage	1 and 2			0.8			0.8	V	
V_{OH}	High-level output voltage	1	2.4			2.4			V	V_{CC} = MIN, V_{IH} = 2 V V_{IL} = 0.8 V, I_{OH} = -400 μA
V_{OL}	Low-level output voltage	2			0.4			0.4	V	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = 18 mA
I_{IH}	High-level input current	3			40 1			40 1	μA mA	V_{CC} = MAX, V_I = 2.4 V V_{CC} = MAX, V_I = 5.5 V
I_{IL}	Low-level input current	4			-1.6			-1.6	mA	V_{CC} = MAX, V_I = 0.4 V
I_{OS}	Short-circuit output current‡	5	-20		-65	-18		-65	mA	V_{CC} = MAX
I_{CC}	Supply current	6		65	89		65	102	mA	V_{CC} = MAX

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type. ‡All typical values are at V_{CC} = 5 V, T_A = 25°C. ‡Not more than one output should be shorted at a time.

SWITCHING CHARACTERISTICS, V_{CC} = 5 V, T_A = 25°C, N = 10

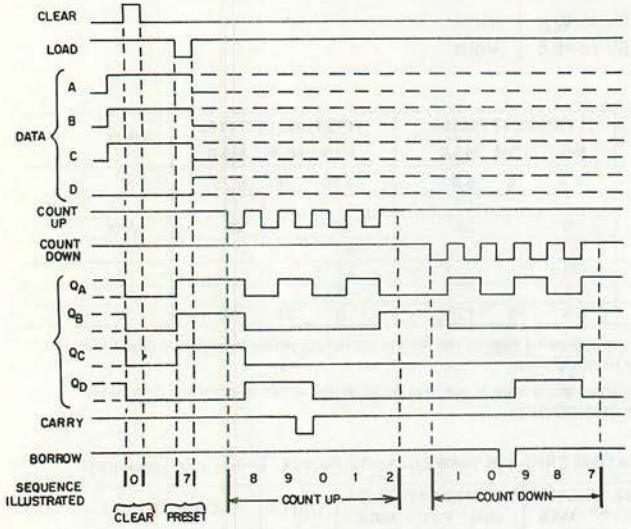
PARAMETER§	FROM INPUT	TO OUTPUT	TEST FIGURE	MIN	TYP	MAX	UNITS	CONDITIONS
f_{max}				25	32		MHz	C_L = 15 pF, R_L = 400 Ω
t_{setup}			7		14	20	ns	
t_{PLH} t_{PHL}	Count-up	Carry	8		17 16	26 24	ns	
t_{PLH} t_{PHL}	Count-down	Borrow	8		16 16	24 24	ns	
t_{PLH} t_{PHL}	Either Count	Q	8		25 31	38 47	ns	
t_{PLH} t_{PLH}	Load	Q	7		27 29	40 40	ns	
t_{PHL}	Clear	Q	7		22	35	ns	

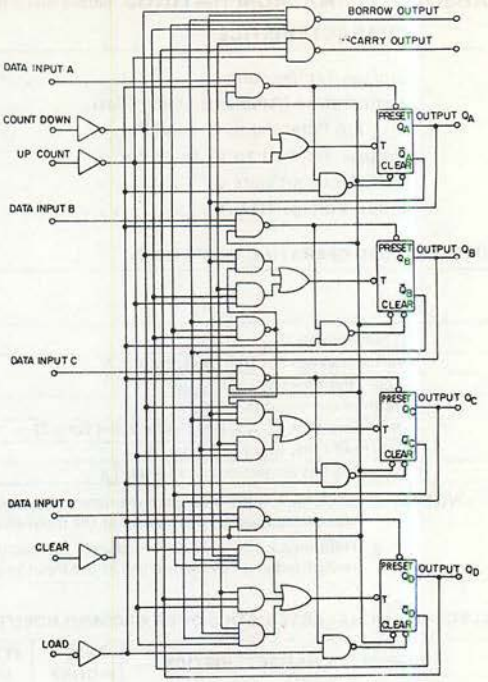
§f_{max} = maximum clock frequency t_{PLH} = propagation delay time, low-to-high-level output t_{PHL} = propagation delay time, high-to-low-level output

ITT54-74192 DECADE COUNTERS

TYPICAL CLEAR, LOAD, AND COUNT SEQUENCES

1. Clear outputs to zero.
2. Load (preset) to BCD seven.
3. Count up to eight, nine, carry, zero, one, and two.
4. Count down to one, zero, borrow, nine, eight, and seven.

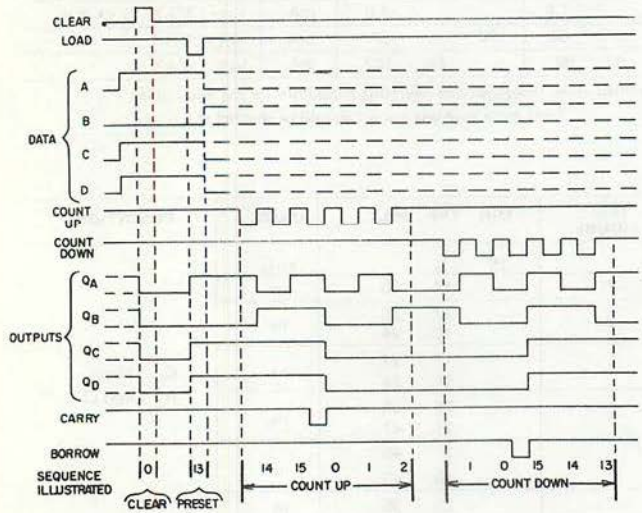


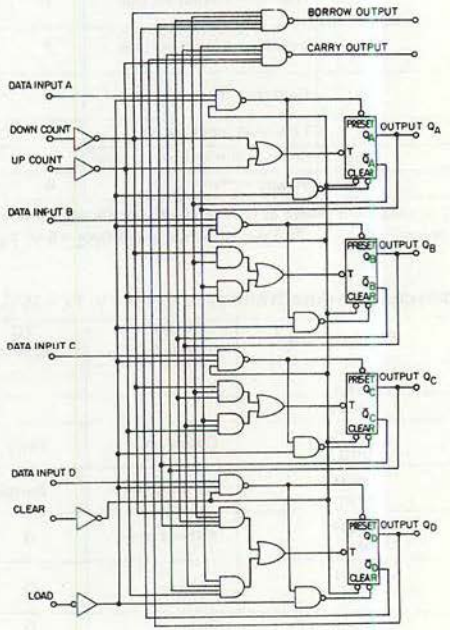


ITT54-74193 BINARY COUNTERS

TYPICAL CLEAR, LOAD, AND COUNT SEQUENCES

1. Clear outputs to zero.
2. Load (preset) to BVD thirteen.
3. Count up to fourteen, fifteen, carry, zero, one, and two.
4. Count down to one, zero, borrow, fifteen, fourteen, and thirteen.





NOTES: A. Clear overrides load, data, and count inputs.
B. When counting up, count-down input must be high; when counting down, count-up input must be high.

PARAMETER MEASUREMENT INFORMATION

D-C TEST CIRCUITS*

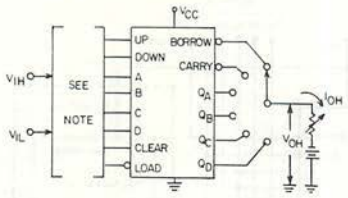


FIGURE 1 – V_{IH}, V_{IL}, V_{OH}
Each output is tested separately.

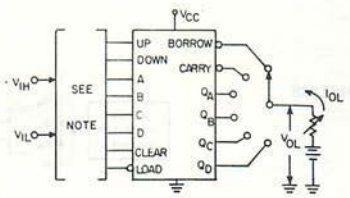


FIGURE 2 – V_{IH}, V_{IL}, V_{OL}
Each output is tested separately.

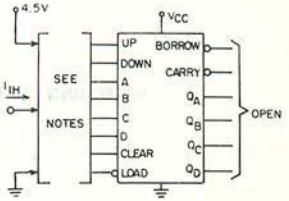


FIGURE 3 – I_{IH}

NOTES: A. Each input is tested separately.
B. Apply V_I to input under test, and ground other inputs except when testing data inputs, apply 4.5 V to clear and load inputs.

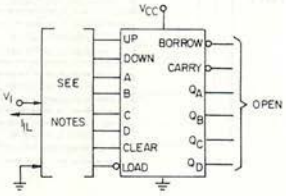


FIGURE 4 – I_{IL}

NOTES: A. Each input is tested separately.
B. Apply V_I to input under test and ground other inputs.

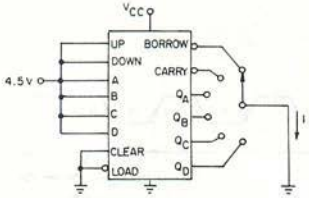


FIGURE 5 – I_{OS}
Each output is tested separately in the high-level state.

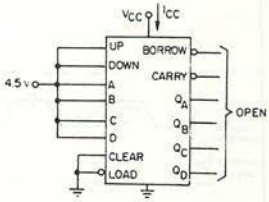
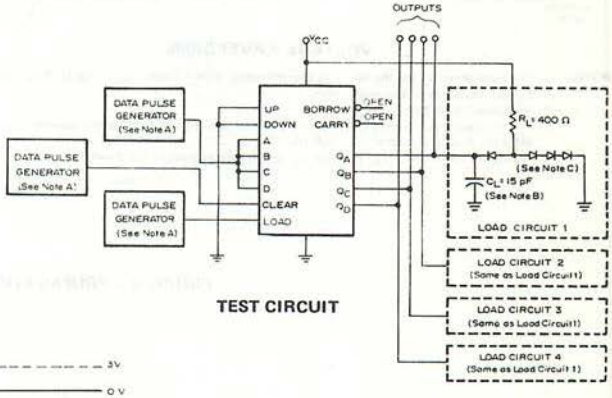


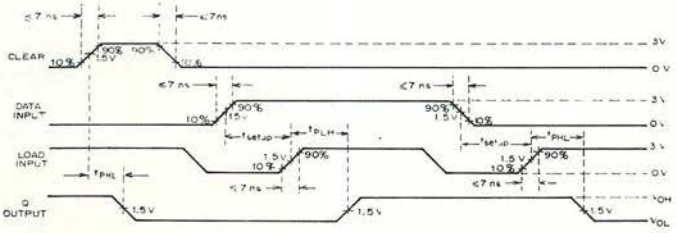
FIGURE 6 – I_{CC}

* Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

SWITCHING CHARACTERISTICS



TEST CIRCUIT



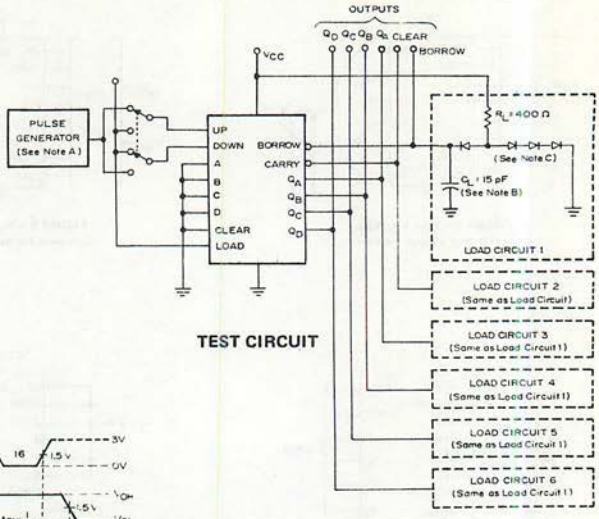
VOLTAGE WAVEFORMS

NOTES: A. The pulse generators have the following characteristics: $Z_{out} \approx 50\ \Omega$; for the data pulse generator, PRR = 500 kHz, duty cycle = 50%; for the load pulse generator, PRR = 1 MHz, duty cycle = 50%.
B. C_L includes probe and jig capacitance.
C. All diodes are 1N3064.

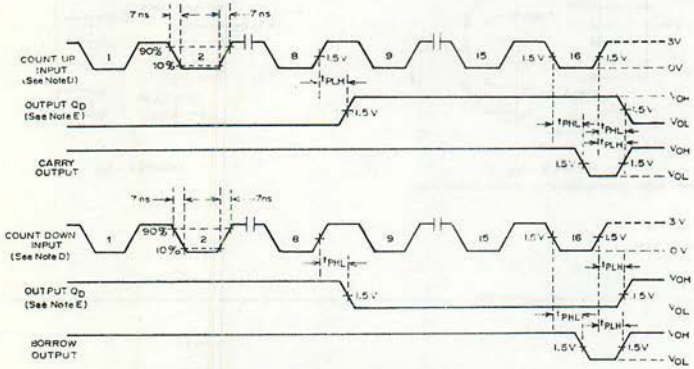
FIGURE 7 – CLEAR, SETUP, AND LOAD TIMES

PARAMETER MEASUREMENT INFORMATION

SWITCHING CHARACTERISTICS



TEST CIRCUIT



VOLTAGE WAVEFORMS

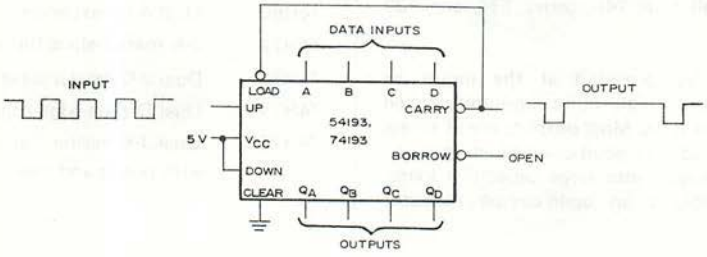
NOTES: A. The pulse generator has the following characteristics: PRR = 1 MHz, $Z_{out} \approx 50\,\Omega$, duty cycle = 50%.
B. C_L includes probe and jib capacitance.
C. All diodes are 1N3064.
D. Count-up and count-down pulses shown are for the SN54193/SN74193 binary counters. Count cycle for SN54192 decade counter is 1 through 10.
E. Waveforms for outputs Q_A, Q_B, and Q_C are omitted to simplify the drawing.

FIGURE 8 – PROPAGATION DELAY TIMES

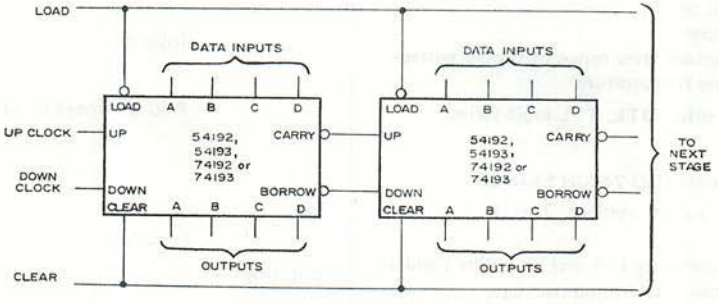
TYPICAL APPLICATION DATA

MODULO-N DIVIDER

The ITT54193/ITT74193 can be used to divide an incoming count frequency by any integral number (N) from one to 16. This is done by modifying the count frequency occurring at the carry output by presetting the data inputs to 16 minus N. By connecting the carry output to the load input, the counter will count to the maximum state (15) and the data inputs will then be enabled on the succeeding clock pulse. The counter outputs are then preset to the levels applied at the data inputs and the count sequence is repeated.



The ITT54192/ITT74192 may be used in the same manner to perform division by any number from 1 to 10.



CASCADING Circuitry is provided internally for cascading these counters. The mode of cascading shown below is ripple borrow/carry. No external components are required.

GENERAL INFORMATION ITT 54H/74H SERIES TTL FAMILY

This series is designed to be used in conjunction with the 54/7400 Series TTL in system locations requiring minimum propagation delays. They form a TTL family (Transistor-Transistor Logic) guaranteed to operate over the following ambient temperature ranges:

54H Series −55°C to 125°C
74H Series 0°C to 75°C

All devices operate over a frequency range between D.C. and typically 30 and 50 MH_Z, and are fully compatible with all 54H/74H series TTL and 930 series DTL.

Clamping diodes are provided at the inputs to enhance the inherent high noise immunity when driving transmission lines. Most outputs are of totem pole configuration to give good drive capability, i.e., high fan-out, especially into large capacitive loads. Other outputs include an open-circuit collector connection.

All functions are available in ceramic dual-in-line or plastic dual-in-line packages.

FEATURES

High speed – typical propagation delay (gate) of 6 ns.

@ C_L = 25pF

Guaranteed noise margin–greater than 400 mV.
Low power dissipation– 23 mW per gate at 50% duty cycle.
Worst case fan-out of 10.
Low output impedance.
Logic levels guaranteed over range of supply voltage and operating temperature
Compatible with other DTL, TTL logic series.

INDEX FOR STANDARD 7400H SERIES

For the military range, replace 74H in the type number by 54H.

Prefix the type number by ITT and end with J which indicates the ceramic dual-in-line package.
For example: ITT5484J is a 16 BIT MEMORY device in 54 series logic with a ceramic dual-in-line package.

TYPE	DESCRIPTION
74H00	Quad 2 i/p NAND
74H01	Quad 2 i/p NAND (open-collector 5-5 V rating)
74H04	Hex inverter
74H05	Hex inverter (open-collector 5-5 V rating)
74H10	Triple 3 i/p NAND
74H20	Dual 4 i/p NAND
74H30	8 i/p NAND
74H40	Quad 2 i/p NAND buffer
74H50	Expandable dual 2 wide, 2 i/p A.O.I.
74H51	Dual 2 wide, 2 i/p A.O.I.
74H53	Expandable 4 wide, 2 i/p A.O.I.
74H54	4 wide, 2 i/p A.O.I.
74H60	Dual 4 i/p expander
74H72	J-K master-slave flip-flop
74H73	Dual J-K master-slave flip-flop
74H74	Dual D-type edge-triggered flip-flop
74H76	Dual J-K master-slave flip-flop with preset and clear

FUNCTIONAL INDEX

	FUNCTION	TYPE
Gates	NAND	74H00
		74H01*
		74H10
		74H20
		74H30
		74H40
	Inverter	74H04
		74H05*
	And-Or-Invert (A.O.I.)	74H50
		74H51
		74H53
		74H54
	Expander	74H60*
Flip-flops		74H72
		74H73
		74H76
	D-type	74H74

INTRODUCTION TO TTL

The TTL circuit configurations are designed so that the uniform logic and noise margin levels apply to all the standard devices in the families. Thus many parameters and their limits are common. In addition the operating conditions are identified for each family. Once these standard operating conditions are understood it becomes possible for the designer to use the family by simply referring to the logic and connection diagrams on each data sheet. All common information is included in the remainder of this section.

For ease in reading, the data only refers to the 74H series family but it is equally applicable to the 54H series. Where there are exceptions these are clearly indicated on the individual data sheets concerned.

LOGIC DEFINITION

Positive logic is used throughout the data sheets. This is defined as follows.

Logical '0' = Low voltage; typically 0.2 V but ⟨ 0.8 V
Logical '1' = High voltage; typically 3.3 V but ⟩ 2.0 V

Current flowing into a device terminal is defined as positive.

D.C. CHARACTERISTICS COMMON TO ALL DEVICES

(except where otherwise stated)

D.C. tests are carried out under the specified conditions. All inputs and outputs are tested for all possible logic states. Worst state load currents and voltages are applied and the test limits are applicable over the full temperature range.

	Min.	Max.	Unit
Supply voltage, V_{CC}:			
74H series	4.75	5.25	V
54H series	4.5	5.5	V
Operating temperature:			
74H series	0	75	°C
54H series	−55	125	°C

D.C. noise margin typically greater than 1V.

ABSOLUTE MAXIMUM RATINGS

(above which the useful life of the device may be impaired)

Continuous supply voltage V_{CC} (Note 1) 7V
Input voltage . . . . . 5.5 V
Voltage between inputs . . . . . 5.5 V
Continuous input current . . . . . −10 mA
Standard output voltage . . . . . −0.5 to 5.5 V
Storage temperature . . . . . −65°C to 150°C

Note I
This rating is reduced to 5.5 V if unused inputs are connected directly to V_{CC}.

STANDARD CHARACTERISTICS

(limits apply over the full range of operating temperature and for standard totem pole output except where otherwise stated).

Where characteristics for devices differ from the table these are shown in the data sheets.

PARAMETER	LIMIT (Note 8)				CONDITIONS	
	Min.	Typ.	Max.	Unit	V_{CC}	
V_{IH}	2.0			V	Min.	V_{OL}⟨0.4V or V_{OH} ⟩ 2.4V (Note 1)
V_{IL}			0.8	V	Min.	V_{OL} ⟨ 0.4V or V_{OH} ⟩ 2.4V (Note 2)
V_{OL} (standard output)		0.22	0.4	V	Min.	I_{OL}= 20 mA, V_{IH}=2V or V_{IL}=0.8V (Note 3)
V_{OL} (buffer output) V_{OH}	2.4	3.3		V	Min.	V_{IL}=0.8V or V_{OH}=2.0V (Note 4)
I_{CEX} open collector only			250	μA	Min.	V_{IL}=0.8V, V_{IH}=2V, V_{OUT}=max. o/p voltage rating
$-I_F$			2.0	mA	Max.	V_F=0.4V (Note 5)
I_R			50	μA	Max.	V_R=2.4V, input loading-1 unit load (Note6)
I_R			1.0	mA	Max.	V_R=5.5 V irrespective of input loading
$-I_{SC}$						
54H series	40		100	mA	Max.	V_{OUT}=0 V (Note 7)

Note 1

Condition at outputs dependent on the truth table of the device. For example, for gates and buffers, $V_{OL} \leq 0.4$ V applies, and for flip-flops, either $V_{OL} \leq 0.4$ V or $V_{OH} \geq 2.4$ V applies at each output. Output conditions do not apply for 74H60.

Note 2

Conditions at outputs dependent on the truth table of the device, for example; for gates and inverters $V_{OH} > 2.4$ V. Output conditions do not apply for devices with open collector output. This parameter does not apply for 7413, 74121.

Note 3

Conditions V_{IH} and V_{IL} depend on device truth table.

Note 4

This parameter for totem pole output devices only. V_{IL} and V_{IH} apply according to the truth table. $I_{OH} = -500\ \mu A$ for devices with Fan-out = 10; $I_{OH} = -1.0$ mA for 54H/74H74; $I_{OH} = -1.5$ mA for 54H/74H40.

Note 5

Limits apply for an input loading of 1 unit load; for other input loadings multiply limits by number of unit loads. For flip-flops, see appropriate data for test conditions.

Note 6

All other inputs at 0 V for 74H72, 74H73, 74H76. For 74H74 consult data sheet. Limits to be multiplied by the input loading of the device.

Note 7

For all devices not more than one output to be shorted at any time. Open collector devices: no parameter for $-I_{SC}$.

Note 8

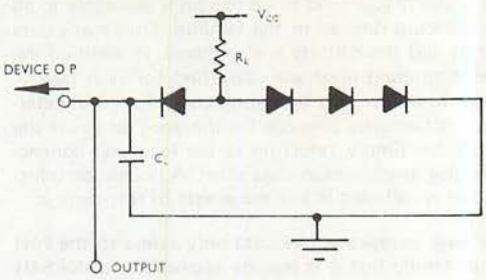
Typical limits are at ambient temperature, T_A=25°C and V_{CC}=5 V.

A.C. TESTS

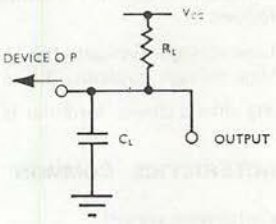
Testing of propagation delays is carried out using the typical switching load circuits shown below. These load circuits are designed to simulate full fan-out loading. An oscilloscope with high impedance probes and having a bandwidth of at least 100 MHz is suitable for these measurements.

TYPICAL SWITCHING TEST LOAD CIRCUITS

For totem pole outputs:



For open collector outputs:

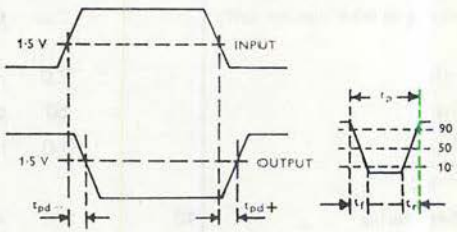


Diodes are type 1N4148 or equiv.

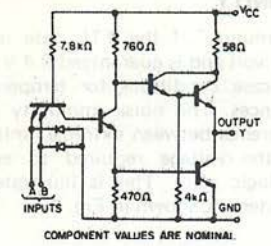
The values of C_L and R_L are quoted in the data sheets. Value of C_L includes probe and jig capitance.

The characteristics of the pulse generator used at the input of the device are stated in the data sheets. Typical characteristics are: V_{OUT}= 3 V; Rise time, tr, =Fall time, t_f,=less than 7 ns; $Z_o = 50$; Pulse Repetition Frequency, P.R.F. = 1 MHz; Pulse width for gate, $t_p = 500$ ns.

Waveforms



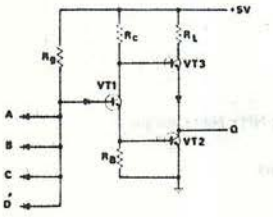
CIRCUIT DIAGRAM OF MIC74H00 GATE



COMPONENT VALUES ARE NOMINAL

The d.c. operation of this circuit is more readily understood if the multiemitter transistor (MET) connecting the inputs is considered equivalent to a diode AND gate in series with an offset diode connected to the base of transistor VT1. This is shown in Fig. 2, the emitter-base junctions of the MET forming the input diodes and the collector-base junction forming the offset diode.

Fig. 2. Simplified analogy of TTL gate.



When all the inputs are positive a logic '1' current flows from the positive supply through R_g into the base of VT1 which heavily conducts and turns VT2 'ON' into the saturated state. Since both VT1 and VT2 are saturated, there is insufficient voltage across the base emitter terminals of VT3 to render it conducting. The output voltage is about +0.2 V, (i.e. saturation voltage of VT2). The collector current of VT2 will consist of the total 'sinking' current from the gates connected to the output terminal. When the base current drive to VT2 is high, VT2 can remain saturated even with a large collector current, with adverse circuit tolerances and temperature variations. This permits a fan-out of up to 10. With a multiemitter transistor, more current flows from a positive held input than with a conventional D.T.L. gate (the leakage current of the reverse biassed input diode) since the MET is biassed in the inverted mode and the functions of emitter and collector are reversed. However, the MET is designed to have a very low inverse gain and I_R is kept to a minimum. I_R will equal the emitter base leakage current plus the product of inverse current gain and I_G.

2. LOW OR OFF STATE

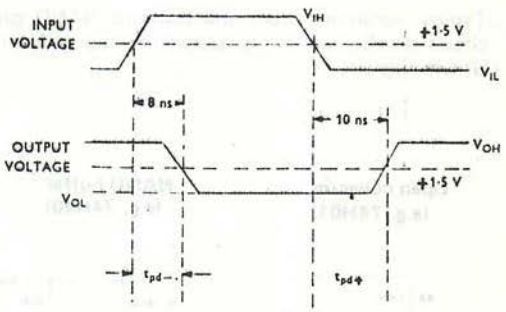
The opposite state shown in Fig. 1B is achieved if the voltage of any number of inputs is reduced below a threshold level of about + 1.5 volts. Fig. 1B shows the conditions when input A is at +0.2 volts (a typical output voltage of a previous gate). No base current flows into VT1 since the collector of the MET is at too low a potential, with respect to its base.

Therefore, no current will flow through VT1 and VT2 other than leakage current (which can be neglected in this analysis). The transistor VT3 will conduct to provide sufficient output current to maintain following gates connected to the output terminal at 3.3 V positive in logic 1. The fan-out is high (10) under worst case conditions because of the low output impedance of VT3.

3. CHANGEOVER BETWEEN STATES

The transistor action of the MET considerably improves the switching speed when compared with a DTL gate. In switching from the ON to the OFF state the MET saturates and rapidly removes the charge stored in VT1 turning it off. Then VT2 begins to turn off and VT3 turns on as the collector potential of VT1 rises. VT3 assists VT2 to turn off and pulls the output terminal rapidly positive, charging any load capacitance. The diode D1 helps to prevent VT2 and VT1 from conducting simultaneously and RL limits the current through VT3 to a safe value during the switch over if the output terminal is accidentally shorted.

Fig. 3. Propagation delay waveforms.



Switching from the OFF to the ON state is more rapid than ON to OFF since none of the transistors VT1, VT2 and MET are saturated in the OFF condition. The switch to the ON condition is particularly fast owing to additional drive by transistor VT1 in turning on VT2. Fig. 3 shows the typical switching times from this gate.

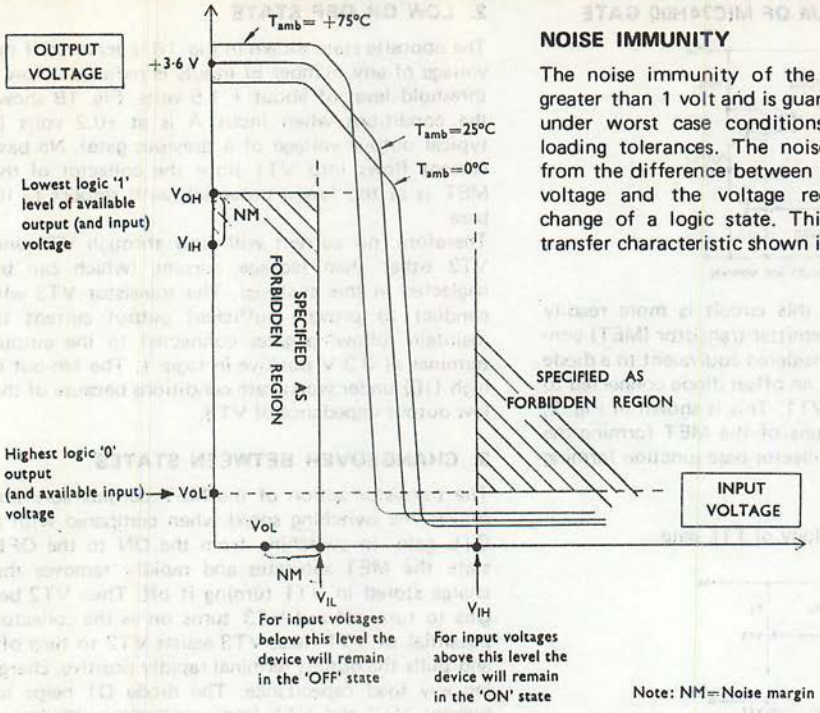


Fig. 4. Typical transfer characteristic showing noise margins

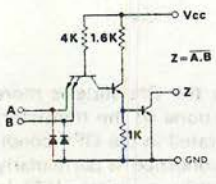
NOISE IMMUNITY

The noise immunity of the TTL gate is typically greater than 1 volt and is guaranteed 0.4 V minimum under worst case conditions for temperature and loading tolerances. The noise immunity is derived from the difference between extreme limits of input voltage and the voltage required to ensure the change of a logic state. This is illustrated by the transfer characteristic shown in Fig. 4.

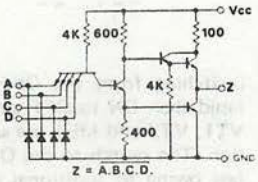
GATES DIFFERING FROM THE STANDARD CIRCUIT

Typical variations from the standard NAND gate circuit configuration are shown in the following circuit diagrams.

Open collector (e.g. 74H01)



NAND buffer (e.g. 74H40)



ITT74H00	Quad 2 input NAND gate
ITT74H01	Quad 2 input NAND gate
ITT74H04	Hex inverter
ITT74H05	Hex inverter (open collector)
ITT74H10	Triple 3 input NAND gate
ITT74H20	Dual 4 input NAND gate
ITT74H30	Single 8 input NAND gate
ITT74H40	Dual 4 input NAND buffer

DESCRIPTION

ITT74H400, ITT74H10, ITT74H20, ITT74H30, ITT74H40 are standard totem pole output gate devices.

ITT74H01 is open collector output device featuring:

Wired or capability
Output rating 5.5V - Suffix "A" denotes 15V

ITT74H40 is a NAND buffer featuring a FAN OUT OF 30.

The circuits of all these devices are the same as those shown in the general information section,

TYPICAL CHARACTERISTICS

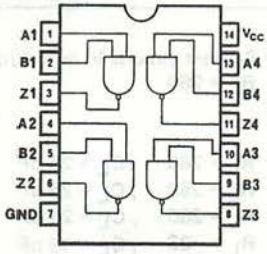
Device type		Propagation delay ns	Power dissipation per package (50% duty cycle) mW
Quad 2 input NAND	74H00	6	.90
Triple 3 input NAND	74H10	6	67.5
Dual 4 input NAND	74H20	6.5	45
Single 8 input NAND	74H30	8	22.5
Open collector 2 input NAND	74H01	9	82
Hex inverter	74H04	6.5	140
Open collector Hex inverter	74H05	9	140
Dual 4 input NAND buffer	74H40	7.5	85

Input loading factor . . . . . 1 unit load

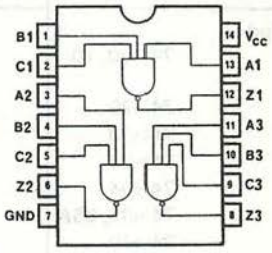
Fan out (for totem pole outputs):
Standard gates . . . . . 1 to 10 unit loads
Buffer gates . . . . . 1 to 30 unit loads

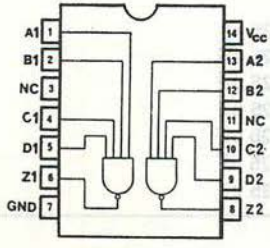
Output voltage rating for
open collector outputs 5.5V

74H400, 74H01

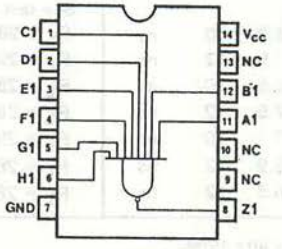


74H10

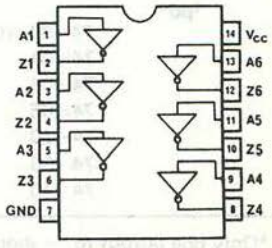




74H20, 74H40



74H30



74H04, 74H05

D.C. CHARACTERISTICS

Information on the absolute maximum ratings and the other D.C. characteristics of these devices (which are common to other integrated circuits in this series) is stated in the general information section.

PARAMETER	LIMIT				CONDITIONS
	Min.	Typ.	Max.	Unit	V_{CC}
I_{CCL}					
74H00, 01		26	40	mA	Max. V_{IN} on all inputs=5.0V
74H10		19.5	30	mA	
74H20		13	20	mA	
74H30		6.5	10	mA	
74H04, 05		40	58	mA	
74H40		25	40	mA	
I_{CCH}					
74H00, 01		10	16.8	mA	Max. V_{IN} on all inputs=0 V
74H01		6.8	10	mA	
74H10		7.5	12.6	mA	
74H20		5	8.4	mA	
74H30		2.5	4.2	mA	
74H40		10.4	16	mA	
74H04, 05		16	26	mA	
Exceptions to common characteristics:					
$-I_{SC}$ (Buffers) 54/74H40	40		125	mA	Max. *$V_{OUT} = V_{IN} = 0V$

SWITCHING CHARACTERISTICS

Switching test circuits as shown in the general information section.

Note

Other inputs of the gate under test taken to 2.4 V,

Characteristics of pulse from generator at a device input:

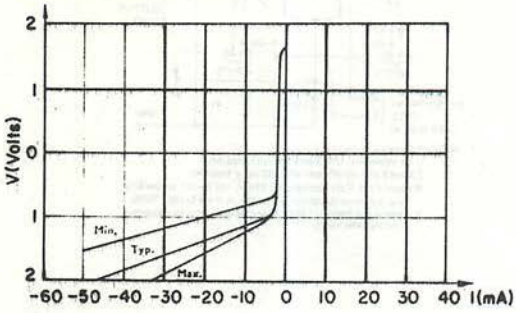
$t_r = 7$ ns, $t_f = 7$ ns, $t_p = 500$ ns, P.R.F. = 1 MHz, $Z_o = 50$, Amplitude = 3.0 V

Parameter		Min.	Typ.	Max.	Units	Conditions
t_{pd+}						
	74H00, 10		5.9	10	ns	See test circuits in introduction, C_L = 25 pF, R_L = 280
	74H20		6	10	ns	
	74H30		6.8	10	ns	
	74H01		10	15	ns	R_L = 280 , C_L = 25 pF
	74H04		6	10	ns	R_L = 280 , C_L = 25 pF
	74H05, 05A		10	15	ns	R_L = 280 , C_L = 25 pF
	74H40		8.5	12	ns	R_L = 93 , C_L = 15 pF
t_{pd-}						See test circuit:
	74H00, 10		6.3	10	ns	R_L = 280 , C_L = 25 pF
	74H01		7.5	12	ns	R_L = 280 , C_L = 25 pF
	74H04		6.5	10	ns	R_L = 280 , C_L = 25 pF
	74H05		7.5	12	ns	R_L = 280 , C_L = 25 pF
	74H20		7	10	ns	R_L = 280 , C_L = 25 pF
	74H30		8.9	12	ns	R_L = 280 , C_L = 25 pF
	74H40		6.5	12	ns	R_L = 280 , C_L = 25 pF

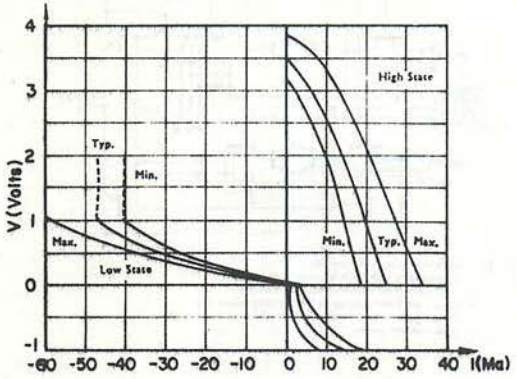
*Only one output to be short-circuited at any time.

TYPICAL CHARACTERISTICS OF STANDARD NAND GATES

Typical and 95% Limit Input Characteristics (at 5 V and 0°C to 75°C)



Typical and 95% Limit Output Characteristics (at 5 V and 0°C to 75°C)



APPLICATION NOTES

Wired-Or Function

The purpose of the 5.5 V open collector devices is primarily to perform the 'wired-OR' function which can not be implemented by the standard active pull up output circuit. The open collector devices require an external resistor between output and V_{CC}. The choice of resistor value is a compromise between fan out requirements, the number of commoned outputs, power dissipation and speed. Limiting values of R_X are given by the following inequalities.

$$R_X > \frac{V_{CC}(max.) - V_{OL}(max.)}{(10-N)\, I_F}$$

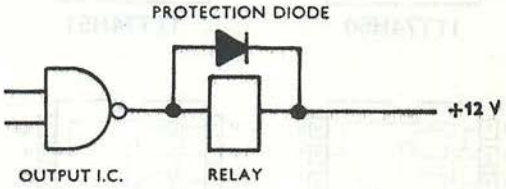
$$R_X < \frac{V_{CC}(min.) - V_{OH}(min.)}{M.I_{CEX} + N.I_R}$$

Where M=Number of outputs commoned together in the 'Wired-OR' function; N=Fan out required.

High Voltage Output

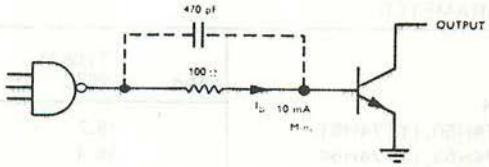
A typical use of the high voltage open collector device:

Miniature relay drives – A protection diode is required to prevent turn off transients damaging the output transistor (as shown).



Output Interfacing

When interfacing between TTL logic and lamps, relays etc. a discrete driving transistor is normally used. If there are several such interface transistors being driven from one multiple gate TTL device a problem is encountered in determining the value of base resistor to be used, to ensure maximum base drive without risk of over dissipating the ICC, when all outputs are high. The circuit shown below is suitable for use with the ITT devices and gives minimum base current of 10 mA.



Standard 74 Series Gate

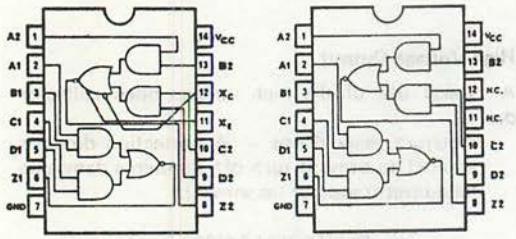
The inclusion of the 470 pF capacitor will give a considerable improvement in speed of this circuit. If the transistor used is a sN2369A propagation delay times from the gate inputs to output of 10ns can be achieved.

DUAL 2 WIDE 2-INPUT AND/OR INVERT GATES – ITT74H50, 51
SINGLE 4 WIDE 2-INPUT AND/OR INVERT GATES – ITT74H53, 54
THE MIC74H50 AND THE MIC74H53 ARE EXPANDABLE

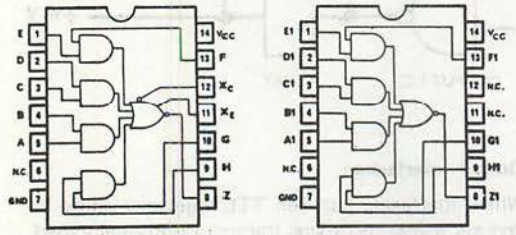
TYPICAL CHARACTERISTICS

Propagation delay . . . . . 6.5 ns
Power dissipation . . . . . 58 mW (74H50, 74H51)
(50% duty cycle) . . . . 42 mW (74H53, 74H54)
Input loading factor . . . . . 1 unit load
Fan-out . . . . . 1 to 10 unit loads

Pin configuration (top views)



ITT74H50 ITT74H51

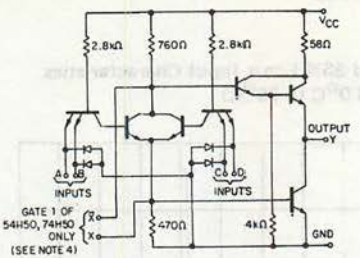


ITT74H53 ITT74H54

Make no external connection to pins 11 and 12

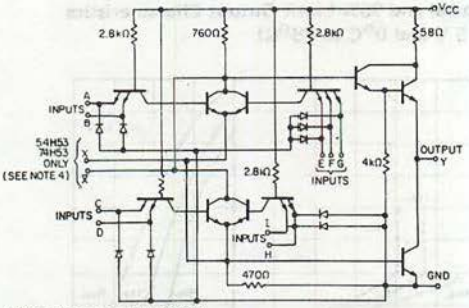
If expander is not used leave pins 11 and 12 open

Circuit diagram of one gate (ITT74H50 and ITT74H51)



NOTES: 1. Component values are nominal.
2. For expanding, both inputs are used together.
3. X and X̄ pins are left open when not using expander.
4. Inputs X and X̄ are functional on 54H50 and 74H50 circuits only. Make no external connection to X and X̄ pins of the 54H51/74H51.
5. A total of four 54H60/74H60 expander gates may be connected to the expander inputs.

Circuit diagram of ITT74H53 and ITT74H54



NOTES: 1. Component values are nominal.
2. For expanding, both inputs are used together.
3. X and X̄ pin are left open when not using expander.
4. Inputs X and X̄ are functional on 54H53/7453 circuits only.
5. A total of four 54H60/74H60 expander gates may be connected to the expander inputs.

PARAMETER	LIMIT				CONDITIONS	
	Min.	Type at 25°C	Max.	Units	V_{CC}	
I_{CCH}						
ITT74H50, ITT74H51		15.2	24	mA	Max.	V_{IN} on all inputs
ITT74H53, ITT74H54		19.4	14	mA	Max.	5.0 V
I_{CCL}		4.0	8.0	mA	Max.	V_{IN} on all inputs 0\
ITT74H50, ITT74H51		8.2	12.8			
ITT74H53, ITT74H54		7.1	11			

Information on the absolute maximum ratings and the other D.C. characteristics of these devices (which are common to other integrated circuits in this series) is stated in the general information section.

D.C. CHARACTERISTICS OF ITT5450/3 EXPANDER INPUTS AT −55°C

PARAMETER	LIMIT				CONDITIONS
	Min.	Type	Max.	Unit	V_{CC}
I_X expander current			5.85	mA	Min. $V_{\overline{X}}$ = 1.4 V
V_{BE} base emitter voltage of output transistor			1.0	V	Min. I_{OL} = 20 mA, R_{CE} = 0, I_E = 700 μA (Note 1)
V_{OH} output high voltage	2.4	3.3		V	Min. I_{OH} = −500 μA, I_E = 320 μA, I_C = −320 μA (Note 1)
V_{OL} output low voltage		0.22	0.4	V	Min. I_{OL} = 20 mA, I_E = 470 μA, R_{CE} = 68 (Note 1)

D. C. CHARACTERISTICS OF ITT74H50/3 EXPANDER INPUTS AT 0°C

PARAMETER	LIMIT				CONDITIONS
	Min.	Type	Max.	Unit	V_{CC}
I_X expander current			6.3	mA	Min. $V_{\overline{X}}$ = 1.4 V
V_{BE} base emitter voltage of output transistor			1.0	V	Min. I_{OL} = 20 mA, R_{CE} = O, I_E = 1.1 mA (Note 1)
V_{OH} output high voltage	2.4	3.3		V	Min. I_{OH} = −500 μA, I_E = 570 μA, I_C = −570 μA (Note 1)
V_{OL} output low voltage		0.22	0.4	V	Min I_{OL} = 20 mA, I_E = 600 μA, R_{CE} = 63 (Note 1)

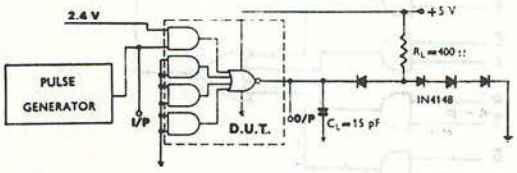
Note 1

V_{CE}, I_E, I_C and R_{CE} refer to voltage, current and resistance on X_E and X_C terminals.

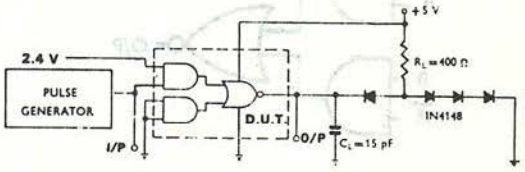
SWITCHING CHARACTERISTICS (V_{CC} = 5.0 V, T_{AMB} = 25°C)

PARAMETER	LIMIT				CONDITIONS
	Min.	Type	Max.	Unit	
t_{pd}^+		7	11	ns	See test circuits, expander pins open
t_{pd}^-		6.2	11	ns	See test circuits, expander pins open
t_{pd}^+		7.4		ns	See test circuits, $C_{\overline{X}}$ = 15 pF
t_{pd}^-		11.4		ns	See test circuits, $C_{\overline{X}}$ = 15 pF

Switching test circuit for ITT74H53/4



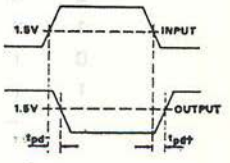
Switching test circuit for ITT74H50/1



Pulse Characteristics

t_f =	= 7 ns
t_r	= 7 ns
t_c	= 500 ns
P.R.F.	= 1 MHz
Z_o	− 50
Amplitude	= 3 V

Waveforms

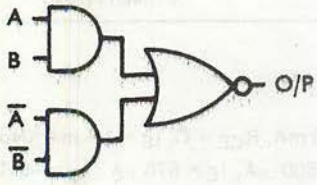


USE OF EXPANDER

The expander points are provided so that the input of the ITT74H50 or the ITT74H53 can be increased by a maximum of four 4-input NAND gates. Both X_C and X_E expander points must be used to connect to the X_C and X_E outputs of the ITT74H60 expander.

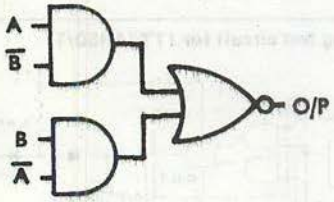
USE AS AN EXCLUSIVE OR GATE

The connections as an exclusive OR gate are shown below with inputs A and B.



A	B	O/P
0	0	0
1	0	1
0	1	1
1	1	0

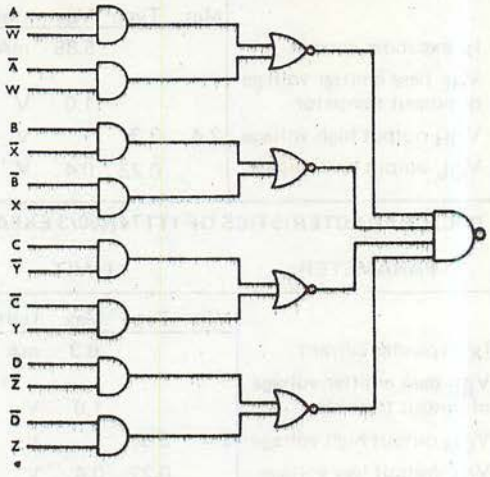
The inverse of exclusive OR function can also be obtained



A	B	O/P
0	0	1
1	0	0
0	1	0
1	1	1

ITT7450 and ITT7451 USED AS A COMPARATOR

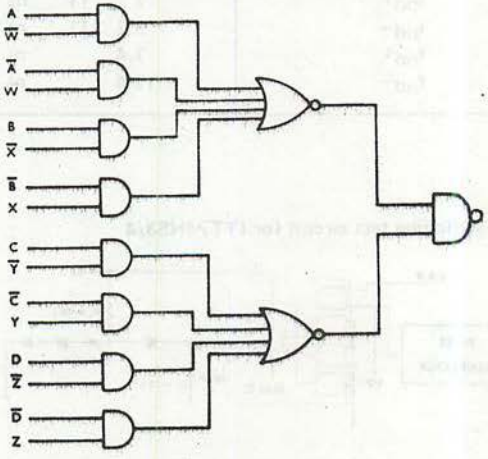
Two binary numbers ABCD and WXYZ.



When ABCD = WXYZ O/P = 0
when ABCD ⟩ or ⟨ WXYZ O/P = 1

ITT7453 and ITT7454 USED AS A COMPARATOR

Two binary numbers ABCD and WYXZ.



When ABCD - WXYZ O/P = 0
when ABCD ⟩ or ⟨ WXYZ O/P = 1

TYPICAL CHARACTERISTICS

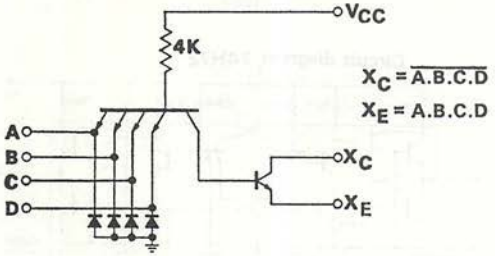
Output capacitance,

V_{CC} and Gnd terminal open	1.3 pF
Power dissipation (50% duty cycle)	12.5 mW
Input loading factor	1 unit load

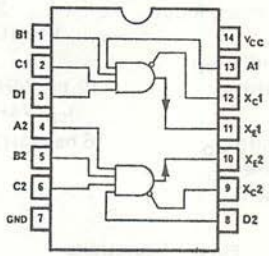
The ITT74H60 expander is intended for use with the ITT74H50 or ITT74H53 AND-OR-INVERT gates. Not more than four expander gates (two packages) should be connected to any AND-OR-INVERT gate. The X_C and X_E outputs of the expander should be connected respectively to X_C and X_E expander inputs of the AND-OR-INVERT gates. Inter-connecting leads should be kept as short as possible.

Circuit diagram of one expander

Resistance values in ohms



Pin configuration



PARAMETER	LIMIT				CONDITIONS	
	Min.	Type at 25°C	Max.	Units	V_{CC}	
V_{ON} on state voltage 74H60			0.4	V	Min	V_E = 1 V, V_{IH} = 2.0 V I_{ON} = 7.4 mA T_{AMB} = 0°C
54H60			0.4	V	Min	I_{ON} = 5.85 mA T_{AMB} = −55°C
V_{ON} on state voltage 74H60			0.4	V	Max	V_E = 0.6 V, V_{IH} = 2.0 V I_{ON} = 7.4 mA T_{AMB} = +70°C
54H60			0.4	V	Max	I_{ON} = 7.85 mA T_{AMB} = +125°C
I_{OFF} off-state output current– 74H60			570	μA	Min.	V_C=v.5V, V_{IL}=0.8V
54H60			320			R_E/GND = 575 Ω T_{AMB} = Min.
I_{ON} on-state output current–						
74H60	−600			μA	Max.	V_{IH}=2.0V, V_E=1.0V
54H60	−470			μA		T_{AMB}=Min.
$-I_F$ input forward current			2.0	mA	Max.	V_F=0.4V
I_R input reverse current			50	mA	Max.	V_R=5.5V

INPUT EXPANDER

PARAMETER	LIMIT				CONDITIONS	
	Min.	Type	Max.	Units	V_{CC}	
I_{CCH} supply current for highest dissipation (off state)		3	4.5	mA	Max.	V_{IN} on all inputs OV, V_E=0.85V
I_{CCL} supply current for lowest dissipation (on state)		1.9	3.5	mA	Max.	V_{IN} on all inputs 5.0V, V_E=-.85V

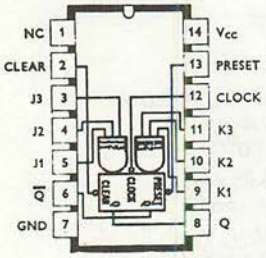
Information on the absolute maximum ratings and the other D.C. characteristics of this device (which are common to other integrated circuits in this series) is stated in the general information section.

TYPICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

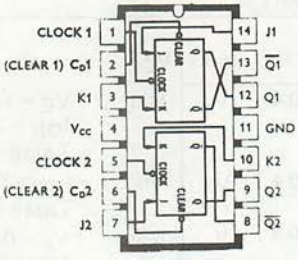
Maximum clock frequency	25 MHz
Propagation delay	18 ns
Power dissipation:	
Single type	80 mW
Dual type	160 mW
Input loading factor:	
J and K clock inputs	1 unit load
Direct and clock inputs	2 unit loads
Fan-out	1 to 10 unit loads
Clock pulse width t_{cp}	12 ns
Clear pulse width t_c	12 ns, 74H72, 74H73 t_{cp}, 74H76
Preset pulse width t_p	16 ns. 74H72, 74H76
Input set up time t_{sp}	t_{cp}
Input hold time t_h	0 ns

Pin configurations

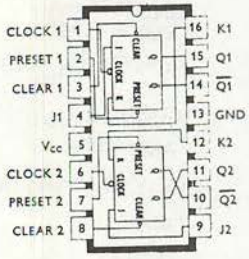
ITT7472



ITT7473



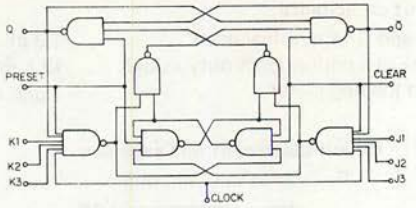
ITT7476



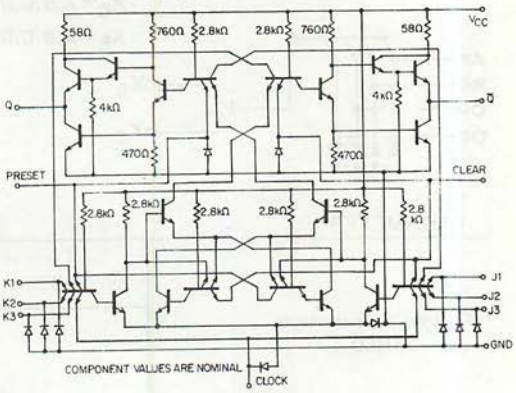
Truth Table

SYNCHRONOUS			ASYNCHRONOUS			
t_n	t_n+1		Preset	Clear	Q	$\overline{Q}$
D Input	Q	$\overline{Q}$	0	0	1	1
0	0	1	1	0	0	1
1	1	0	0	1	1	0
			1	1	No Control	

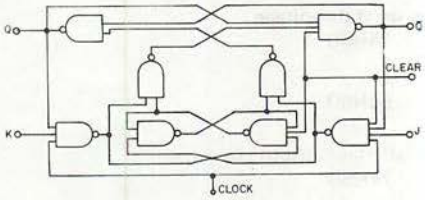
Logic diagram



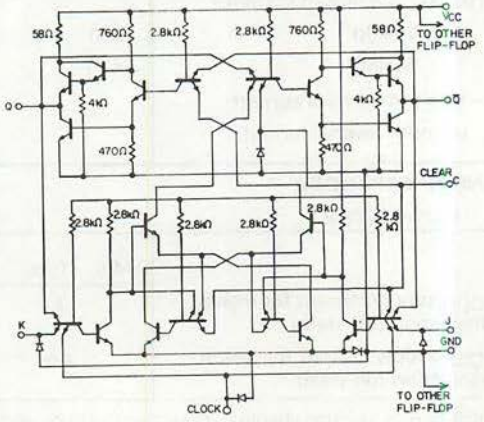
Circuit diagram 74H72



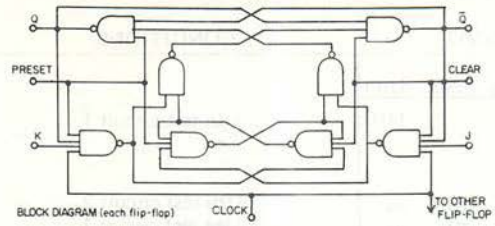
Logic diagram



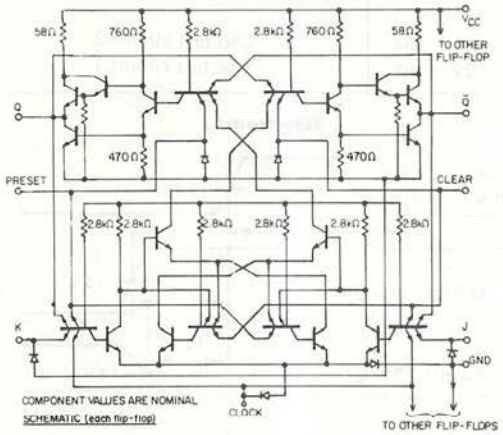
Circuit diagram ITT74H73



Logic diagram



Circuit diagram 74H76



DESCRIPTION

These devices consist of gated Master and slave bistables. The ITT74H72 with preset, clear and triple J and K inputs. The ITT74H73 with clear and single J and K inputs. The ITT74H76 with preset, clear and single J and K inputs. The direct inputs of clock J or K inputs. The clock input operates as follows, on a positive going transistion first the slave bistable is isolated from the master, then information is transferred from the J and K inputs to the master bistable. On a negative going transition first the J and K inputs are disabled then the information is transferred to the slave bistable. Operation will be according to the truth table if J and K information is present before and during the period that the clock is high. Because of the internal feedback from the Q and $\bar{Q}$ outputs to the J and K input AND gates one or other of the gates will have a logical '0' on one internal input. The external inputs cannot affect that gate. The other input AND gate will have a logical '1' on its internal input, if one of the external inputs goes to a logical '1' at any time while the clock is high the master bistable will change state and the Q and $\bar{Q}$ outputs will follow on the negative transition of the clock.

PARAMETER	LIMIT				CONDITIONS
	Min.	Type at 25°C	Max.	Units	V_{CC}
$-I_F$ input forward current					
All J and K inputs and clock			2.0	mA	Max. V_F=0.4V
Preset, clear			4.0	mA	Max. (Note 1)
I_R					
J and K inputs and clock			50	μA	Max. V_R = 2.4 V
Preset, and clear			100	μA	Max. V_R = 2.4 V
I_{CC} supply current		16	25	mA	Max.
Single type		32	50	mA	
All dual types					

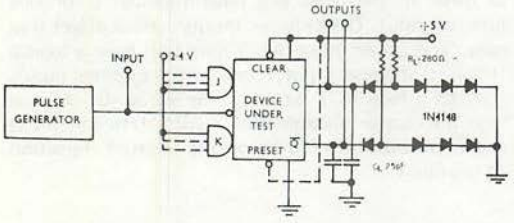
Note 1
Test with all other inputs at 4.5 V. Use preset or clear to set device to appropriate logic stste. Clock to be tested for both logic states. When testing J or K inputs all other inputs including internal inputs to the appropriate input AND gate must be at logical '1'.

Information on the absolute maximum ratings and the other D.C. characteristics of this device (which are common to other integrated circuits in this series) is stated in the general information section.

SWITCHING CHARACTERISTICS V_{CC}=5.0V, T_{AMB}=25°C

PARAMETER	LIMIT				CONDITIONS
	Min.	Typ.	Max.	Unit	
f_{max} maximum input clock frequency	25	30		MHz	Use test circuit 1.
t_{pd}+ propagation delay time to logical '1'					
Clear or preset to output		6	13	ns	Use test circuit 2.
Clock to output	6	14	21	ns	Use test circuit 1.
t_{pd}- propagation delay time to logical '0'					
Clear or preset to output		12	24	ns	Use test circuit 2.
Clock to output	10	22	27	ns	Use test circuit 1.

Test Circuit 1

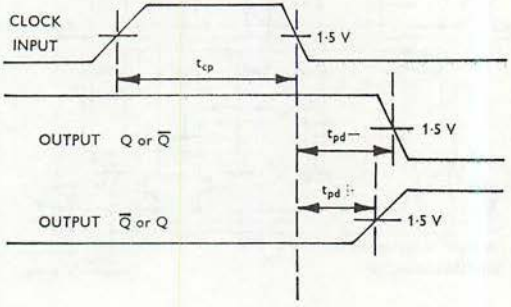


C_L includes probe and jig capacitance

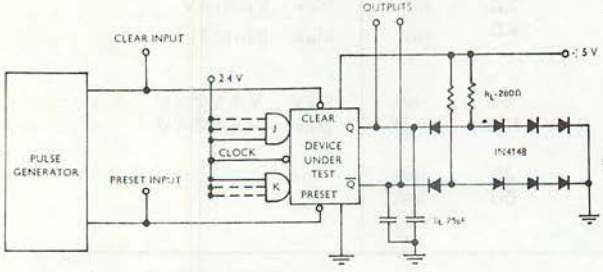
Pulse Characteristics

t_r = 7 ns
t_f = 7 ns
t_{cp} = 20 ns
R.F. = 1 MHz
Amplitude = 3 V

Waveforms



Test circuit 2)

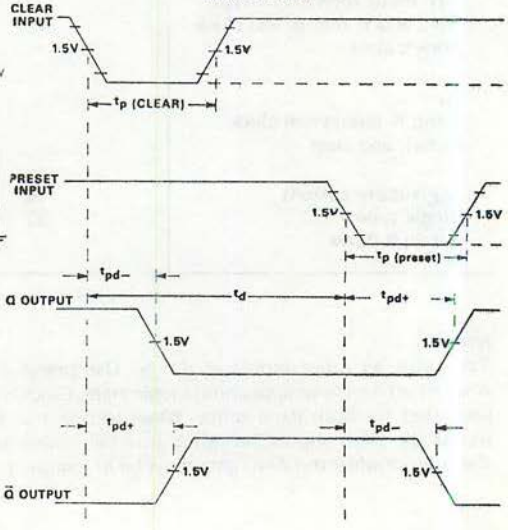


C_L includes probe and jig capacitance

Pulse Characteristics

Same as Test Circuit 1, except t_p = 16 ns.

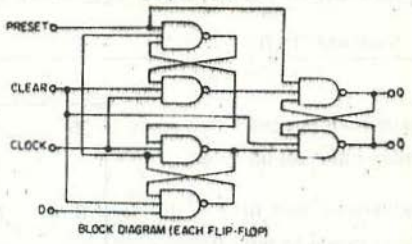
Waveforms



TYPICAL CHARACTERISTICS AND OPERATING CONDITIONS

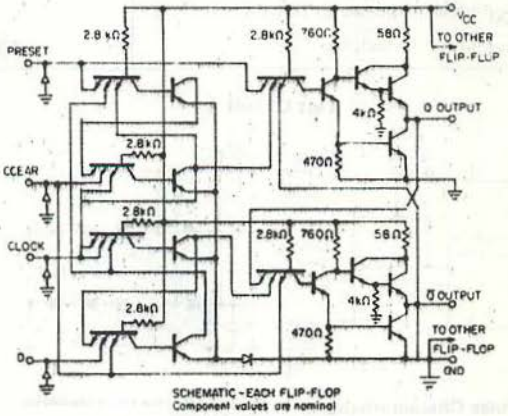
Maximum clock frequency	35 MHz
Propagation delay	11 ns
Power dissipation	150 mW
Input loading factor:	
Preset or data	1 unit load
Clear or clock	2 unit loads
Fan out	1 to 10 unit loads
Clock pulse width t_{cp}	15 ns min.
Preset or clear pulse width t_p	25 ns min.

Logic diagram



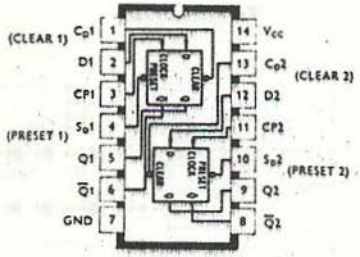
BLOCK DIAGRAM (EACH FLIP-FLOP)

Circuit diagram of one flip-flop



SCHEMATIC - EACH FLIP-FLOP
Component values are nominal

Pin configuration
(top view)



Truth Table

SYNCHRONOUS			ASYNCHRONOUS			
t_n	t_n+1		Preset	Clear	Q	$\overline{Q}$
D Input	Q	$\overline{Q}$	0	0	1	1
0	0	1	1	0	0	1
1	1	0	0	1	1	0
			1	1	No Control	

DESCRIPTION

The ITT74H74 is an edge triggered D type flip-flop in which the transfer of the D input data takes place during the positive transition of the clock input. When the clock input is above or below the transfer threshold the 'D' input is inhibited. The transfer threshold is not directly related to the transition time of the positive going edge. Preset and clear inputs operate irrespective of the logic state of the clock or D input.

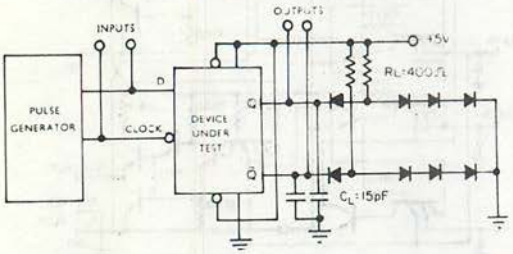
PARAMETER	LIMIT				CONDITIONS	
	Min.	Typ. at 25°C	Max.	Unit	V_{CC}	
$-I_F$ Preset or D input			2.0	mA	Max.	V_F=0.4V
Clear or clock			4.0	mA	Max.	V_F=0.4V
I_R D input			50	µA	Max.	V_R=2.4V
Preset or clock			100	µA	Max.	V_R=2.4V
All inputs			1	mA	Max.	V_R=5.5V
Clear			150	µA	Max.	V_R=2.4V
I_{CC} 54H74		30	42	mA	Max.	All inputs high
74H74		30	50	mA		

Information on the absolute maximum ratings and the other D.C. characteristics of this device (which are common to other integrated circuits in this series) is stated in the general information section.

SWITCHING CHARACTERISTICS V_{CC}=5.0V, T_{AMB}=25°C

PARAMETER	LIMIT				CONDITIONS
	Min.	Typ.	Max.	Unit	
f_{max} maximum input clock frequency	35	43		MHz	Use test circuit 1
t_{sp} minimum input set up time		10		ns	Use test circuit 1 ("Low" Data)
		15		ns	Use test circuit 1 ("High" Data)
t_h minimum input hold time	0			ns	Use test circuit 1
t_{pd+} clear or preset to output			20	ns	Use test circuit 2
t_{pd+} clock to output	4	8.5	15	ns	Use test circuit 1
t_{pd-} clear or preset to output			30	ns	Use test circuit 2
t_{pd-} clock to output	7	13	20	ns	Use test circuit 1

Test Circuit 1

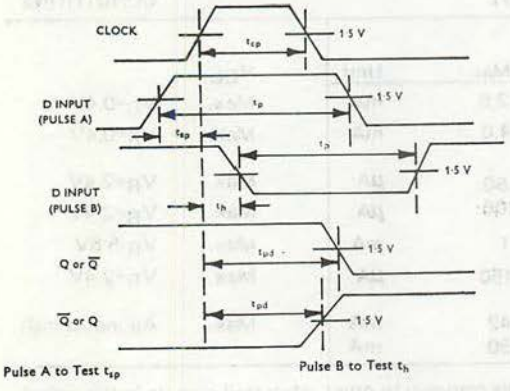


C_L includes probe and jig capacitance

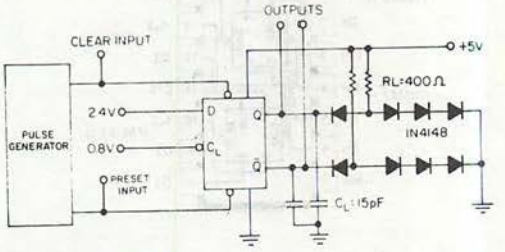
Pulse Characteristics

t_r = 7 ns
t_f = 7 ns
t_{cp} = 20 ns
t_p (D input) = 60 ns
R.F. clock = 1 MHz
R.F D input = ½ R.F clock
Amplitude = 3 V

Waveforms



Test Circuit 2

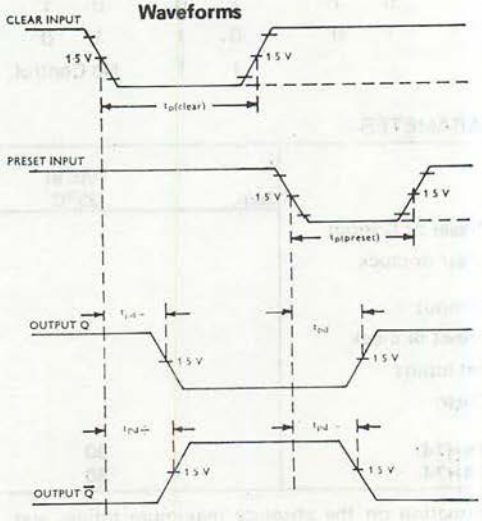


C_L includes probe and jig capacitance

Pulse Characteristics

t_r = 7 ns
t_f = 7 ns
t_p = 25 ns
R.F. = 1 MHz
Amplitude = 3 V

Waveforms



HIGH SPEED SATURATED TRANSISTOR-TRANSISTOR LOGIC CIRCUITS

- **Single power supply requirements: 5 volts optimum, 4.5 to 5.5 volts range**
- **High speed: typical gate propagation delay time of 7 ns**
- **High DC noise margin: typically one volt**
- **Added input diodes and low output impedance provides minimum AC noise susceptibility**
- **Fan Out: 10TTL loads**
- **Power dissipation: 11mw per NAND gate at a 50% duty cycle**
- **Compatible with ITT DTL family and other DTL and TTL circuits**
- **NAND gate pin configurations are compatible with DTL**

The ITT MIC9000 Series of TTL circuits is designed to be used in any digital system where good noise immunity, high speed, medium power and high fan-out performance is required. The line is characterized by a broad number of functions available in a variety of packages. The basic elements of the family are active low level output AND gates commonly known as NAND gates.

Typical high level noise immunity of every device in the family is 1.9 V and typical low level noise immunity is 0.9 V. Worst case immunity is 400 mV over the entire temperature range. Power dissipation is typically 11 mW per gate function at a 50% duty cycle, and the average propagation delay is 7 nanoseconds per gate function. A single 5 V ±10 per cent power supply is used with the circuits.

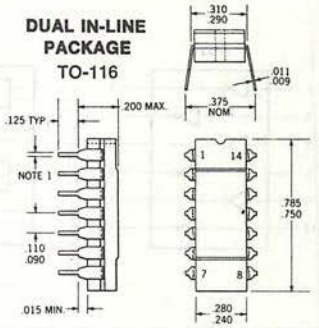
The gates were designed to provide low output impedance in both high and low states which results in good capacitive drive capability and good immunity to crosstalk. The output impedance in the low state is about 10 ohms and in the high state, about 20 ohms. To further enhance noise immunity, all inputs of all devices incorporate diode clamps which considerably reduces the ringing which can result from long lines and impedance mismatches. The binary elements are of a JK, DC master slave design and will toggle at 40 MHz, except for the 9000 element. The 9000 has capacitors purposely incorporated in the design to increase its set-up time and provide it with considerable immunity to long clock skew. Due to the longer set-up time the 9000 toggle frequency is 20 MHz. A common JK input is incorporated on all binary elements to provide data entry inhibit/enable. The input to the clock on each element is buffered to reduce the clock input loading.

The V_{CC} and ground terminals of all devices are located on diagonal corners of the package which allows two degrees of freedom in routing of power and ground leads on the PC boards. Special care has been taken in establishing pin-outs for the flip-flop so as to minimize cross-overs when laying out common dynamic functions with these elements. Simple loading rules are incorporated so that the fan-in and fan-out capability of each device will be quickly established.

The MIC9000 series TTL is compatible with DTL and MSI devices as well as the more complex functions which will be available in the future.

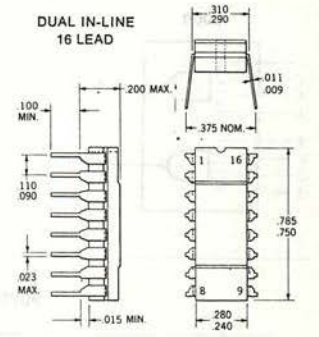
DIMENSIONS

DUAL IN-LINE PACKAGE
TO-116

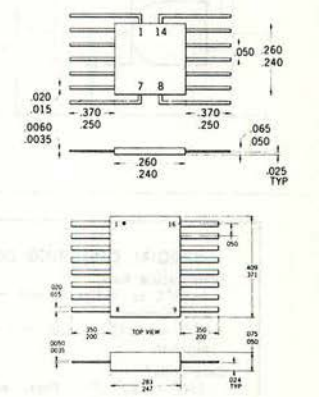


NOTE: 1. Board drilling dimensions should equal your practice for a conventional .020 inch diameter lead.

DUAL IN-LINE 16 LEAD



DIMENSIONS — FLAT PACK
TO-86



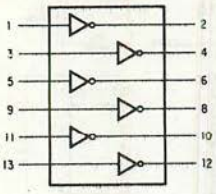
16 LEAD—check factory for availability

NOTE: All dimensions in inches

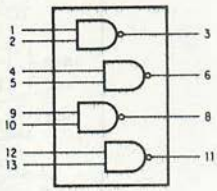
MIC9000 SERIES TTL INTEGRATED CIRCUITS

NAND GATES

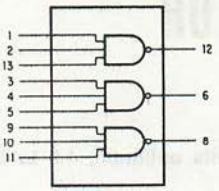
9016



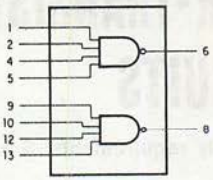
9002



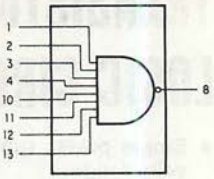
9003



9004

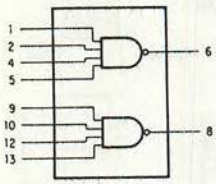


9007



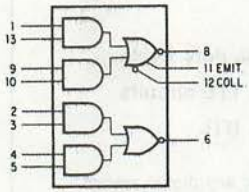
BUFFER

9009

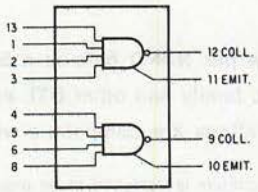


AND-OR-INVERT GATES AND EXTENDER

9005

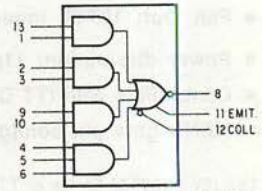


9006



(extender for use with 9005 & 9008)

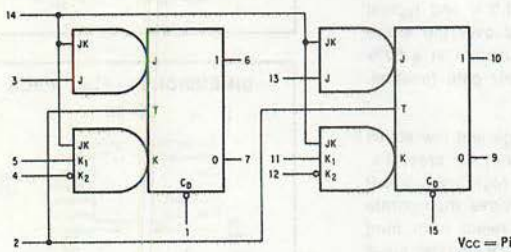
9008



V_{CC} = Pin 14
Gnd = Pin 7

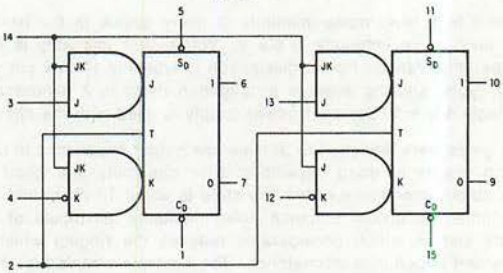
DUAL FLIP-FLOPS

9020



V_{CC} = Pin 16
Gnd = Pin 8

9022



SPECIAL ORDERING CODE

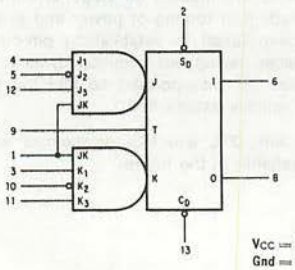
Temperature Range:
−55°C to +125°C, add −1 to MIC number.
0°C to +75°C, add −5 to MIC number.

Case Style:
.250" x .250" Flat Pack, add "B" following last digit.
Ceramic Dual In-Line, add "D" following last digit.

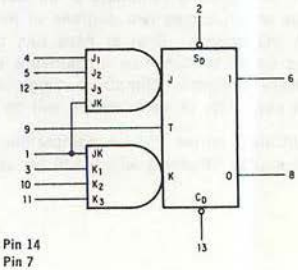
Example:
MIC 9002-1D is −55° to +125°C. Temperature range in Ceramic Dual-In-Line package.
Flat-pack and Dual-In-Line packages have same pin configuration.

SINGLE FLIP-FLOPS

9001



9000



V_{CC} = Pin 14
Gnd = Pin 7

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias (MIC9000-1)	−55°C to +125°C
Temperature (Ambient) Under Bias (MIC9000-5)	0°C to +75°C
V_{CC} Pin Potential to Ground (See Note 1)	−0.5V to +8.0V
Input Voltage (D.C.) (See Note 2)	−0.5V to +5.5V
Input Current (See Note 2)	−30 mA to +5.0 mA
Output Voltage, Output Normally High	0 V to +V_{CC} value
Current Into Output Terminal, Output Low (except 9009)	50 mA
Current Into Output Terminal, Output Low 9009	100 mA

NOTE 1

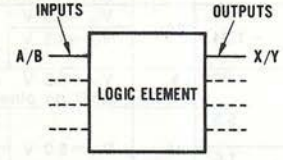
The maximum V_{CC} value of 8.0 volts is not the primary factor in determining the maximum V_{CC} which may be applied to a number of interconnected devices. The voltage at a high output is approximately 2 V_{BE}'s below the V_{CC} voltage, so the primary limit on the V_{CC} is that the voltage at any input may not go above 5.5 V unless the current is limited, so this effectively limits the system V_{CC} to approximately 7.0 volts.

NOTE 2

Because of the input clamp diodes, excess current can be drawn out of the inputs if the D.C. input voltage is more negative than −0.5 V. The diode is designed to clamp off large negative A.C. swings associated with fast fall times and long lines. This maximum rating is intended only to limit the steady state input voltage and current.

LOADING RULES

In this data sheet the following notation has been chosen to indicate the input loading and output drive for all logic elements.



Where A = high logic level input load factor
B = low logic level input load factor
X = high logic level output drive factor
Y = low logic level output drive factor

When checking for loading violations it is only necessary to insure that the sum of the high logic level input load factors at any node does not exceed the high logic level output drive factor at that node. The same is true for the low level load and drive factors. These rules apply only within the TTL MIC9000 series.

Multiplying the factor with the appropriate current per unit load gives the input loading or output drive in terms of current. For the TTL circuits of this data sheet, current per unit is −1.6 mA maximum at the low logic level and is 60 μA maximum at the high logic level.

In the case where unused inputs of an AND gate are shorted to a driven input, the high logic level input load factor for the inputs will be the number of inputs shorted together times the high logic input load factor for one input. The low logic level input load factor for the inputs will be the same as that for a single input.

UNUSED INPUTS

Proper termination of unused inputs will result in maximum operating speed. Substantial degradation of turn-on delay may occur if unused inputs are left open.

The following are acceptable ways to terminate unused inputs:

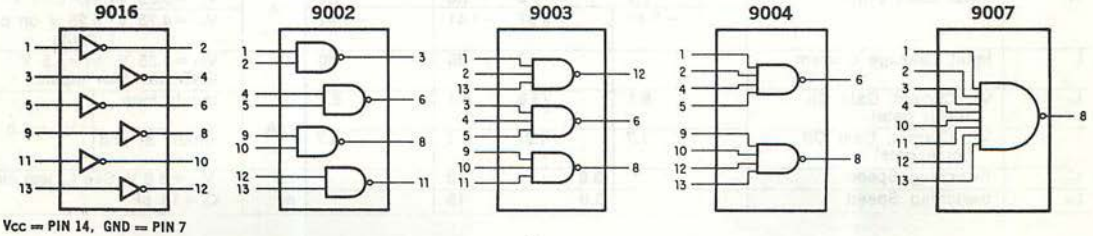
1. Tie the input to a used input on the same gate. The TTL 9000 series has made special provision for this method by offering extra high level drive factor on all outputs.
2. Tie the input to V_{CC} through a resistor. This resistor should be chosen to keep the input current within absolute maximum ratings for any possible extreme of the V_{CC} supply. More than one input may be terminated through one resistor.
3. Tie inputs to a separate supply between 4.5 and 2.4 V, if one should be available.
4. Tie the inputs to the output of an unused gate. The unused gate must provide a constant high level output.

NAND GATES — 9002, 9003, 9004 AND 9007

HEX INVERTER — 9016

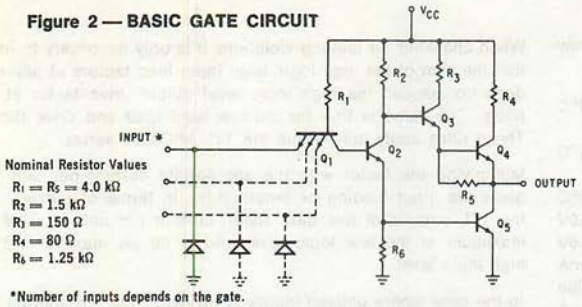
The 9002, 9003, 9004 and 9007 are active low level output AND gates commonly known as NAND gates. The 9016 is a hex inverter with input and output characteristics identical to the 9002, 9003, 9004 and 9007. The variety of gate combinations provides the system designer the utmost in logic flexibility and reduces package count.

Figure 1 — LOGIC SYMBOL AND PIN CONFIGURATIONS



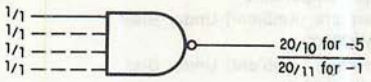
V_{CC} = PIN 14, GND = PIN 7

Figure 2 — BASIC GATE CIRCUIT



*Number of inputs depends on the gate.

Figure 3 — LOADING FACTORS



ELECTRICAL CHARACTERISTICS 9002, 9003, 9004, 9007 AND 9016 (T_A = −55°C to 125°C, V_{CC} = 5.0 V ± 10%)

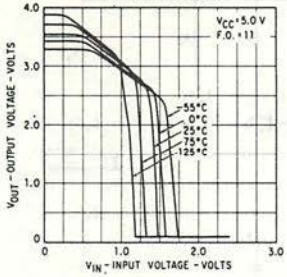
SYMBOL	CHARACTERISTIC	LIMITS −55°C MIN.	LIMITS −55°C MAX.	LIMITS 25°C MIN.	LIMITS 25°C TYP.	LIMITS 25°C MAX.	LIMITS 125°C MIN.	LIMITS 125°C MAX.	UNITS	CONDITIONS
V_{OH}	Output High Voltage	2.4		2.4	2.7		2.4		Volts	V_{CC} = 4.5 V I_{OH} = −1.32 mA Inputs at V_{IL} (see below)
V_{OL}	Output Low Voltage		0.4		0.21	0.4		0.4	Volts	V_{CC} = 5.5 V I_{OL} = 17.6 mA V_{IH} = 5.5 V
										V_{CC} = 4.5 V I_{OL} = 13.6 mA Inputs at V_{IH} (see below)
V_{IH}	Input High Voltage	2.0		1.7			1.4		Volts	Guaranteed input high threshold for all inputs
V_{IL}	Input Low Voltage		0.8			0.9		0.8	Volts	Guaranteed input low threshold for all inputs
I_F	Input Load Current		−1.6		−1.1	−1.6		−1.6	mA	V_{CC} = 5.5 V V_F = 0.4 V
			−1.24		−0.87	−1.24		−1.24		V_{CC} = 4.5 V 5.5 V on other inputs
I_R	Input Leakage Current				10	60		60	μA	V_{CC} = 5.5 V V_R = 4.5 V GND on other inputs
I_{PD}	V_{CC} Current, Gate On (each gate)		5.5		3.5	5.5		5.5	mA	V_{CC} = 5.0 V Inputs high
	V_{CC} Current, Gate Off (each gate)		1.6		1.07	1.6		1.6		V_{CC} = 5.0 V Inputs at gnd
t_{pd+}	Switching Speed			3.0		10			ns	V_{CC} = 5.0 V, See t_{pd} test circuit
t_{pd-}	Switching Speed			3.0		12			ns	C_L = 15 pF

ELECTRICAL CHARACTERISTICS 9002, 9003, 9004, 9007 AND 9016 (T_A = 0°C to 75°C, V_{CC} = 5.0 V ± 5%)

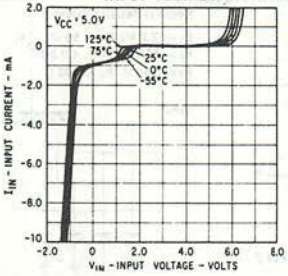
SYMBOL	CHARACTERISTIC	LIMITS 0°C MIN.	LIMITS 0°C MAX.	LIMITS 25°C MIN.	LIMITS 25°C TYP.	LIMITS 25°C MAX.	LIMITS 75°C MIN.	LIMITS 75°C MAX.	UNITS	CONDITIONS
V_{OH}	Output High Voltage	2.4		2.4	2.9		2.4		Volts	V_{CC} = 4.75V I_{OH} = −1.2 mA Inputs at V_{IL} (see below)
V_{OL}	Output Low Voltage		0.45		0.21	0.45		0.45	Volts	V_{CC} = 5.25 V I_{OL} = 16.0 mA V_{IH} = 5.25 V
										V_{CC} = 4.75 V I_{OL} = 14.1 mA Inputs at V_{IH} (see below)
V_{IH}	Input High Voltage	1.9		1.8			1.6		Volts	Guaranteed input high threshold for all inputs
V_{IL}	Input Low Voltage		0.85			0.85		0.85	Volts	Guaranteed input low threshold for all inputs
I_F	Input Load Current		−1.6		−1.0	−1.6		−1.6	mA	V_{CC} = 5.25 V V_F = 0.45 V
			−1.41		−0.91	−1.41		−1.41		V_{CC} = 4.75 V 5.25 V on other inputs
I_R	Input Leakage Current				10	60		60	μA	V_{CC} = 5.25 V V_R = 4.5 V GND on other inputs
I_{PD}	V_{CC} Current, Gate On (each gate)		6.1		3.6	6.1		6.1	mA	Inputs high V_{CC} = 5.0 V
	V_{CC} Current, Gate Off (each gate)		1.7		1.07	1.7		1.7		Inputs at gnd V_{CC} = 5.0 V
t_{pd+}	Switching Speed			3.0		13			ns	V_{CC} = 5.0 V, See t_{pd} test circuit
t_{pd-}	Switching Speed			3.0		15			ns	C_L = 15 pF

TYPICAL INPUT AND OUTPUT CHARACTERISTICS 9002, 9003, 9004, 9007 AND 9016

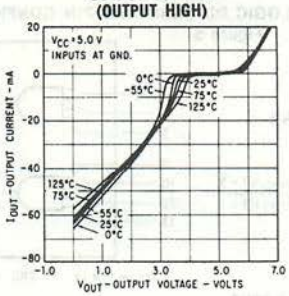
OUTPUT VOLTAGE VERSUS INPUT VOLTAGE



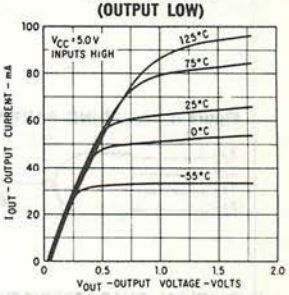
INPUT CURRENT VERSUS INPUT VOLTAGE



OUTPUT CURRENT VERSUS OUTPUT VOLTAGE (OUTPUT HIGH)

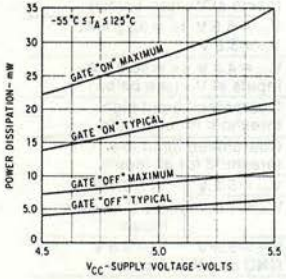


OUTPUT CURRENT VERSUS OUTPUT VOLTAGE (OUTPUT LOW)

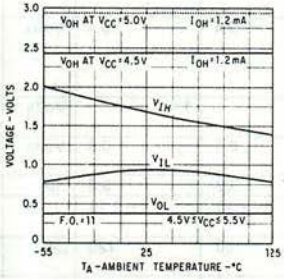


POWER DISSIPATION, LOGIC LEVELS AND NOISE IMMUNITY

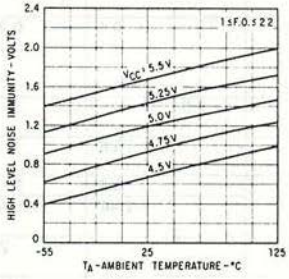
POWER DISSIPATION VERSUS SUPPLY VOLTAGE



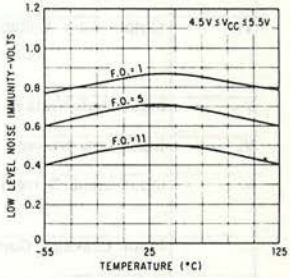
WORST CASE LOGIC LEVELS VERSUS AMBIENT TEMPERATURE



WORST CASE HIGH LEVEL NOISE IMMUNITY VERSUS AMBIENT TEMPERATURE



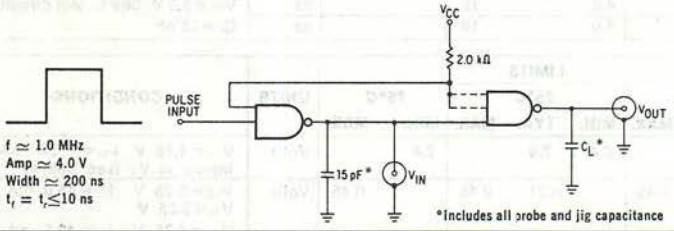
WORST CASE LOW LEVEL NOISE IMMUNITY VERSUS AMBIENT TEMPERATURE



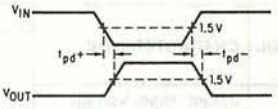
SWITCHING CHARACTERISTICS

$f \simeq 1.0$ MHz
Amp $\simeq 4.0$ V
Width $\simeq 200$ ns
$t_r = t_f \leq 10$ ns

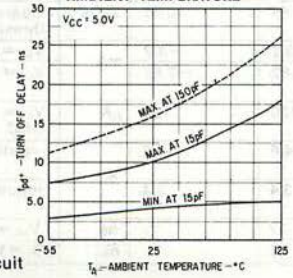
tpd TEST CIRCUIT



SWITCHING WAVEFORM

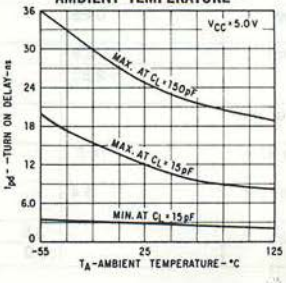


WORST CASE TURN OFF DELAY VERSUS AMBIENT TEMPERATURE*



*See t_{pd} test circuit

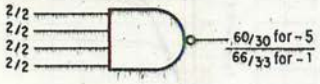
WORST CASE TURN ON DELAY VERSUS AMBIENT TEMPERATURE*



NAND BUFFER — 9009

The 9009 is a power gate capable of sinking and sourcing large currents for high fanout applications. Logically it is the same as the 9004.

Figure 4 LOADING FACTORS



LOGIC DIAGRAM AND PIN CONFIGURATION
Figure 5

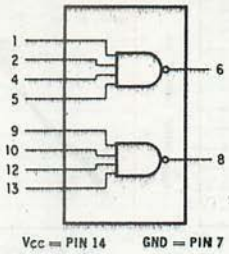
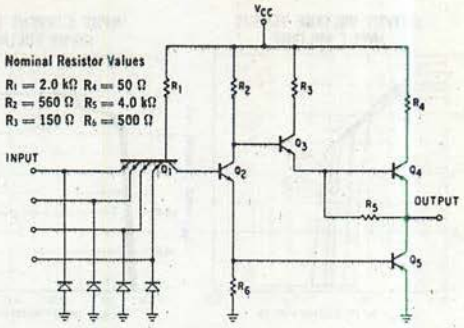


Figure 6 CIRCUIT DIAGRAM (One Gate)



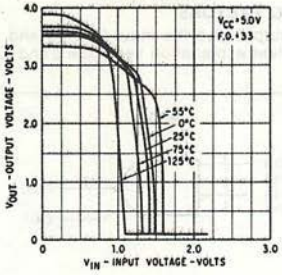
ELECTRICAL CHARACTERISTICS 9009

SYMBOL	CHARACTERISTIC	LIMITS −55°C MIN.	LIMITS −55°C MAX.	LIMITS 25°C MIN.	LIMITS 25°C TYP.	LIMITS 25°C MAX.	LIMITS 125°C MIN.	LIMITS 125°C MAX.	UNITS	CONDITIONS
V_{OH}	Output High Voltage	2.4		2.4	2.7		2.4		Volts	V_{CC} = 4.5 V I_{OH} = −3.96 mA Inputs at V_{IL} (see below)
V_{OL}	Output Low Voltage		0.4		0.21	0.4		0.4	Volts	V_{CC} = 5.5 V I_{OL} = 52.8 mA V_{IH} = 5.5 V
										V_{CC} = 4.5 V I_{OL} = 40.8 mA Inputs at V_{IH} (see below)
V_{IH}	Input High Voltage	2.0		1.7			1.4		Volts	Guaranteed input high threshold for all inputs
V_{IL}	Input Low Voltage		0.8			0.9		0.8	Volts	Guaranteed input low threshold for all inputs
I_F	Input Load Current		3.2		2.15	3.2		3.2	mA	V_{CC} = 5.5 V V_F = 0.4 V
			−2.48		−1.74	−2.48		−2.48		V_{CC} = 4.5 V 5.5 V on other inputs
I_R	Input Leakage Current				20	120		120	μA	V_{CC} = 5.5 V V_R = 4.5 V GND on other inputs
I_{PD}	V_{CC} Current, Gate On (each gate)		12.9		8.6	12.9		12.9	mA	V_{CC} = 5.0 V Inputs high
	V_{CC} Current, Gate Off (each gate)		3.2		2.15	3.2		3.2		V_{CC} = 5.0 V Inputs grounded
t_{pd+}	Switching Speed			4.0		15			ns	V_{CC} = 5.0 V, See t_{pd} test circuit
t_{pd-}	Switching Speed			3.0		10			ns	C_L = 15 pF

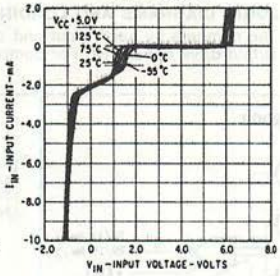
SYMBOL	CHARACTERISTIC	LIMITS 0°C MIN.	LIMITS 0°C MAX.	LIMITS 25°C MIN.	LIMITS 25°C TYP.	LIMITS 25°C MAX.	LIMITS 75°C MIN.	LIMITS 75°C MAX.	UNITS	CONDITIONS
V_{OH}	Output High Voltage	2.4		2.4	2.9		2.4		Volts	V_{CC} = 4.75 V I_{OH} = −3.6 mA Inputs at V_{IL} (see below)
V_{OL}	Output Low Voltage		0.45		0.21	0.45		0.45	Volts	V_{CC} = 5.25 V I_{OL} = 48.0 mA V_{IH} = 5.25 V
										V_{CC} = 4.75 V I_{OL} = 42.3 mA Inputs at V_{IH} (see below)
V_{IH}	Input High Voltage	1.9		1.8			1.6		Volts	Guaranteed input high threshold for all inputs
V_{IL}	Input Low Voltage		0.85			0.85		0.85	Volts	Guaranteed input low threshold for all inputs
I_F	Input Load Current		−3.2		−2.0	−3.2		−3.2	mA	V_{CC} = 5.25 V V_F = 0.45 V
			−2.82		−1.82	−2.82		−2.82		V_{CC} = 4.75 V 5.25 V on other inputs
I_R	Input Leakage Current				20	120		120	μA	V_{CC} = 5.25 V V_R = 4.5 V GND on other inputs
I_{PD}	V_{CC} Current, Gate On (each gate)		14.6		8.6	14.6		14.6	mA	Inputs high V_{CC} = 5.0 V
	V_{CC} Current, Gate Off (each gate)		3.4		2.15	3.4		3.4		Inputs at gnd V_{CC} = 5.0 V
t_{pd+}	Switching Speed			3.0		17			ns	V_{CC} = 5.0 V, See t_{pd} test circuit
t_{pd-}	Switching Speed			2.0		13			ns	C_L = 15 pF

TYPICAL INPUT AND OUTPUT CHARACTERISTICS 9009

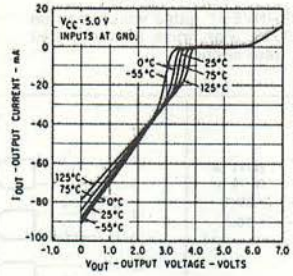
OUTPUT VOLTAGE VERSUS INPUT VOLTAGE



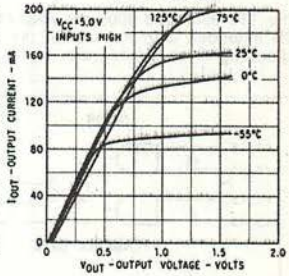
INPUT CURRENT VERSUS INPUT VOLTAGE



OUTPUT CURRENT VERSUS OUTPUT VOLTAGE

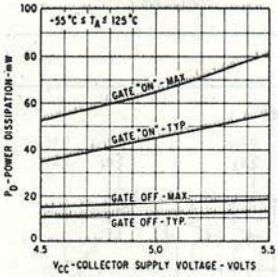


OUTPUT CURRENT VERSUS OUTPUT VOLTAGE (OUTPUT LOW)

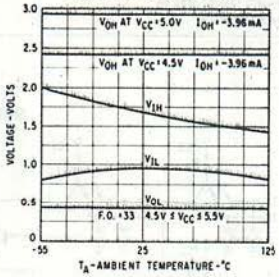


POWER DISSIPATION, LOGIC LEVELS AND NOISE IMMUNITY

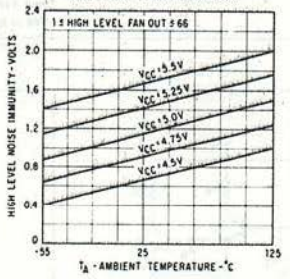
POWER DISSIPATION VERSUS SUPPLY VOLTAGE



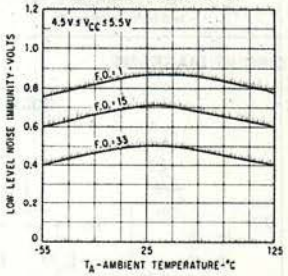
WORST CASE LOGIC LEVELS VERSUS AMBIENT TEMPERATURE



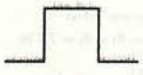
WORST CASE HIGH LEVEL NOISE IMMUNITY VERSUS AMBIENT TEMPERATURE



WORST CASE LOW LEVEL NOISE IMMUNITY VERSUS AMBIENT TEMPERATURE

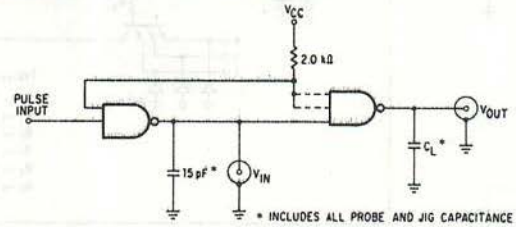


SWITCHING CHARACTERISTICS

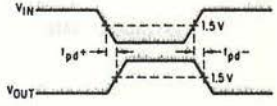


f ≃ 1.0 MHz
Amp ≃ 4.0 V
Width ≃ 200 ns
t_r ≃ t_f ≤ 10 ns

tpd TEST CIRCUIT

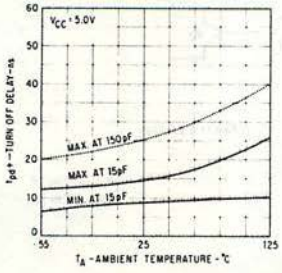


SWITCHING WAVEFORM

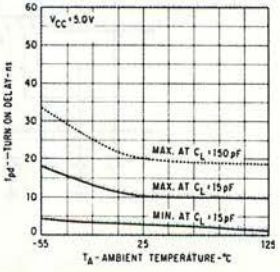


9009-1

WORST CASE TURN OFF DELAY VERSUS AMBIENT TEMPERATURE*

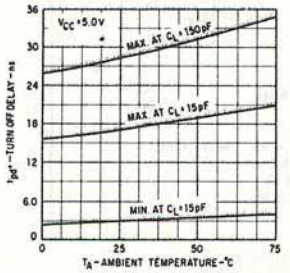


WORST CASE TURN ON DELAY VERSUS AMBIENT TEMPERATURE

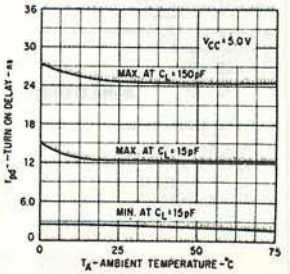


9009-5

WORST CASE TURN OFF DELAY VERSUS AMBIENT TEMPERATURE*



WORST CASE TURN ON DELAY VERSUS AMBIENT TEMPERATURE*



* See t_{pd} test circuit.

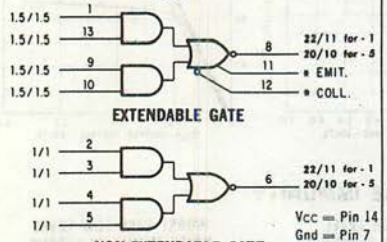
EXTENDABLE AND-OR-INVERT GATES — 9005, 9008
EXTENDER — 9006

The TTL 9005 and 9008 are AND-OR-INVERT gates which may be OR extended with the use of the 9006. For noise immunity and operating level curves, refer to the gate section.

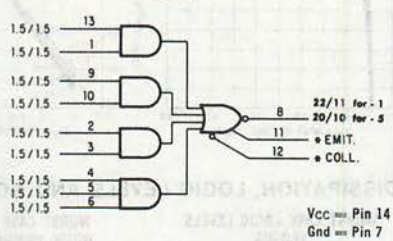
LOGIC DIAGRAMS AND LOADING FACTORS

The numbers by each input and output give the input loading and output drive capability. For complete explanation see Page 2 and 3.

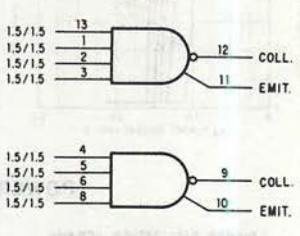
9005



9008

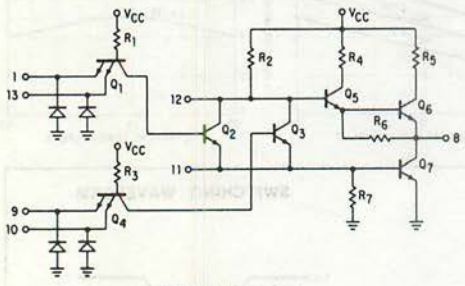


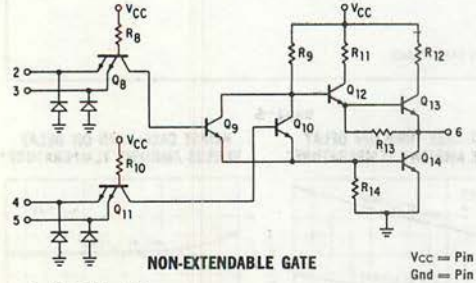
9006



CIRCUIT DIAGRAMS

9005

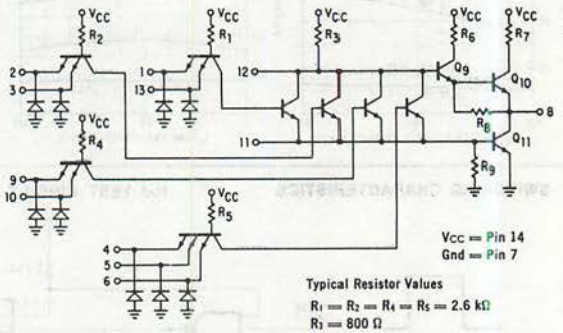




Typical Resistor Values

$R_1 = R_3 = 2.6\ k\Omega$
$R_2 = 800\ \Omega$
$R_4 = R_{11} = 150\ \Omega$
$R_5 = R_{12} = 80\ \Omega$
$R_6 = R_8 = R_{10} = R_{13} = 4.0\ k\Omega$
$R_7 = 665\ \Omega$
$R_9 = 1.5\ k\Omega$
$R_{14} = 1.25\ k\Omega$

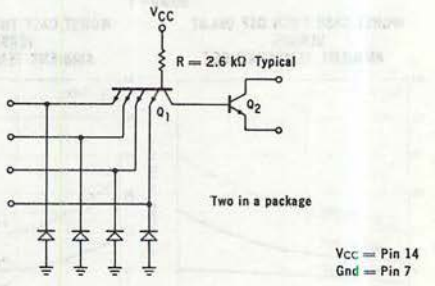
9008



Typical Resistor Values

$R_1 = R_2 = R_4 = R_5 = 2.6\ k\Omega$
$R_3 = 800\ \Omega$
$R_6 = 150\ \Omega$
$R_7 = 80\ \Omega$
$R_8 = 4.0\ k\Omega$
$R_9 = 665\ \Omega$

9006



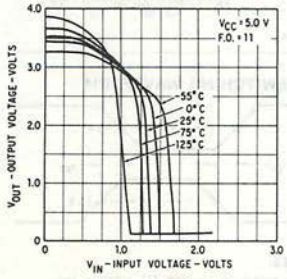
ELECTRICAL CHARACTERISTICS 9005, 9006 AND 9008 ($T_A = -55°C$ to $125°C$, $V_{CC} = 5.0\ V \pm 10\%$)

SYMBOL	CHARACTERISTIC	LIMITS −55°C MIN.	LIMITS −55°C MAX.	LIMITS 25°C MIN.	LIMITS 25°C TYP.	LIMITS 25°C MAX.	LIMITS 125°C MIN.	LIMITS 125°C MAX.	UNITS	CONDITIONS & COMMENTS
V_{OH}	Output High Voltage	2.4		2.4	2.7		2.4		Volts	$V_{CC} = 4.5\ V$ $I_{OH} = -1.32\ mA$ V_{IL} = value indicated below on this table
V_{OL}	Output Low Voltage		0.4		0.2	0.4		0.4	Volts	$V_{CC} = 5.5\ V$ $I_{OL} = 17.6\ mA$ $V_{IH} = 5.5\ V$
										$V_{CC} = 4.5\ V$ $I_{OL} = 13.6\ mA$ V_{IH} = (see below)
V_{IH}	Input High Voltage	2.0		1.7			1.4		Volts	Guaranteed input high threshold for all inputs
V_{IL}	Input Low Voltage		0.8			0.9		0.8	Volts	Guaranteed input low threshold for all inputs
I_F	Input Load Current		−1.6		−1.1	−1.6		−1.6	mA	$V_{CC} = 5.5\ V$
	9005 Non-Extendable Gate		−1.24		−0.87	−1.24		−1.24		$V_{CC} = 4.5\ V$
	Input Load Current		−2.4		−1.5	−2.4		−2.4	μA	$V_{CC} = 5.5\ V$
	Extendable Gate and Extender		−1.86		−1.31	−1.86		−1.86		$V_{CC} = 4.5\ V$
										$V_F = 0.4\ V$, 5.5 V on other inputs
I_R	Input Leakage Current 9005 Non-Extendable Gate				5.0	60		60	mA	$V_{CC} = 5.5\ V$ $V_R = 4.5\ V$
	Input Leakage Current Extendable Gate and Extender				7.5	90		90		Gnd on all other inputs
I_{PD}	V_{CC} Current, Gate "ON" 9005 Non-Extendable Gate		6.5		4.5	6.5		6.5	mA	$V_{CC} = 5.0\ V$
	9005 Extendable Gate		11.3		7.6	11.3		11.3		All inputs open
	9008		12.5		9.3	12.5		12.5		
	V_{CC} Current, Gate "OFF" 9005 Non-Extendable Gate		3.1		2.1	3.1		3.1	mA	$V_{CC} = 5.0\ V$
	9005 Extendable Gate		4.7		3.3	4.7		4.7		All inputs except extender inputs gnd.
	9008		9.4		6.6	9.4		9.4		
ΔI_{PD}	Extra Current Drain from one 9006 Extender Gate "ON"		1.61		1.08	1.61		1.61	mA	$V_{CC} = 5.0\ V$ All inputs high 9006 attached to a 9005
	Extra Current Drain from one 9006 Extender Gate "OFF"		2.35		1.65	2.35		2.35	mA	$V_{CC} = 5.0\ V$ All inputs grounded 9006 attached to a 9005

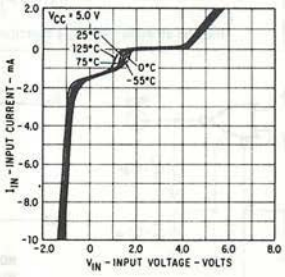
Note: Output characteristics apply to a 9005 (both gates) or a 9008.
Input characteristics apply to a 9005 (both gates) or a 9008 using either the internal gates or an external 9006 extender.

9005, 9006, 9008
TYPICAL INPUT-OUTPUT CHARACTERISTICS
(EXTENDABLE GATES*)

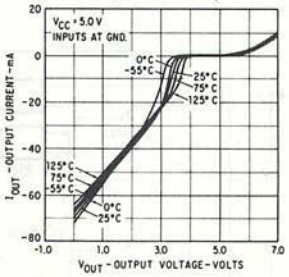
OUTPUT VOLTAGE VERSUS INPUT VOLTAGE



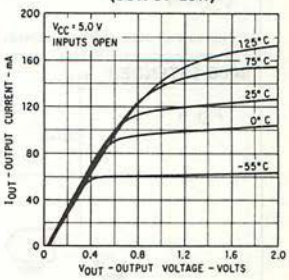
INPUT CURRENT VERSUS INPUT VOLTAGE



OUTPUT CURRENT VERSUS OUTPUT VOLTAGE (OUTPUT HIGH)



OUTPUT CURRENT VERSUS OUTPUT VOLTAGE (OUTPUT LOW)



*Curves on Page 6 apply to 9005 nonextendable gate.

ELECTRICAL CHARACTERISTICS 9005, 9006 AND 9008 ($T_A = 0°C$ to $75°C$, $V_{CC} = 5.0\ V \pm 5\%$)

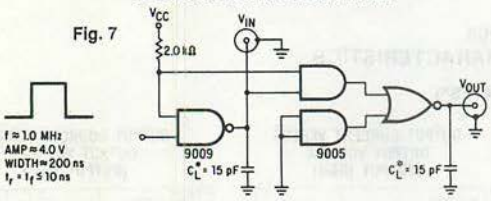
SYMBOL	CHARACTERISTIC	LIMITS 0°C MIN.	0°C MAX.	25°C MIN.	25°C TYP.	25°C MAX.	75°C MIN.	75°C MAX.	UNITS	CONDITIONS
V_{OH}	Output High Voltage	2.4		2.4	2.9		2.4		Volts	$V_{CC} = 4.75\ V$, $I_{OH} = -1.2\ mA$; V_{IL} = value indicated below on this table
V_{OL}	Output Low Voltage		0.45		0.2	0.45		0.45	Volts	$V_{CC} = 5.25\ V$, $I_{OL} = 16.0\ mA$; $V_{CC} = 4.75\ V$, $I_{OL} = 14.1\ mA$
V_{IH}	Input High Voltage	1.9		1.8			1.6		Volts	Guaranteed input high threshold for all inputs
V_{IL}	Input Low Voltage		0.85			0.85		0.85	Volts	Guaranteed input low threshold for all inputs
I_F	Input Load Current		−1.6		−1.04	−1.6		−1.6	mA	$V_{CC} = 5.25\ V$; $V_F = 0.45\ V$, 5.25 V on other inputs
	9005 Non-Extendable Gate		−1.41		−0.79	−1.41		−1.41		$V_{CC} = 4.75\ V$; $V_F = 0.45\ V$, 5.25 V on other inputs
	Input Load Current		−2.4		−1.56	−2.4		−2.4	mA	$V_{CC} = 5.25\ V$; $V_F = 0.45\ V$, 5.25 V on other inputs
	9005 Extendable Gates and Extender		−2.12		−1.19	−2.12		−2.12		$V_{CC} = 4.75\ V$; $V_F = 0.45\ V$, 5.25 V on other inputs
I_R	Input Leakage Current 9005 Non-Extendable Gate				5.0	60		60	μA	$V_R = 4.5\ V$, $V_{CC} = 4.75\ V$, Gnd on all other inputs
	Input Leakage Current Extendable Gates and Extender				7.5	90		90		$V_R = 4.5\ V$, $V_{CC} = 4.75\ V$, Gnd on all other inputs
I_{PD}	V_{CC} Current, Gate "ON"								mA	$V_{CC} = 5.0\ V$, All inputs open
	9005 Non-Extendable Gate		7.7		4.5	7.7		7.7		$V_{CC} = 5.0\ V$, All inputs open
	9005 Extendable Gate		13.6		7.6	13.6		13.6		$V_{CC} = 5.0\ V$, All inputs open
	9008		17.7		9.3	17.7		17.7		$V_{CC} = 5.0\ V$, All inputs open
	V_{CC} Current, Gate "OFF"								mA	$V_{CC} = 5.0\ V$, All inputs except extender inputs gnd.
	9005 Non-Extendable Gate		3.4		2.2	3.4		3.4		$V_{CC} = 5.0\ V$, All inputs except extender inputs gnd.
	9005 Extendable Gate		5.1		3.3	5.1		5.1		$V_{CC} = 5.0\ V$, All inputs except extender inputs gnd.
	9008		10.2		6.6	10.2		10.2		$V_{CC} = 5.0\ V$, All inputs except extender inputs gnd.
ΔI_{PD}	Extra Current Drain when one 9006 Extender is attached to a 9005 Gate "ON"		2.05		1.08	2.05		2.05	mA	$V_{CC} = 5.0\ V$, All inputs high
	Extra Current Drain when one 9006 Extender is attached to a 9005 Gate "OFF"		2.54		1.65	2.54		2.54	mA	$V_{CC} = 5.0\ V$, All inputs grounded

Note: Output characteristics above apply to a 9005 (both gates) or a 9008.
Input characteristics above apply to a 9005 (both gates) or a 9008 using either the internal gates or an external 9006 extender.

AC CHARACTERISTICS tpd TEST CIRCUIT

9005 NON-EXTENDABLE GATE

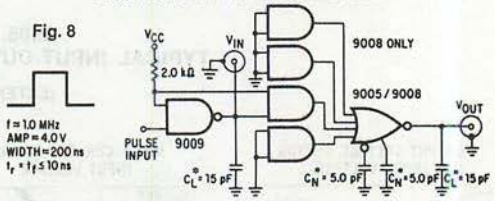
Fig. 7



*Includes all probe and/or jig capacitance.

9005 OR 9008 EXTENDABLE GATE

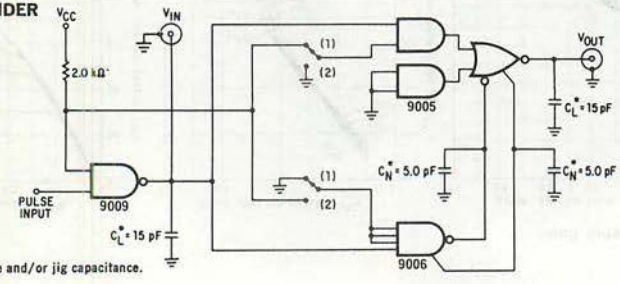
Fig. 8



*Includes all probe and/or jig capacitance.

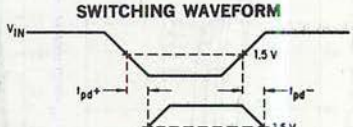
9006 EXTENDER

Fig. 9



*Includes all probe and/or jig capacitance.

SWITCHING WAVEFORM



NOTES:
With switch in position (1) measure tpd of 9005. With switch in position (2) measure tpd (9005) + Δtpd (9006). Capacitances include probe and jig capacitances.

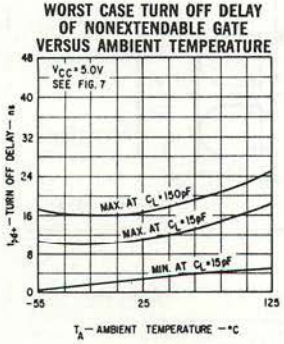
AC CHARACTERISTICS ($T_A = 25°C$) **9005-1, 9006-1, AND 9008-1**

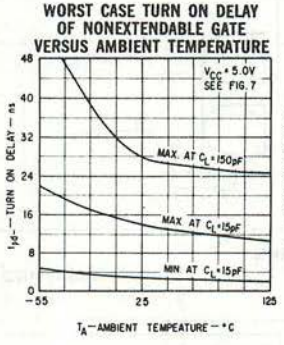
SYMBOL	LIMITS MIN.	LIMITS MAX.	UNITS	CONDITIONS & COMMENTS
t_{pd+}	3.0	15	ns	$V_{CC} = 5.0$ V, $C_L = 15$ pF
t_{pd-}	3.0	15		9005 Nonextendable gate only, See Fig. 7
t_{pd+}	3.0	18	ns	$V_{CC} = 5.0$ V, $C_L = 15$ pF, $C_N = 5.0$ pF
t_{pd-}	3.0	13		9005 Extendable gate and 9008, See Fig. 8
Δt_{pd+}	−3.0	5.0	ns	9006 only
Δt_{pd-}	−3.0	5.0		The 9006 is tested by measuring its propagation time through the 9005. The t_{pd} readings shall not exceed the 9005 readings by the specified amount. See Fig. 9.
Symbols are defined in the test circuit.				

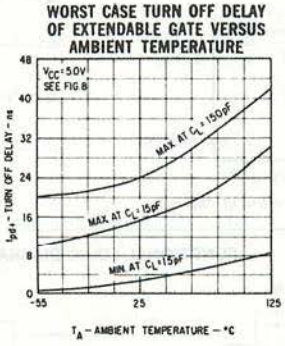
AC CHARACTERISTICS ($T_A = 25°C$) **9005-5, 9006-5, AND 9008-5**

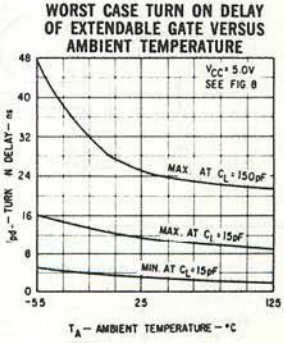
SYMBOL	LIMITS MIN.	LIMITS MAX.	UNITS	CONDITIONS & COMMENTS
t_{pd+}	3.0	12	ns	$V_{CC} = 5.0$ V, $C_L = 15$ pF
t_{pd-}	3.0	14		9005 Nonextendable gate only, See Fig. 7
t_{pd+}	3.0	15	ns	$V_{CC} = 5.0$ V, $C_L = 15$ pF, $C_N = 5.0$ pF
t_{pd-}	3.0	12		9005 Extendable gate and 9008, See Fig. 8
Δt_{pd+}	−2.0	4.0	ns	9006 only
Δt_{pd-}	−2.0	4.0		The 9006 is tested by measuring its propagation time through the 9005. The t_{pd} readings shall not exceed the 9005 readings by the specified amount. See Fig. 9.
Symbols are defined in the test circuit.				

9005-1, 9006-1 AND 9008-1









J-K FLIP-FLOPS — 9000, 9001, DUAL J-K FLIP-FLOPS — 9020, 9022

The TTL 9000 series has four flip-flops to satisfy the storage requirements of a logic system. All are master-slave JK designs and have the same high speed and high noise immunity as the rest of the 9000 series. As with the gates, all inputs have diode clamps to further enhance the noise immunity.

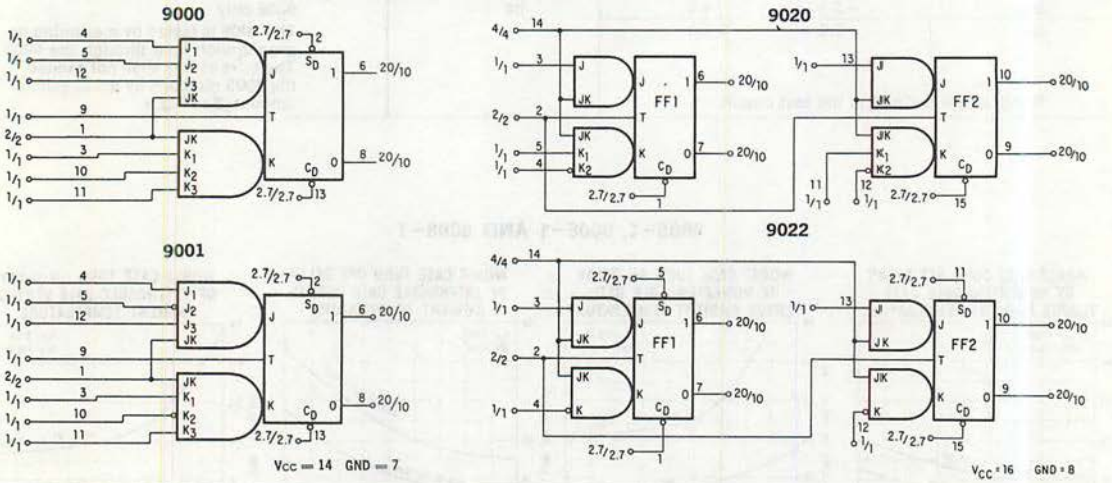
The JK type flip-flop was chosen for all flip-flop elements in this family because of its inherent logic power. The input function required to produce a given sequency of states for a JK flip-flop will, in general, contain more "don't care" conditions than the corresponding function for an RS flip-flop. These additional "don't care" conditions will, in most cases, reduce the amount of gating elements required to implement the input function.

The master-slave design offers the advantage of a DC threshold on the clock input initiating the transition of the outputs, so that careful control of clock pulse rise and fall times is not required.

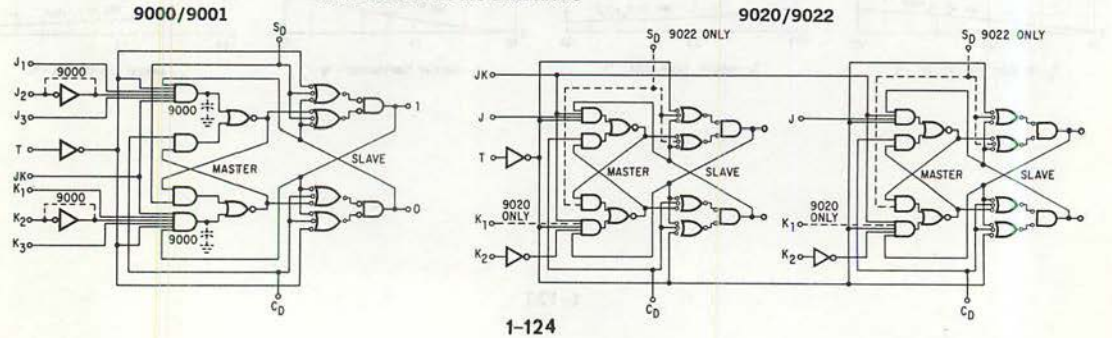
Data is accepted by the master while the clock is in the low state. Refer to the truth table for definition of "ONE" and "ZERO" data. Transfer from the master to the slave occurs on the low to high transition of the clock. When the clock is high, the J and K inputs are inhibited.
A joint (JK) input is provided for all flip-flops in this family. This common input removes the necessity of gating the clock signal with an external gate in many applications. This not only reduces package count, but also reduces the possibility of clock skew problems, since with internal gating provided, all flip-flops may be driven from a common clock line. Several TTL drivers may be used in parallel to drive this common clock line, if the load exceeds the F.O. capability of the 9009 buffer.

The asynchronous inputs provide ability to control the state of the flip-flop independent of static conditions of the clock and synchronous inputs. Both asynchronous set and clear are provided on all flip-flops except the 9020, which because of a logic trade-off has only clear inputs. The set or clear pin being low absolutely guarantees that one output will be high, but if opposing data is present at the synchronous inputs and the flip-flop is clocked, the low output may momentarily spike high synchronous with a positive transition of the clock. If the low output of the flip-flop is connected to other flip-flop inputs clocked from the same line, the spike will be masked by the clock. If the clock is suspended during the time when the asynchronous inputs are activated, no spike will occur. When the spikes can cause problems, a simple solution is to common the joint JK inputs with the synchronous set or reset signal.

LOGIC DIAGRAMS AND LOADING FACTORS



FUNCTIONAL LOGIC DIAGRAMS



TRUTH TABLES

SYNCHRONOUS OPERATION

BEFORE CLOCK OUTPUTS		BEFORE CLOCK INPUTS		OUTPUTS AFTER CLOCK	
ONE	ZERO	J	K	ONE	ZERO
L	H	L*	X	L	H
L	H	H*	X	H	L
H	L	X	L*	H	L
H	L	X	H*	L	H

ASYNCHRONOUS OPERATION

INPUTS		OUTPUTS	
S_D	C_D	ONE	ZERO
L	L	H	H
L	H	H	L
H	L	L	H
H	H	Synchronous Inputs Control	

SYNCHRONOUS OPERATION

The truth table defines the next state of the flip-flop after a low-to-high transition of the clock pulse. The next state is a function of the present state and the J and K inputs as shown in the table.

The J and K inputs in the table refer to the basic flip-flop J and K inputs as indicated on the logic diagrams. These internal inputs are for every flip-flop the result of a logic operation on the external J and K inputs. This operation is represented symbolically by AND gates in the logic diagram for each flip-flop. Logic diagrams are in accordance with MIL Standard 806B.

The L* symbol in the J and K input column is defined as meaning that that input does not go high at any time while the clock is low.

The H* symbol in the J or K input column is defined as meaning that the input has been high at some time while the clock was low.

The X symbol indicates that the condition of that input has no effect on the next state of the flip-flop.

The H and L symbols refer to steady state high and low voltage levels, respectively.

UNUSED INPUTS

The 9001, 9020 and 9022 all have active level low synchronous inputs. When not in use they must be grounded. All other unused inputs including asynchronous should be tied high for maximum operating speed. Use one of the methods recommended on Page 3.

ELECTRICAL CHARACTERISTICS 9000, 9001, 9020 AND 9022 ($T_A = -55°C$ to $125°C$, $V_{CC} = 5.0\ V \pm 10\%$)

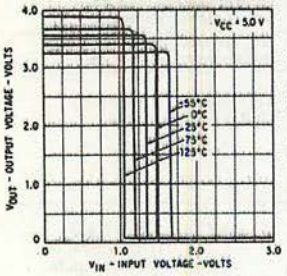
SYMBOL	CHARACTERISTIC	LIMITS −55°C MIN.	LIMITS −55°C MAX.	LIMITS 25°C MIN.	LIMITS 25°C TYP.	LIMITS 25°C MAX.	LIMITS 125°C MIN.	LIMITS 125°C MAX.	UNITS	CONDITIONS & COMMENTS	
V_{OH}	Output High Voltage	2.4		2.4	2.7		2.4		Volts	$V_{CC} = 4.5\ V$, $I_{OH} = -1.2\ mA$	
V_{OL}	Output Low Voltage		0.4		0.21	0.4		0.4	Volts	$V_{CC} = 4.5\ V$, $I_{OL} = 12.4\ mA$ $V_{CC} = 5.5\ V$, $I_{OL} = 16.0\ mA$	
V_{IH}	Input High Voltage	2.0		1.7			1.4		Volts	Guaranteed input high threshold for all inputs	
V_{IL}	Input Low Voltage		0.8			0.9		0.8	Volts	Guaranteed input low threshold for all inputs	
I_R	Input Leakage All J, K inputs T inputs 9000, 9001 JK inputs 9000, 9001 T inputs 9020, 9022 JK inputs 9020, 9022 S_D, C_D (all flip-flops)				5.0 10 20 14	60 120 240 160		60 120 240 160	μA	$V_{CC} = 5.5\ V$ $V_R = 4.5\ V$ Gnd. on other inputs.	
I_F	Input Current All J, K inputs T inputs 9000, 9001 JK inputs 9000, 9001 T inputs 9020, 9022 JK inputs 9020, 9022 S_D, C_D (all flip-flops)		−1.60 −3.20 −6.40 −4.32		−1.1 −2.2 −4.4 −2.97	−1.60 −3.20 −6.40 −4.32		−1.60 −3.20 −6.40 −4.32	mA	$V_{CC} = 5.5\ V$	$V_F = 0.4\ V$ 5.5 V Gnd on other inputs
I_F	Input Current All J, K inputs T inputs 9000, 9001 JK inputs 9000, 9001 T inputs 9020, 9022 JK inputs 9020, 9022 S_D, C_D (all flip-flops)		−1.24 −2.48 −4.96 −3.35		−0.87 −1.74 −3.48 −2.35	−1.24 −2.48 −4.96 −3.75		−1.24 −2.48 −4.96 −3.35	mA	$V_{CC} = 4.5\ V$	
I_{FD}	V_{CC} Current 9000 9001 9020, 9022 each flip-flop		24 28 27		13 14 14	24 28 27		24 28 27	mA	S_D at gnd S_D at gnd C_{D1}, C_{D2} at gnd	$V_{CC} = 5.0\ V$

ELECTRICAL CHARACTERISTICS 9000, 9001, 9020 AND 9022 ($T_A = 0°C$ to $75°C$, $V_{CC} = 5.0\ V \pm 5\%$)

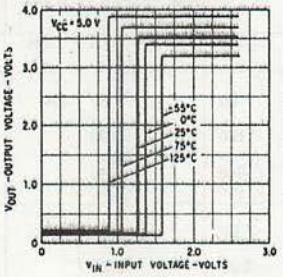
SYMBOL	CHARACTERISTIC	LIMITS 0°C MIN.	LIMITS 0°C MAX.	LIMITS 25°C MIN.	LIMITS 25°C TYP.	LIMITS 25°C MAX.	LIMITS 75°C MIN.	LIMITS 75°C MAX.	UNITS	CONDITIONS & COMMENTS	
V_{OH}	Output High Voltage	2.4		2.4	3.0		2.4		Volts	$V_{CC} = 4.75\ V$, $I_{OH} = -1.2\ mA$	
V_{OL}	Output Low Voltage		0.45		0.21	0.45		0.45	Volts	$V_{CC} = 4.75\ V$, $I_{OL} = 14.1\ mA$ $V_{CC} = 5.25\ V$, $I_{OL} = 16\ mA$	
V_{IH}	Input High Voltage	1.9		1.8			1.6		Volts	Guaranteed input high threshold for all inputs	
V_{IL}	Input Low Voltage		0.85			0.85		0.85	Volts	Guaranteed input low threshold for all inputs	
I_R	Input Leakage All J, K inputs T inputs 9000, 9001 JK inputs 9000, 9001 T inputs 9020, 9022 JK inputs 9020, 9022 S_D, C_D (all flip-flops)				5.0 10 20 14	60 120 240 160		60 120 240 160	μA	VCC = 5.25 V, $V_R = 4.5\ V$ Gnd. on other inputs.	
I_F	Input Current All J, K inputs T inputs 9000, 9001 JK inputs 9000, 9001 T inputs 9020, 9022 JK inputs 9020, 9022 S_D, C_D (all flip-flops)		−1.60 −3.20 −6.40 −4.32		−1.0 −2.0 −4.0 −2.7	−1.60 −3.20 −6.40 −4.32		−1.60 −3.20 −6.40 −4.32	mA	$V_{CC} = 5.25\ V$	$V_F = 0.45\ V$ 5.25 V on other inputs
I_F	Input Current All J, K inputs T inputs 9000, 9001 JK inputs 9000, 9001 T inputs 9020, 9022 JK inputs 9020, 9022 S_D, C_D (all flip-flops)		−1.41 −2.82 −5.64 −3.78		−0.94 −1.88 −3.76 −2.54	−1.41 −2.82 −5.64 −3.78		−1.41 −2.82 −5.64 −3.78	mA	$V_{CC} = 4.75\ V$	
I_{PD}	V_{CC} Current 9000 9001 9020, 9022 each flip-flop		28 33 30			28 33 30		28 33 30	mA	S_D at gnd S_D at gnd C_{D1}, C_{D2} at gnd	$V_{CC} = 5.0\ V$

TYPICAL INPUT AND OUTPUT CHARACTERISTICS 9000, 9001, 9020 AND 9022

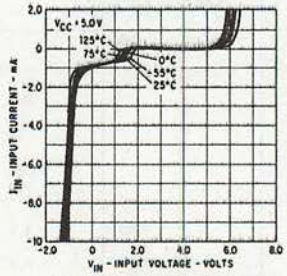
OUTPUT VOLTAGE VERSUS INPUT VOLTAGE ASYNCHRONOUS INPUTS



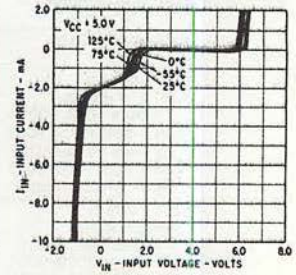
CLOCK OUTPUT VOLTAGE VERSUS INPUT VOLTAGE



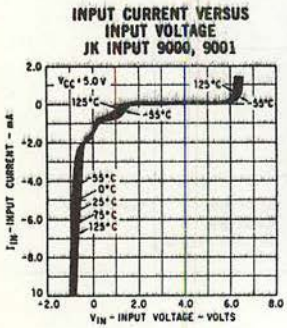
INPUT CURRENT VERSUS INPUT VOLTAGE 9004



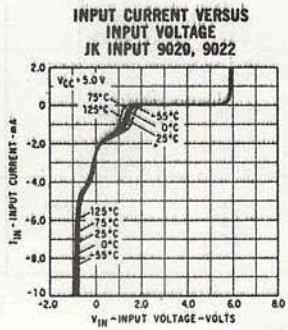
INPUT CURRENT VERSUS INPUT VOLTAGE 9009



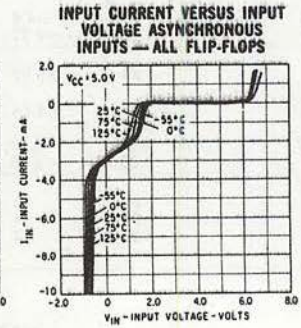
INPUT CURRENT VERSUS INPUT VOLTAGE JK INPUT 9000, 9001



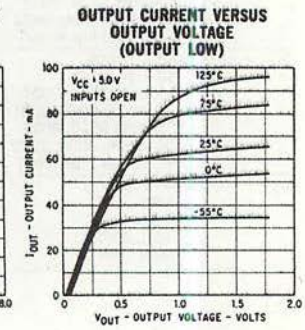
INPUT CURRENT VERSUS INPUT VOLTAGE JK INPUT 9020, 9022



INPUT CURRENT VERSUS INPUT VOLTAGE ASYNCHRONOUS INPUTS — ALL FLIP-FLOPS



OUTPUT CURRENT VERSUS OUTPUT VOLTAGE (OUTPUT LOW)

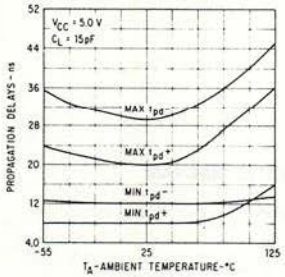


SWITCHING CHARACTERISTICS ($T_A = 25°C$, $V_{CC} = 5.0$ V, $C_L = C_I = 15$ pF of all flip-flops unless otherwise noted)

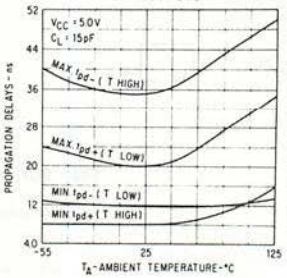
	CHARACTERISTICS		MIN.	TYP.	MAX.	UNITS	FIGURES
t_{pd+}	Clock-to-Output			12	20	ns	10, 11, 12
	S_D or C_D-to-Otuput			12	20	ns	10, 11. 12
t_{pd-}	Clock-to-Output			20	30	ns	10, 11, 12
	S_D or C_D-to-Output			25	35	ns	10, 11. 12
t_{set-up}	J, K or JK	9000 Only	30* 35	22		ns	10, 12
	Data Entry		10* 12	8.0		ns	10, 11, 12
	J or $\overline{K}$ Data Entry		17	12		ns	10, 11, 12
$t_{release}$	J, K or JK	9000 Only		18	12	ns	10, 12
	Data Entry			7.0	1.0	ns	10, 11, 12
	J or $\overline{K}$ Data Entry			11	4.0	ns	10, 11, 12
Pulse Widths	Clock 9000 Only	Positive		20		ns	10, 12
		Negative		25		ns	10, 12
		Positive		8.0		ns	10, 11, 12
		Negative		10		ns	10, 11, 12
	S_D or C_D	Negative		25		ns	10, 11, 12
Toggle Frequency		9000 Only		20		MHz	10, 12
				50		MHz	10, 11, 12

*For –1 types

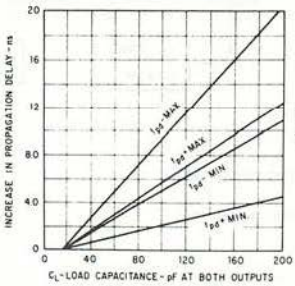
MAX. AND MIN. PROPAGATION DELAYS VERSUS AMBIENT TEMPERATURE T TO OUTPUT



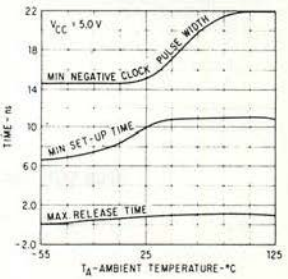
MAX. AND MIN. PROPAGATION DELAYS VERSUS AMBIENT TEMPERATURE ASYNCHRONOUS INPUTS TO OUTPUTS



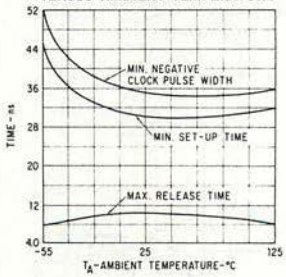
INCREASE IN ASYNCHRONOUS OR CLOCK INPUT DUE TO OUTPUT CAPACITANCE



9001-9020-9022 SET-UP/RELEASE TIME AND NEGATIVE CLOCK PULSE WIDTH VERSUS AMBIENT TEMPERATURE

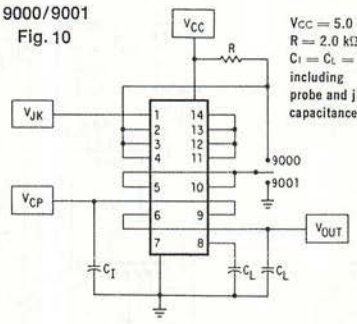


9000 NEGATIVE CLOCK PULSE WIDTH SET-UP/RELEASE TIME VERSUS AMBIENT TEMPERATURE



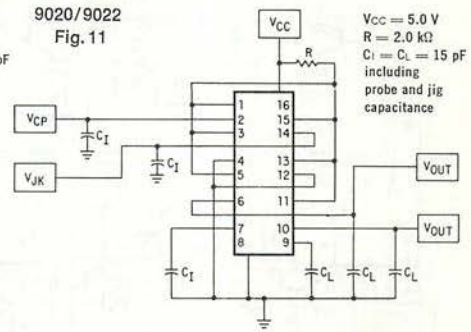
SWITCHING TEST CIRCUITS

9000/9001 Fig. 10



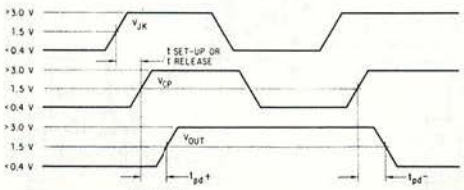
V_{CC} = 5.0 V
R = 2.0 kΩ
$C_I = C_L$ = 15 pF including probe and jig capacitance

9020/9022 Fig. 11



V_{CC} = 5.0 V
R = 2.0 kΩ
$C_I = C_L$ = 15 pF including probe and jig capacitance

WAVEFORMS Fig. 12



SWITCHING TEST NOTES

t_{pd+} and t_{pd-}

1. V_{JK} should be kept at the high logic level when performing t_{pd} tests.
2. Drive the clock pulse input with a suitable pulse source. t_{pd+} and t_{pd-} delays are as defined in the waveforms.

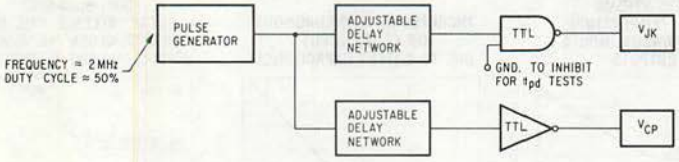
$t_{set\text{-}up}$

1. $t_{set\text{-}up}$ is defined as the minimum time required for a HIGH to be present at a synchronous logic input at any time during the low state of the clock in order for the flip-flop to respond to the data.
2. The test for $t_{set\text{-}up}$ is performed by adjusting the timing relationship between the V_{CP} and V_{JK} inputs to the $t_{set\text{-}up}$ minimum value. A device that passes the test will have the output waveform shown. The output of a device that does not pass the $t_{set\text{-}up}$ test will remain at a static logic level (no switching will occur).

$t_{release}$

1. $t_{release}$ is defined as the maximum time allowed for a HIGH to be present at a synchronous logic input at any time during the low state of the clock and not be recognized.
2. The test for $t_{release}$ is performed by adjusting the timing relationship between V_{CP} and V_{JK} to the $t_{release}$ maximum value. The outputs of devices that pass will remain at static logic levels. In order to check both J and K sides of the flip-flop it is necessary to perform the test with the flip-flop in each of its two possible states, i.e., set and clear. This can be accomplished by making use of the appropriate direct inputs to establish the state before a test. The outputs of devices that do not pass the $t_{release}$ test will exhibit pulses instead of static levels.

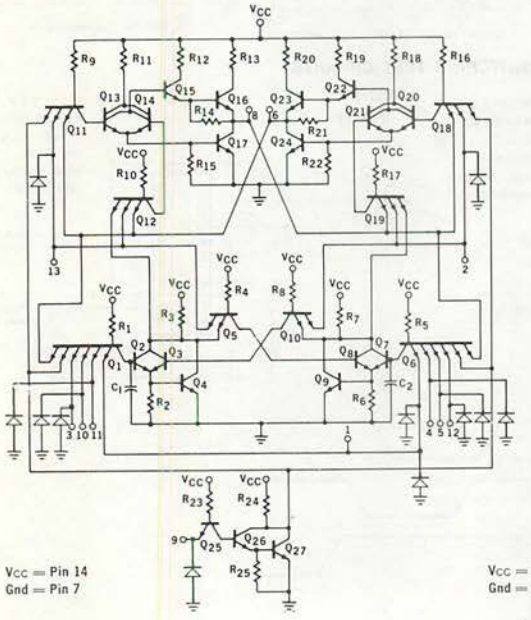
RECOMMENDED INPUT PULSE SOURCES



DTL9932 gates with adjustable capacitors connected from extender inputs to ground make suitable delay elements.

9000 SCHEMATIC DIAGRAM

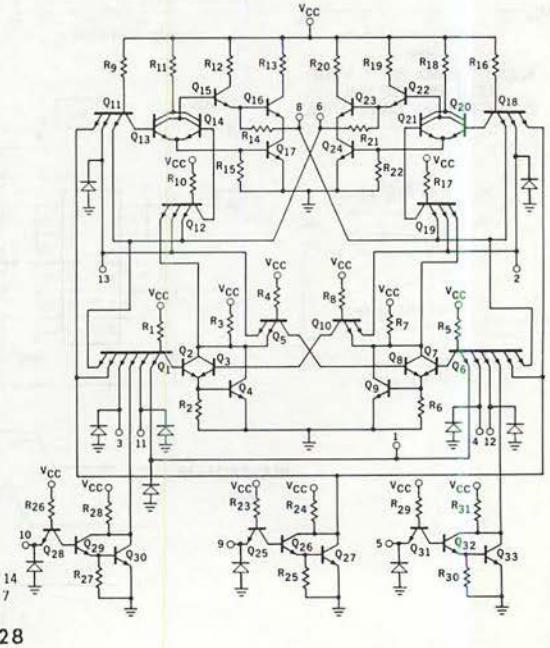
For resistor values, see page 16



V_{CC} = Pin 14
Gnd = Pin 7

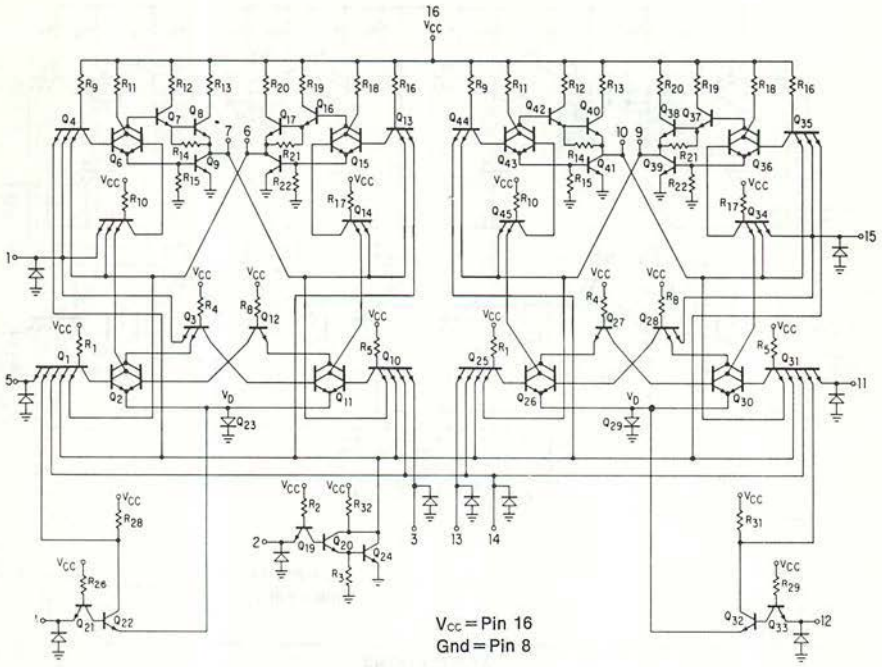
9001 SCHEMATIC DIAGRAM

For resistor values, see page 16



V_{CC} = Pin 14
Gnd = Pin 7

9020 SCHEMATIC DIAGRAM

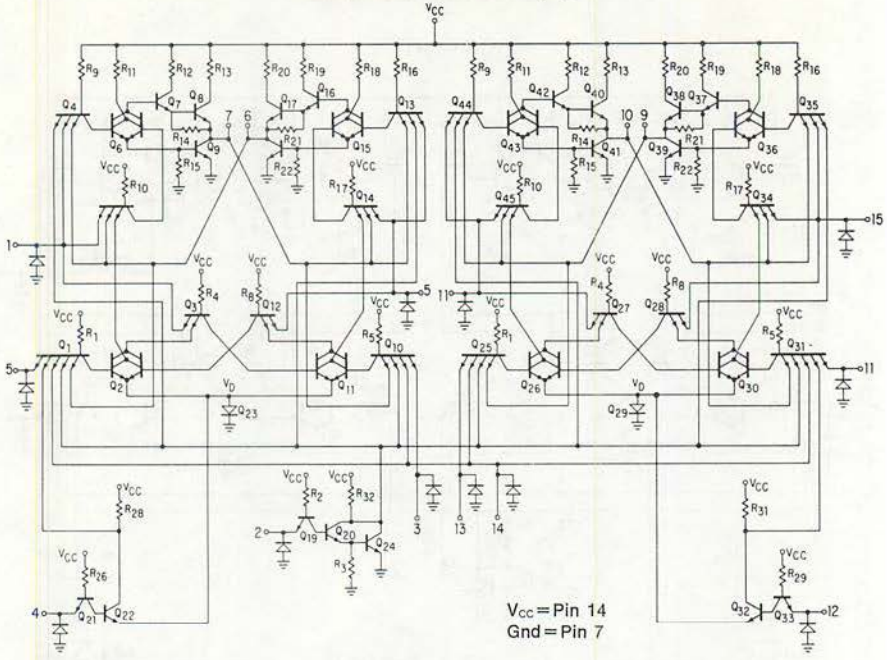


NOMINAL COMPONENT VALUES (ALL FLIP-FLOPS)

R_1, R_4, R_5, R_8, R_{10}, R_{14}, R_{17}, R_{21}, R_{22}, R_{23}, R_{24}, R_{26}, R_{29} = 4.0 kΩ
R_2, R_3, R_6, R_7 = 2.0 kΩ
R_9, R_{16}, R_{28}, R_{31} = 6.0 kΩ
R_{11}, R_{18} = 1.5 kΩ
R_{12}, R_{19} = 150 Ω
R_{13}, R_{20} = 80 Ω
R_{15}, R_{22}, R_{25}, R_{27}, R_{30} = 1.25 kΩ
R_{32} = 1.0 kΩ
C_1, C_2 = 10 pF

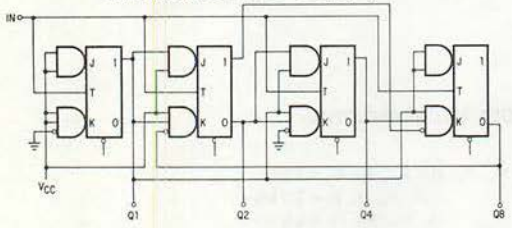
9022 SCHEMATIC DIAGRAM

For resistor values, see table on page



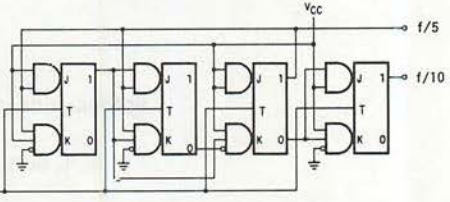
APPLICATIONS

SYNCHRONOUS BCD COUNTER



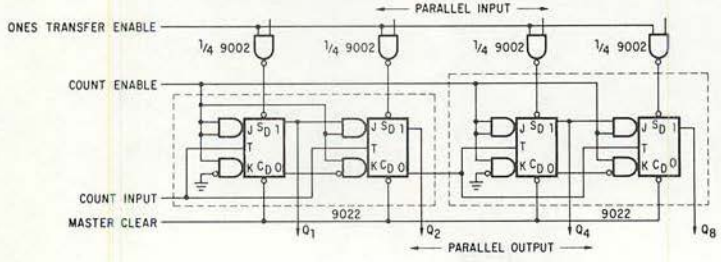
Two TTL 9020 Dual Flip-Flops require no additional gating to produce a fully synchronous 8421 code BCD Counter.

DIVIDE BY TEN COUNTER



Two TTL 9020 Dual Flip-Flops require no additional gating elements to produce divide by ten circuit with a square wave divide by ten output and a divide by five output.

BINARY COUNTER WITH ASYNCHRONOUS PARALLEL LOAD AND CLEAR



Binary counter using synchronous 2 bit stages with trickle down between stages illustrates method of utilizing dual JK flip-flops having common clocks in counter applications.

DUAL J$\overline{K}$ (OR D) FLIP-FLOP

- **Dual Rank Type Circuit**
- **Separate Clocks**
- **Separate Asynchronous Set and Clear Inputs**
- **Low Power Dissipation**
- **Compatible with ITT DTL and Other TTL Families**
- **Input Diode Clamping**
- **25 MHz Operation**

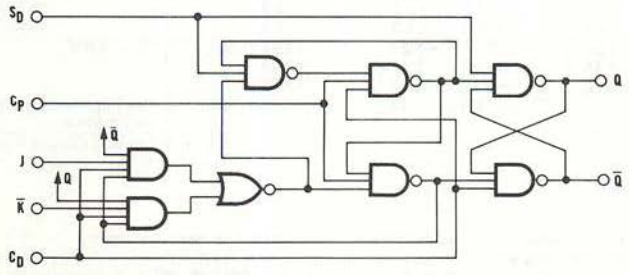
The MIC9024 consists of two high-speed, completely independent transition clocked J$\overline{K}$ flip-flops. The clocking operation is independent of rise and fall times of the clock waveform. The J$\overline{K}$ design allows operation as a D flip-flop by simply connecting the J and $\overline{K}$ pins together.

ABSOLUTE MAXIMUM RATINGS

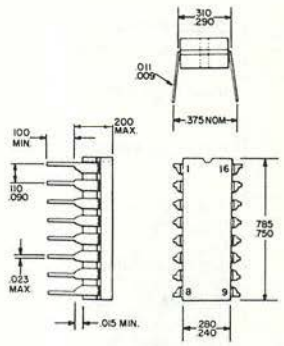
CHARACTERISTICS		UNITS
Storage Temperature	−65 to +150	°C
Temperature (Ambient) Under Bias	−55 to +125	°C
V_{CC} Pin Potential to Ground Pin (See Note 1)	−0.5 to +8	Volts
Voltage applied to output when output is high	0 V to +V_{CC}	value
Input Voltage (DC) (See Note 2)	−0.5 to +5.5	Volts
Input Current (DC) (See Note 2)	−30 to +5	mA
Current into output when output is low	+30	mA

Notes 1 and 2 following page

LOGIC DIAGRAM

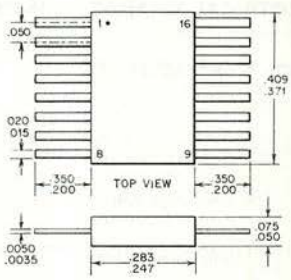


DIMENSIONS — DUAL IN-LINE

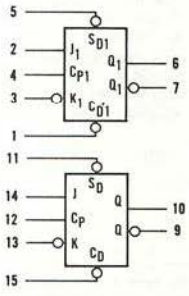


Leads are intended for insertion in hole rows on .300" centers. They are purposely shipped with "positive" (.375) misalignment to facilitate insertion.

DIMENSIONS — FLAT PACK



LOGIC SYMBOL



*ELECTRICAL CHARACTERISTICS ($T_A = 0°C$ to $75°C$, $V_{CC} = 5\ V \pm 5\%$) (Note 3)

SYMBOL	CHARACTERISTIC	LIMITS 0°C MIN.	LIMITS 0°C MAX.	LIMITS 25°C MIN.	LIMITS 25°C TYP.	LIMITS 25°C MAX.	LIMITS 75°C MIN.	LIMITS 75°C MAX.	UNITS	CONDITIONS AND COMMENTS
V_{OH}	Output High Voltage	2.4		2.4	3.0		2.4		Volts	$V_{CC} = 4.75\ V$, $I_{OH} = -1.2\ mA$
V_{OL}	Output Low Voltage		0.45		0.21	0.45		0.45	Volts	$V_{CC} = 4.75\ V$, $I_{OL} = 14.1\ mA$ $V_{CC} = 5.25\ V$, $I_{OL} = 16\ mA$
V_{IH}	Input High Voltage	1.9		1.8			1.6		Volts	Guaranteed input high threshold for all inputs. (To Sink I_{OL})
V_{IL}	Input Low Voltage		0.85			0.85		0.85	Volts	Guaranteed input low threshold for all inputs. (For V_{OH} Output)
I_R $2I_R$ $4\ I_R$	J, K Leakage Current Clock Input, S_D C_D				5.0 10 20	60 120 240		60 120 240	μA	$V_{CC} = 5.25\ V$, $V_R = 4.5\ V$ Gnd. on other inputs
I_F $2\ I_F$ $3\ I_F$	J, K Input Current Clock Input, S_D C_D (Note 4)		−1.6 −3.2 −4.8		−1.0 −2.0 −3.0	−1.6 −3.2 −4.8		−1.6 −3.2 −4.8	mA	$V_{CC} = 5.25\ V$ $V_F = 0.45\ V$ 4.5 V on other inputs
I_F $2\ I_F$ $3\ I_F$	J, K Input Current Clock Input, S_D C_D (Note 4)		−1.41 −2.82 −4.23		−0.94 −1.88 −2.82	−1.41 −2.82 −4.23		−1.41 −2.82 −4.23	mA	$V_{CC} = 4.75\ V$
I_{PD}	Current Drain				9.0	14			mA	Per Flip Flop in Worst Logic State
I_{SC}	Output Current				−65				mA	Logic 1 Output Short Circuit

*Pulse tested.

*ELECTRICAL CHARACTERISTICS ($T_A = -55°C$ to $125°C$, $V_{CC} = 5\ V \pm 10\%$) (Note 3)

SYMBOL	CHARACTERISTIC	LIMITS −55°C MIN.	LIMITS −55°C MAX.	LIMITS 25°C MIN.	LIMITS 25°C TYP.	LIMITS 25°C MAX.	LIMITS 125°C MIN.	LIMITS 125°C MAX.	UNITS	CONDITIONS AND COMMENTS
V_{OH}	Output High Voltage	2.4		2.4	2.7		2.4		Volts	$V_{CC} = 4.5\ V$, $I_{OH} = -1.2\ mA$
V_{OL}	Output Low Voltage		0.4 0.4		0.2 0.25	0.4 0.4		0.4 0.4	Volts Volts	$V_{CC} = 4.5\ V$, $I_{OL} = 12.4\ mA$ $V_{CC} = 5.5\ V$, $I_{OL} = 16\ mA$
V_{IH}	Input High Voltage	2.0		1.7			1.4		Volts	Guaranteed input high threshold for all inputs. (To Sink I_{OL})
V_{IL}	Input Low Voltage		0.8			0.9		0.8	Volts	Guaranteed input low threshold for all inputs. (For V_{OH} Output)
I_R $2I_R$ $4\ I_R$	J, K Leakage Current Clock Input, S_D C_D				5.0 10 20	60 120 240		60 120 240	μA	$V_{CC} = 5.5\ V$, $V_R = 4.5\ V$ Gnd. on other inputs
I_F $2\ I_F$ $3\ I_F$	J, K Input Current Clock Input, S_D C_D (Note 4)		−1.6 −3.2 −4.8		−1.1 −2.2 −3.3	−1.6 −3.2 −4.8		−1.6 −3.2 −4.8	mA	$V_{CC} = 5.5\ V$ $V_F = 0.4\ V$ 4.5 V on other inputs
I_F $2\ I_F$ $3\ I_F$	J, K Input Current Clock Input, S_D C_D (Note 4)		−1.24 −2.48 −3.72		−0.91 −1.82 −2.73	−1.24 −2.48 −3.72		−1.24 −2.48 −3.72	mA	$V_{CC} = 4.5\ V$
I_{PD}	Current Drain				9.0	14			mA	Per Flip Flop in Worst Logic State
I_{SC}	Output Current				−65				mA	Logic 1 Output Short Circuit

*Pulse tested.

NOTES:

(1) The maximum V_{CC} value of 8.0 volts is not the primary factor in determining the maximum V_{CC} which may be applied to a number of interconnected devices. The voltage at a high output is approximately 1 V_{BE} below the V_{CC} voltage, so the primary limit on the V_{CC} is that the voltage at any input may not go above 5.5 V unless the current is limited, so this effectively limits the system V_{CC} to approximately 7.0 volts.

(2) Because of the input clamp diodes, excess current can be drawn out of the inputs if the D.C. input voltage is more negative than −0.5 V. The diode is designed to clamp off large negative A.C. swings associated with fast fall times and long lines. This maximum rating is intended only to limit the steady state input voltage and current.

(3) Positive current is into device and negative current is out of device.

(4) Denotes maximum current under normal operation. These currents may increase up to 4 I_F if J, K = Logic 1 and S_D = Logic 0.

TRUTH TABLES

SYNCHRONOUS ENTRY J-K MODE OPERATION

INPUTS AT t_n		OUTPUTS AT t_{n+1}	
J	$\overline{K}$	Q	$\overline{Q}$
L	H	No Change	
L	L	L	H
H	H	H	L
H	L	Toggles	

SYNCHRONOUS ENTRY D MODE OPERATION

INPUTS AT t_n	OUTPUTS AT t_{n+1}	
D	Q	$\overline{Q}$
L	L	H
H	H	L

L = Low Logic Level, H = High Logic Level

ASYNCHRONOUS ENTRY INDEPENDENT OF CLOCK & SYNCHRONOUS INPUTS

INPUTS		OUTPUTS	
S_D 5(11)	C_D 1(15)	Q 6(10)	$\overline{Q}$ 7(9)
L	L	H	H
L	H	H	L
H	L	L	H
H	H	No Change	

LOADING RULES

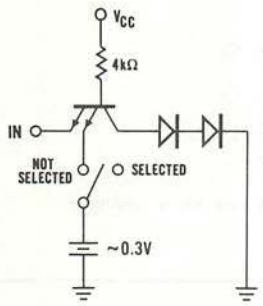
INPUT	LOADING
J and $\overline{K}$	1 U.L.
C_p and S_D	2 U.L.
C_D* (Note 4)	3 U.L.

OUTPUTS	FAN OUT	
	High State	Low State
Q	20	10
$\overline{Q}$	20	10

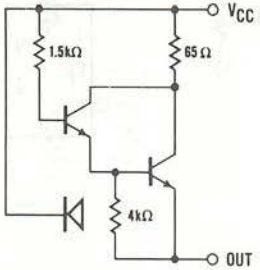
1 U.L. = 1 TTL Unit Load as defined by the entries I_R and I_F tables.

TYPICAL INPUT AND OUTPUT CHARACTERISTICS

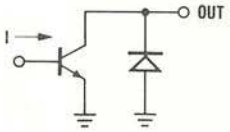
EQUIVALENT INPUT CIRCUIT



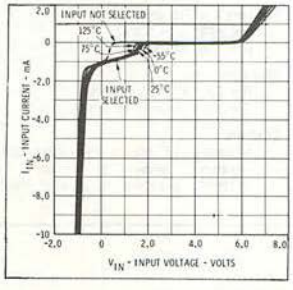
OUTPUT HIGH EQUIVALENT CIRCUIT



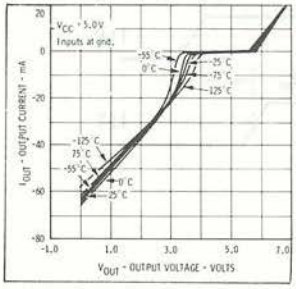
OUTPUT LOW EQUIVALENT CIRCUIT



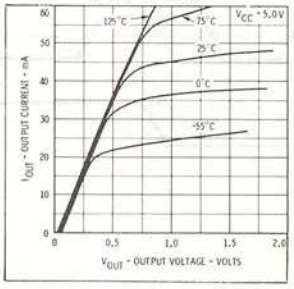
INPUT CURRENT VERSUS INPUT VOLTAGE



OUTPUT CURRENT VERSUS OUTPUT VOLTAGE (OUTPUT HIGH)



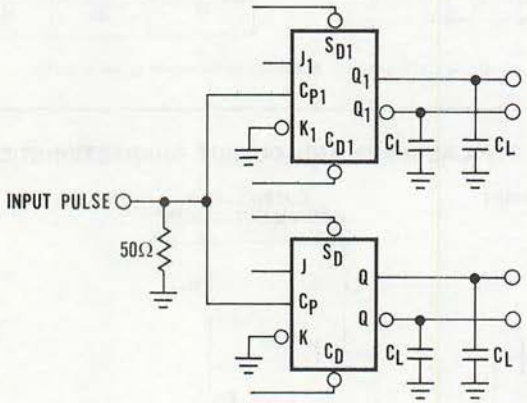
OUTPUT CURRENT VERSUS OUTPUT VOLTAGE (OUTPUT LOW)



SWITCHING CHARACTERISTICS ($T_A = 25°C$, $V_{CC} = 5.0$ V, $C_L = 15$ pF)

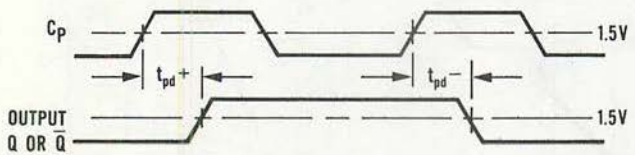
SYMBOL	CHARACTERISTIC	LIMITS 25°C MIN.	LIMITS 25°C TYP.	LIMITS 25°C MAX.	UNITS	COMMENTS
t_{pd+}	J, K, D		25		ns	Each Flip-Flop
t_{pd-}	J, K, D		20		ns	
$t_{release}$			2.0		ns	
$t_{set\text{-}up}$			15		ns	
t_{pd+}	S_D to Q		10		ns	
t_{pd-}	S_D to Q		25		ns	
	Toggle Frequency		25		MHz	

SWITCHING TEST CIRCUIT



C_L includes probe and jig capacitance

WAVEFORMS



SPECIAL ORDERING CODE

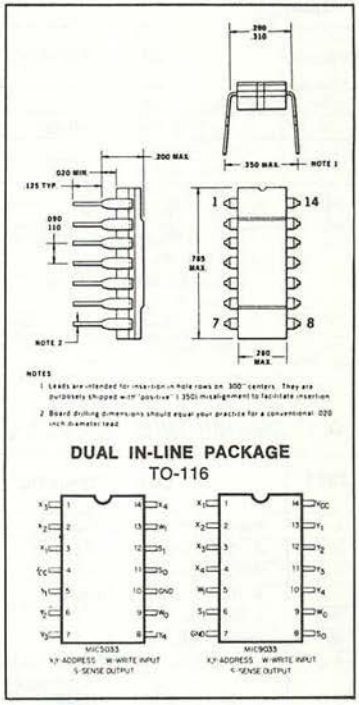
Temperature Range:
1 = −55° to +125°C
5 = 0° to +75°C

Package:
B = .250" X .250" Flat Pack
D = Dual In-Line, 16 leads

Example:
MIC9024 - 1B means operating temperature range of −55° to +125°C, supplied in a Flat Pack

16-BIT MEMORY CELL

- **High Speed**
- **Compatible with DTL and TTL Logic**
- **High Noise Immunity, Typically >1 Volt**
- **High Fanout**
- **Low Power Dissipation - 250 mw Typical**



DUAL IN-LINE PACKAGE
TO-116

The MIC 9033/5033 is a Planar epitaxial integrated 16-bit, bit-oriented, non-destructive readout memory cell, compatible with ITT MIC 930 DTL and ITT MIC 9000 TTL digital integrated circuits. This memory cell, organized as 16 word by one bit, is designed for high-speed scratch-pad memory applications.

The memory cells consist of 16 R-S flip-flops arranged in an addressable four-by-four matrix. The desired bit location is selected by raising the coincident X-Y address lines to a logic "1" (typically 3.5 volts) and holding the non-selected address lines at logic "0" (approximately ground). As many as four locations may be addressed simultaneously without destroying stored information. The data and complemented data stored at the addressed bit location may be read at the output terminals. If the addressed bit location contains a "1", the one output (S_1) will be in a low state; zero output (S_0) will be in a high state. Both W_1 and W_0 must be at logic "0" during reading.

Writing is accomplished by activating one of the write amplifiers. To write a "1", the desired bit location is addressed and the input of the "write one" (W_1) amplifier is raised to a logic "1". To write a "0", the input of the "write zero" (W_0) amplifier is raised to a logic "1".

The outputs are open-collector, which may be wire "OR" ed for word expansion. An external resistor should be returned to V_{CC} to pull-up the wire "OR"ed outputs.

ELECTRICAL CHARACTERISTICS

Ratings

SYMBOL	CHARACTERISTIC	LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNITS
V_{CC}	Supply Voltage			7.0	Volts
V_{CC}	Operating Supply Voltage	4.5	5.0	5.5	Volts
	Input Voltage			5.5	Volts
	Output Voltage			5.5	Volts
T_A	Ambient Temperature	0		+75	°C
T_S	Storage Temperature	−65		+150	°C
θ_{J-A}	Thermal Resistance, Junction-to-Ambient:				
	(1) Free Air		120		°C/Watt
	(2) 200 Ft./Min. Air Flow		65		°C/Watt
	(3) 400 Ft./Min. Air Flow		55		°C/Watt
θ_{J-C}	Thermal Resistance, Junction-to-Case		30		°C/Watt
P_D	Power Dissipation		0.25		Watts

SPECIAL ORDERING CODE

Temperature Range:
5 = 0°C to 75°C

Case Style:
Ceramic Dual-In-Line, 14 leads, add "D" following last digit.

Fanout:
40 mA Fanout part numbers:
MIC5033-5D1 or MIC9033-5D1
20 mA Fanout part numbers:
MIC5033-5D2 or MIC9033-5D2

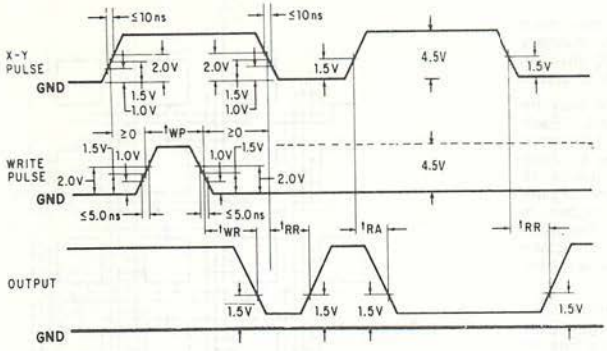
D. C. Characteristics ($V_{CC}=5.0$ V, $T_A=0°C$ to $+75°C$)

TEST	CHARACTERISTIC	LIMITS MIN.	LIMITS MAX.	UNITS	CONDITIONS
I_{FA}	Address Input Low Current		11	mA	$V_{FA}=0$ V
I_{RA}	Address Input High Current		0.4	mA	$V_{RA}=4.5$ V
I_{FW}	Write Input Low Current		1.5	mA	$V_{FW}=0$ V
I_{RW}	Write Input High Current		0.1	mA	$V_{RW}=4.5$ V
V_{IL}	Input Low Voltage		1.0	Volts	
V_{IH}	Input High Voltage	2.1		Volts	
V_{OL}	Output Low Voltage 9033/5033-XX1		0.45	Volts	$R_L=120\ \Omega$ to V_{CC}
	9033/5033-XX2		0.45	Volts	$R_L=240\ \Omega$ to V_{CC}
I_{OH}	Output Leakage Current		0.1	mA	$V_{OH}=V_{CC}$
I_{CC}	Power Drain		65	mA	$V_{CC}=5.25$ V Inputs Grounded

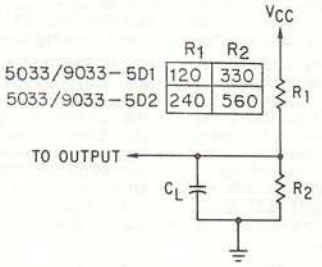
Switching Time Tests ($V_{CC}=5.0$ V, $T_A=0°C$ to $+75°C$)

TEST	CHARACTERISTIC	LIMITS C_L(pF)	LIMITS MIN.	LIMITS MAX.	UNITS	CONDITIONS
t_{WP}	Write Pulse Width		25		ns	One X-Y location high, all others low, W_O low when checking W_I, W_I low when checking W_O.
t_{WR}	Write Recovery Time	30		35	ns	One X-Y location high, all others low, "1" previously stored when testing S_O, "0" previously stored when checking S_I.
t_{RR}	Read Recovery Time	30		20	ns	One X-Y location switched, all others low, "1" previously stored when testing S_I, "0" previously stored when testing S_O.
t_{RA}	Read Access Time	200		30	ns	
t_{RA}	Read Access Time	30		22	ns	Four X-Y locations switched, all others low, "1"s previously stored when testing S_I, "0"s previously stored when testing S_O.

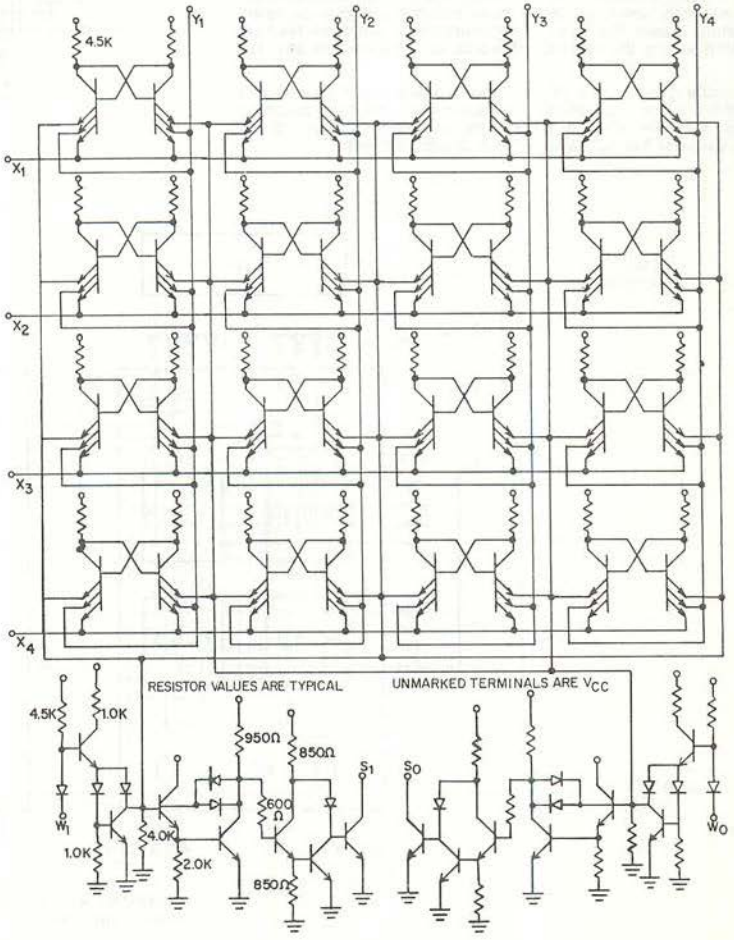
SWITCHING TEST WAVEFORMS



SWITCHING TEST OUTPUT LOAD



CIRCUIT DIAGRAM



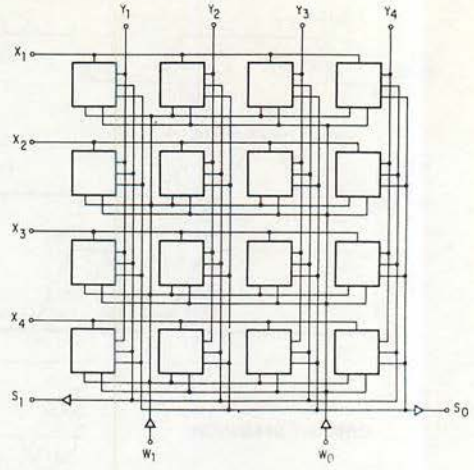
APPLICATIONS

A memory utilizing MIC5033/9033 16-bit memory cells may have any desired word length and the number of words in the memory is a multiple of 16. To illustrate how the MIC5033/9033 may be used to construct a larger memory, the following example is given:

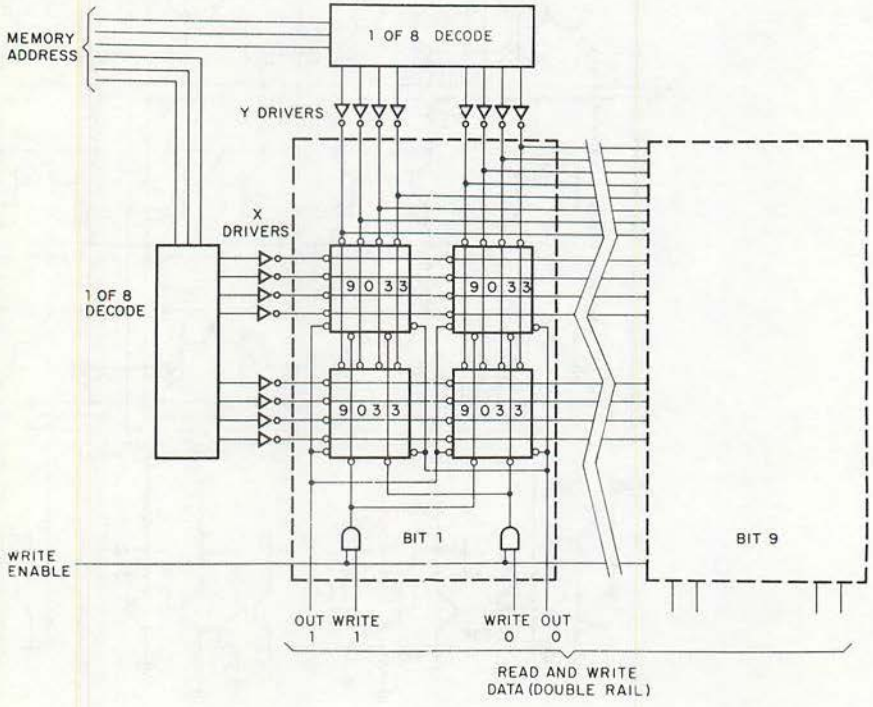
The six memory address lines from an external source may be decoded at the first level with two 1-out-of-8 decoders. Each output of the 1-out-of-8 decoders controls a driving transistor. These driving transistors provide the current necessary to drive eight X and eight Y address lines. Each transistor drives 18 MIC5033/9033 memory cells. The figure below shows the organization of such a memory. The four MIC5033/9033's shown in detail represent 64 words of one bit each. There are nine such groups of four MIC5033/9033's each, each group representing one of the nine bit positions. The 16 address driving transistors drive all nine groups.

The 1-out-of-8 decoder produces one of the eight combinations of three inputs only if the Enable input is at a high logic level. If the Enable input is at a high logic level, one, and only one, of the eight outputs assumes a low logic level. If the Enable input is at a low logic level, all the outputs assume a high logic level. This feature allows the several decoders to be used for memory addressing where the number of words is increased to say 128 or 256.

The example given above is only one of many organizations and is presented as an illustration. Obviously many address decoding schemes may be utilized depending on memory size, driver fan-out, decoder fan-out, wiring, heat dissipation, etc.



LOGIC DIAGRAM

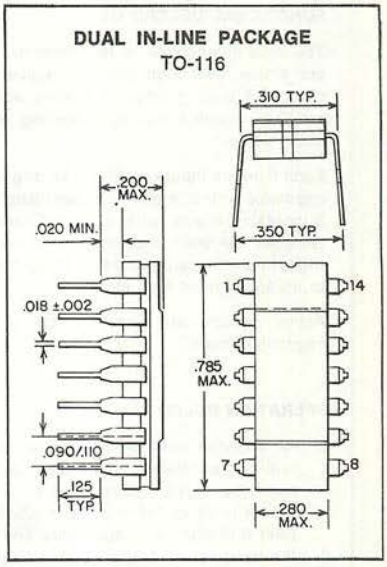


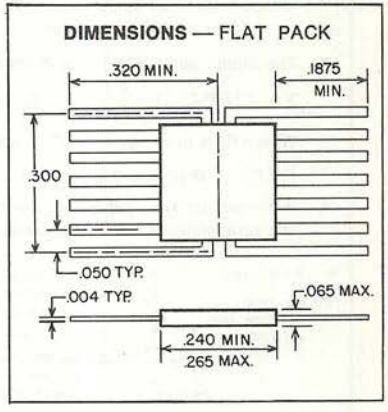
RETRIGGERABLE MONOSTABLE MULTIVIBRATOR TTL

- **Complementary Outputs and Complementary DC level sensitive inputs — insensitive to input pulse transition time.**
- **"Leading edge" or "trailing edge" triggering.**
- **High speed operation — maximum input repetition rate greater than 10 MHz.**
- **High noise immunity — 400 mV worst case.**
- **High fanout — up to 8 TTL loads.**
- **Accurate timing — determined by external R and C — 50 nsec. to ∞ output pulse width range.**
- **Choice of operating mode — inputs can normally allow retriggering, but can also be locked out.**
- **Input diode clamps prevent ringing.**
- **Logic levels are compatible with ITT DTL 930, ITT TTL 9000, MSI and other DTL and TTL families.**
- **Pulse width compensated for V_{CC} and temperature variations.**

The retriggerable monostable multivibrator or one-shot provides an output pulse with high accuracy and a very wide duration range (50 nsec to ∞). It has four DC level-sensitive inputs, two are active-level High and two are active-level Low. Designed for high speed operation, the MIC9601 will respond to trigger inputs even when already in its active timing state, and will time itself out from the last input pulse received.

The unique design of the MIC9601 makes it very useful in applications such as in square-wave and variable delay pulse generators, long delay timers, pulse absence detectors, digital low-pass filters, and even FM demodulators.





ABSOLUTE MAXIMUM RATINGS

CHARACTERISTICS		UNITS
Storage Temperature	−65 to +150	°C
Temperature (Ambient) Under Bias	−55 to +125	°C
V_{CC} Pin Potential to Ground (See Note 1)	−0.5 to +8.0	Volts
Input Voltage (D.C.) (See Note 2)	−0.5 to +5.5	Volts
Input Current (See Note 2)	−30 to +5.0	mA
Voltage Applied to Output When Output is High	0 V to +V_{CC}	value
Current Into Output When Output is Low	50	mA

NOTES:

(1) The maximum V_{CC} value of 8.0 volts is not the primary factor in determining the maximum V_{CC} which may be applied to a number of interconnected devices. The voltage at a high output is approximately 1 V_{BE} below the V_{CC} voltage, so the primary limit on the V_{CC} is that the voltage at any input may not go above 5.5 V unless the current is limited, so this effectively limits the system V_{CC} to approximately 7.0 volts.

(2) Because of the input clamp diodes, excess current can be drawn out of the inputs if the D.C. input voltage is more negative than −0.5 V. The diode is designed to clamp off large negative A.C. swings associated with fast fall times and long lines. This maximum rating is intended only to limit the steady state input voltage and current.

FUNCTIONAL DESCRIPTION

The 9601 monostable multivibrator has four inputs, two of which are active level high and two active level low. This allows a choice of leading edge or trailing edge triggering. The inputs are D.C. coupled making triggering independent of input transition times.

Each time the input conditions for triggering are met, the external capacitor is discharged in a short time and a new cycle is begun. Successive inputs with a period shorter than the delay time retrigger the 9601 and result in a continuous true output. Retriggering may be inhibited by tying the negation (Q) output back to an active level high input.

Active pullups are provided for good drive capability into capacitive loads.

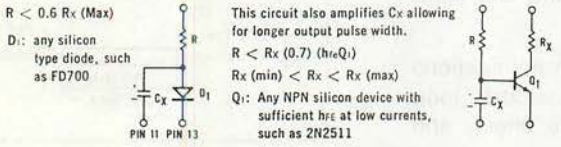
OPERATION RULES

1. An external resistor R_x and an external capacitor C_x are required as shown in the logic diagram. The values of R_x may vary from 5.0 kΩ to 50 kΩ for 0 to +75°C operation, and 5.0 kΩ to 25 kΩ for −55 to +125°C operation. C_x may vary from 0 to any value necessary and obtainable.
2. If a fixed value of R_x is used, the following values are recommended: R_x = 30 kΩ for 0 to +75°C operation; R_x = 10 kΩ for −55 to +125°C operation.
3. The output pulse width T is defined as follows:

   $T = 0.32\ R_xC_x\ [1 + \frac{0.7}{R_x}]$ (For C_x greater than 10^3 pF)

   Where R_x is in kΩ, C_x is in pF, T is in ns

   For $C_x < 10^3$ pF, see Fig. 14
4. If electrolytic type capacitors are to be used, the following two arrangements are recommended:

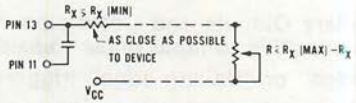


Both circuits prevent reverse voltage across C_x. The pulse width T for the circuits is defined as follows:

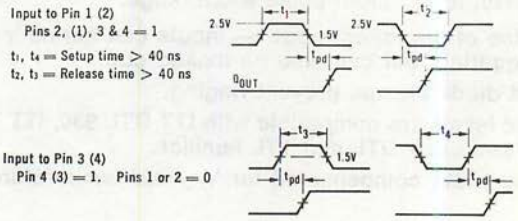
$T \approx 0.36\ RC_x\ [1 + \frac{0.7}{R}]$

Where R is in kΩ, C_x is in pF, T is in ns

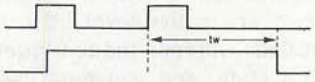
5. To obtain variable pulse width, by remote trimming, the following circuit is recommended:



6. Under any operating condition, C_x and R_x (min) must be kept as close to the circuit as possible to minimize stray capacitance and reduce noise pickup.
7. Input Trigger Pulse Rules.



8. The retrigger pulse width is calculated as shown below:

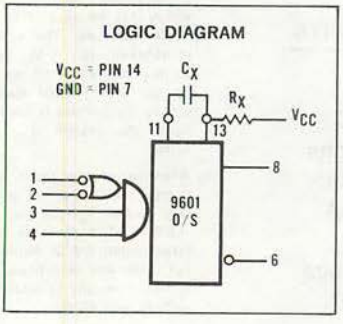


$tw = tpw + tpd+ = 0.32\ RxCx\ (1 + \frac{0.7}{Rx}) + tpd+$

The retrigger pulse width is equal to the pulse width tpw plus a delay time. For pulse widths greater than 500 ns, tw can be approximated as tpw.

NOTE: Retriggering will not occur if the retrigger pulse comes within .32 R_xC_x $(\frac{.7}{R_x})$ ns after the initial trigger pulse.

LOGIC DIAGRAM



SPECIAL ORDERING CODE

Temperature Range:
1 = −55° +125°C
5 = 0° to +75C

Package:
B = .250" X .250" Flat Pack
D = Dual In-Line ,14 leads

Example:
MIC9601- 1B means operating temperature range of −55° to +125°C, supplied in a Flat Pack

ELECTRICAL CHARACTERISTICS ($T_A = -55°C$ to $125°C$, $V_{CC} = 5\ V \pm 10\%$)

SYMBOL	CHARACTERISTIC	LIMITS						UNITS	CONDITIONS (Note 1)
		−55°C		+25°C			+125°C		
		MIN.	MAX.	MIN.	TYP.	MAX.	MIN. MAX.		
V_{OH}	Output High Voltage	2.4		2.4	3.3		2.4	Volts	$V_{CC} = 4.5\ V$, $I_{OH} = -0.72$ mA (Note 2)
V_{OL}	Output Low Voltage		0.4		0.2	0.4	0.4	Volts	$V_{CC} = 4.5\ V$, $I_{OL} = 10$ mA (Note 2)
V_{IH}	Input High Voltage	2.0		1.7			1.4	Volts	$V_{CC} = 4.5\ V$ (Note 3)
V_{IL}	Input Low Voltage		0.85			0.90	0.85	Volts	$V_{CC} = 5.5\ V$ (Note 3)
I_F	Input Load Current		−1.6		−1.1	−1.6	−1.6	mA	$V_{CC} = 5.5\ V$, $V_F = 0.4\ V$
I_R	Input Leakage Current				15	60	60	μA	$V_{CC} = 5.5\ V$, $V_R = 4.5\ V$
I_{SC}	Short Circuit Current			−10		−40		mA	$V_{CC} = 5.0\ V$, $V_{OUT} = 0\ V$ (Note 2)
I_{pd}	Quiescent Power Supply Drain		25			25	25	mA	$V_{CC} = 5.5\ V$
t_{pd+}	Negative Trigger Input to True Output				25	40		ns	$V_{CC} = 5.0\ V$, $R_X = 5.0\ k\Omega$, $C_X = 0$, $C_L = 15$ pF
t_{pd-}	Negative Trigger Input to Complement Output				25	40		ns	$V_{CC} = 5.0\ V$, $R_X = 5.0\ k\Omega$, $C_X = 0$, $C_L = 15$ pF
$t_{pw(min)}$	Minimum True Output Pulse Width				45	65		ns	$V_{CC} = 5.0\ V$, $R_X = 5.0\ k\Omega$, $C_X = 0$, $C_L = 15$ pF
Δt_{pw}	Pulse Width Variation			3.08	3.42	3.76		μsec	$V_{CC} = 5.0\ V$, $R_X = 10\ k\Omega$, $C_X = 1000$ pF
C_{STRAY}	Maximum Allowable Wiring Cap. (Pin 13)		50			50	50	pF	Pin 13 to Ground
R_X	Timing Resistor	5.0	25	5.0		25	5.0 25	kΩ	

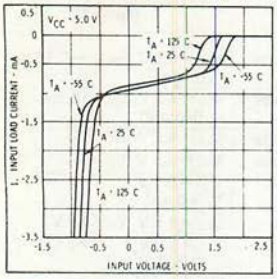
TABLE II — ELECTRICAL CHARACTERISTICS ($T_A = 0°C$ to $75°C$, $V_{CC} = 5\ V \pm 5\%$)

SYMBOL	CHARACTERISTIC	LIMITS						UNITS	CONDITIONS (Note 1)
		0°C		+25°C			+75°C		
		MIN.	MAX.	MIN.	TYP.	MAX.	MIN. MAX.		
V_{OH}	Output High Voltage	2.4		2.4	3.4		2.4	Volts	$V_{CC} = 4.75\ V$, $I_{OH} = -0.96$ mA (Note 2)
V_{OL}	Output Low Voltage		0.45		0.2	0.45	0.45	Volts	$V_{CC} = 4.75\ V$, $I_{OL} = 12.8$ mA (Note 2)
V_{IH}	Input High Voltage	1.9		1.8			1.6	Volts	$V_{CC} = 4.75\ V$ (Note 3)
V_{IL}	Input Low Voltage		.85			0.85	0.85	Volts	$V_{CC} = 5.25\ V$ (Note 3)
I_F	Input Load Current		−1.6		−1.0	−1.6	−1.6	mA	$V_{CC} = 5.25\ V$, $V_F = 0.45\ V$
I_R	Input Leakage Current				15	60	60	μA	$V_{CC} = 5.25\ V$, $V_R = 4.5\ V$
I_{SC}	Short Circuit Current			−10		−40		mA	$V_{CC} = 5.0\ V$, $V_{OUT} = 0\ V$ (Note 2)
I_{pd}	Quiescent Power Supply Drain		25			25	25	mA	$V_{CC} = 5.25\ V$ Ground Pins 1 and 2
t_{pd+}	Negative Trigger Input to True Output				25	40		ns	$V_{CC} = 5.0\ V$, $R_X = 5.0\ k\Omega$, $C_X = 0$, $C_L = 15$ pF
t_{pd-}	Negative Trigger Input to Complement Output				25	40		ns	$V_{CC} = 5.0\ V$, $R_X = 5.0\ k\Omega$, $C_X = 0$, $C_L = 15$ pF
$t_{pw(min)}$	Minimum True Output Pulse Width				45	65		ns	$V_{CC} = 5.0\ V$, $R_X = 5.0\ k\Omega$, $C_X = 0$, $C_L = 15$ pF
Δt_{pw}	Pulse Width Variation			3.08	3.42	3.76		μsec	$V_{CC} = 5.0\ V$, $R_X = 10\ k\Omega$, $C_X = 1000$ pF
C_{STRAY}	Maximum Allowable Wiring Cap. (Pin 13)		50			50	50	pF	Pin 13 to Ground
R_X	Timing Resistor	5.0	50	5.0		50	5.0 50	kΩ	

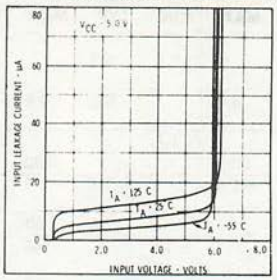
NOTES: (1) Unless otherwise noted, 10 kΩ resistor placed between Pin 13 and V_{CC}, for all tests. (R_X)
(2) Ground Pin 11 for V_{OL} Pin 6 or V_{OH} Pin 8 or I_{SC} Pin 8. Open Pin 11 for V_{OL} Pin 8 or V_{OH} Pin 6 or I_{SC} Pin 6.
(3) Pulse Test to determine V_{IH} and V_{IL} (Min PW 40 ns).

TYPICAL ELECTRICAL CHARACTERISTICS

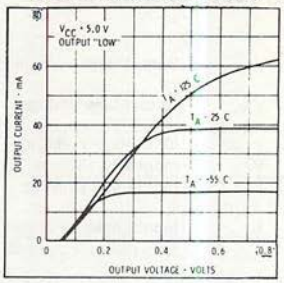
INPUT LOAD CURRENT VERSUS INPUT VOLTAGE



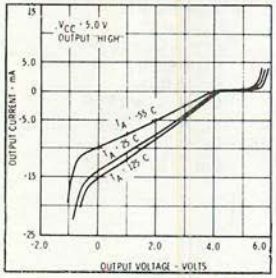
INPUT LEAKAGE CURRENT VERSUS INPUT VOLTAGE



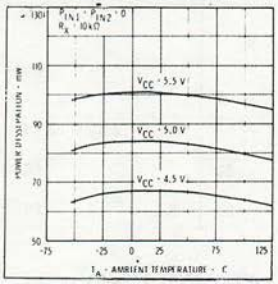
OUTPUT CURRENT VERSUS OUTPUT VOLTAGE (LOW STATE)



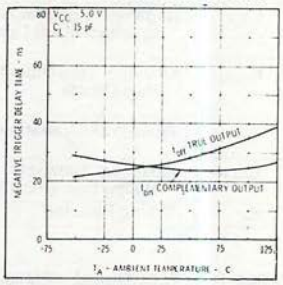
OUTPUT CURRENT VERSUS OUTPUT VOLTAGE (HIGH STATE)



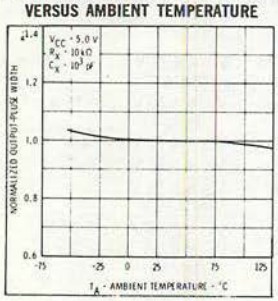
POWER DISSIPATION VERSUS AMBIENT TEMPERATURE



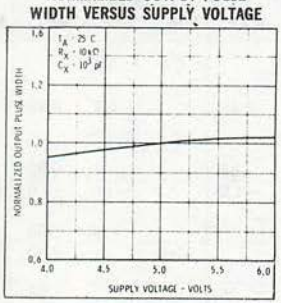
NEGATIVE TRIGGER DELAY TIME VERSUS AMBIENT TEMPERATURE



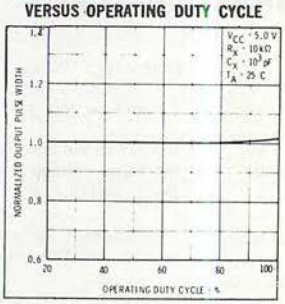
NORMALIZED OUTPUT PULSE WIDTH VERSUS AMBIENT TEMPERATURE



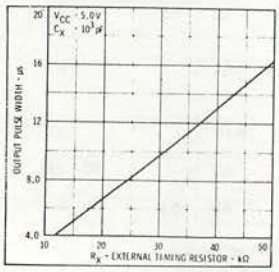
NORMALIZED OUTPUT PULSE WIDTH VERSUS SUPPLY VOLTAGE



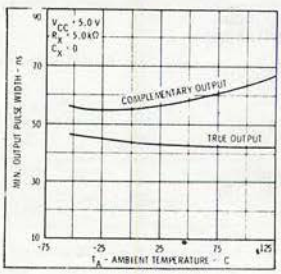
NORMALIZED OUTPUT PULSE WIDTH VERSUS OPERATING DUTY CYCLE



PULSE WIDTH VERSUS TIMING RESISTANCE

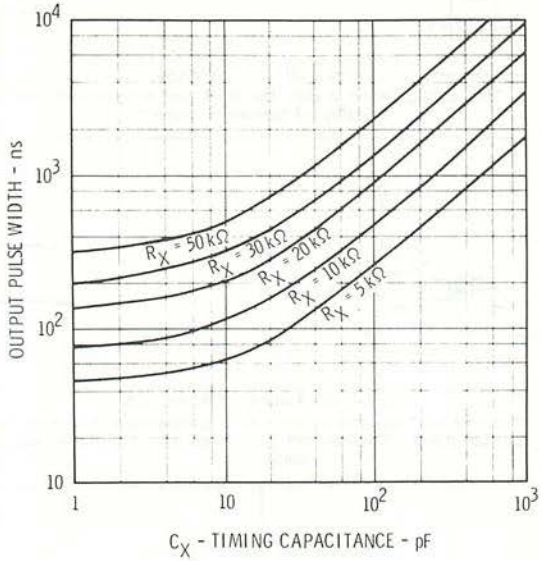


OUTPUT PULSE WIDTH VERSUS AMBIENT TEMPERATURE

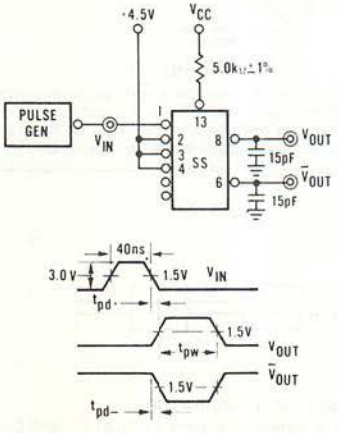


OUTPUT PULSE WIDTH VERSUS TIMING RESISTANCE AND CAPACITANCE

For $C_X < 10^3$ pF (For $C_X \geq 10^3$pF, $t_{pw} = 0.32\ R_X C_X\ (1 + \frac{0.7}{R_X})$



SWITCHING TIME TEST CIRCUIT AND WAVEFORMS



NOTE: Capacitance includes Jig and Probe

LOADING RULES

TTμL INPUT LOAD AND DRIVE FACTORS

−55°C to +125°C

INPUT LEVEL	LOAD FACTOR
High	1
Low	1
OUTPUT STATE	DRIVE FACTOR
High	12
Low	6

0°C to 75°C

INPUT LEVEL	LOAD FACTOR
High	1
Low	1
OUTPUT STATE	DRIVE FACTOR
High	16
Low	8

CCSL INPUT LOAD AND DRIVE FACTORS

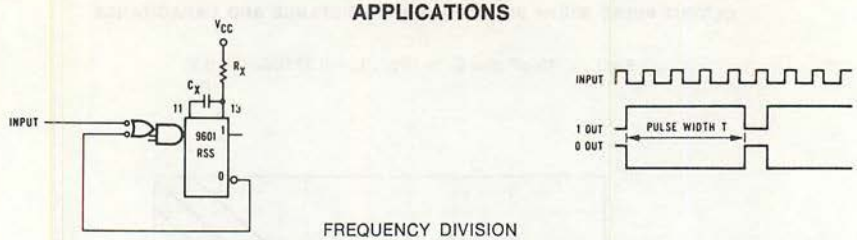
−55°C to +125°C

INPUT LEVEL	LOAD FACTOR
High	12
Low	10
OUTPUT STATE	DRIVE FACTOR
High	144
Low	62

0°C to 75°C

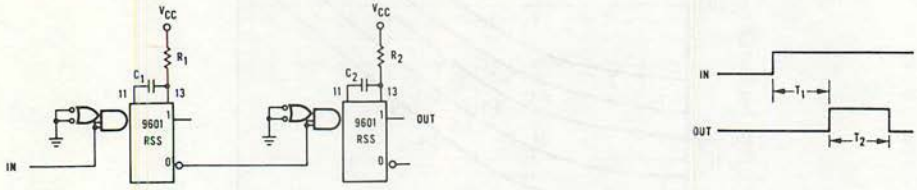
INPUT LEVEL	LOAD FACTOR
High	12
Low	10.5
OUTPUT STATE	DRIVE FACTOR
High	192
Low	85

APPLICATIONS



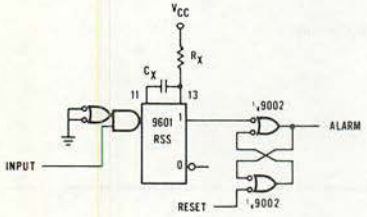
FREQUENCY DIVISION

This configuration makes the 9601 non-retriggerable and capable of frequency division.



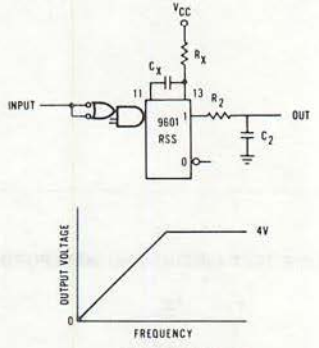
DELAYED PULSE GENERATION

The first 9601 determines the time T_1 before the initiation of the output pulse. The second 9601 determines T_2, the output pulse width.



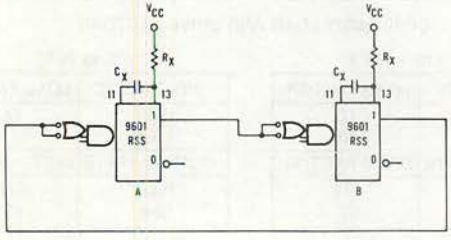
MALFUNCTION INDICATOR

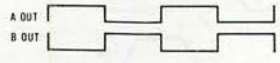
The output of the retriggerable single shot will only remain high if the input frequency is above some fixed value. The input, may be a flip flop which normally has a fixed frequency of operation. A system malfunction is indicated when the flip flop frequency drops and retriggering operation of single shot ceases.



DISCRIMINATOR

The 9601 can be used to produce a voltage output proportional to input frequency. For a fixed TC of R_x and C_x, the duty cycle of the output will vary with frequency. This is integrated by R_2 C_2 producing a voltage proportional to frequency.





ASTABLE MULTIVIBRATOR

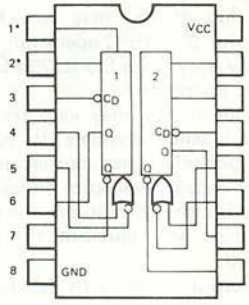
Frequency of operation is dependent upon value of R_x and C_x.

DUAL RETRIGGERABLE RESETTABLE MONOSTABLE MULTIVIBRATOR

The TTL/Monostable 9602 is a dual retriggerable, resettable monostable multivibrator which provides an output pulse whose duration and accuracy is a function of external timing components. The ITT9602 has excellent immunity to noise on the V_{CC} and ground lines. The ITT9602 uses TTL inputs and outputs for high speed and high fanout capability and is compatible with all members of the TTL family.

- **72 ns to ∞ Output Width Range**
- **Retriggerable 0 to 100% Duty Cycle**
- **TTL Input Gating - Leading or Trailing Edge Triggering**
- **Complementary TTL Outputs**
- **Optional Retrigger Lock-Out Capability**
- **Pulse Width Compensated for V_{CC} and Temperature Variations**
- **Resettable**

CONNECTION DIAGRAM
(TOP VIEW)



*Pins for external timing

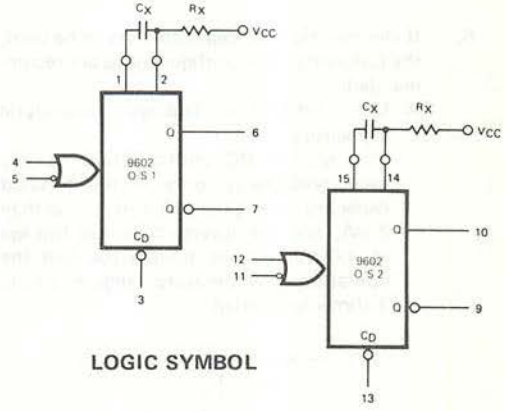
ABSOLUTE MAXIMUM RATINGS

(above which the useful life may be impaired)

Storage Temperature −65°C to +150°C
Temperature (Ambient) Under Bias −55°C to +125°C
V_{CC} Pin Potential to Ground (See Note 1) −0.5 V to +8.0 V
Input Voltage (D.C.) (See Note 2) −0.5 V to +5.5 V
Input Current (See Note 2) −30 mA to +5.0 mA
Voltage Applied to Output When Output is High −0.5 V to +V_{CC} value
Current Into Output When Output is Low 50 mA

NOTES:

1. The maximum V_{CC} value of 8.0 volts is not the primary factor in determining the maximum V_{CC} which may be applied to a number of interconnected devices. The voltage at a high output is approximately 1 V_{BE} below the V_{CC} voltage, so the primary limit on the V_{CC} is that the voltage at any input may not go above 5.5 V unless the current is limited. This effectively limits the system V_{CC} to approximately 7.0 volts.
2. Because of the input clamp diodes, excess current can be drawn out of the inputs if the D.C. input voltage is more negative than −0.5 V. The diode is designed to clamp off large negative A.C. swings associated with fast fall times and long lines. This maximum rating is intended only to limit the steady state input voltage and current.



LOGIC SYMBOL

FUNCTIONAL DESCRIPTION

The 9602 dual resettable, retriggerable monostable multivibrator has two inputs per function, one active high and one active low. This allows leading edge or trailing edge triggering. The TTL inputs make triggering independent of input transition times. When input conditions for triggering are met, a new cycle starts and the external capacitor is rapidly discharged and then allowed to charge. An input cycle time shorter than the output cycle time will retrigger the 9602 and result in a continuous true output. (See Rule 9.) The output pulse may be terminated at any time by correcting the reset pin to a low logic level pin. Active pullups are provided on the outputs for good drive capability into the capacitive loads.

OPERATION RULES

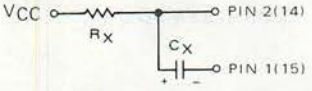
1. An external resistor (R_X) and external capacitor (C_X) are required as shown in the Logic Diagram.
2. The value of R_X may vary from 5.0 to 50 kΩ for 0 to 75°C operation. The value of R_X may vary from 5.0 to 25 kΩ for −55 to +125°C operation.
3. The value of C_X may vary from 0 to any necessary value available. If, however, the capacitor has leakages approaching 3.0 μA or if stray capacitance from either terminal to ground is more than 50 pF, the timing equations may not represent the pulse width obtained.
4. The output pulse with (t) is defined as follows:

$$t = 0.31\ R_X C_X \left[1 + \frac{1}{R_X}\right]$$

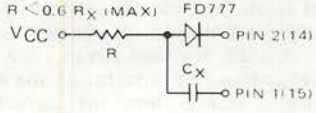
Where R_X is in kΩ
C_X is in pF
t is in ns
for $C_X < 10^3$ pF, see Fig. 17.

5. If electrolytic type capacitors are to be used, the following three configurations are recommended:

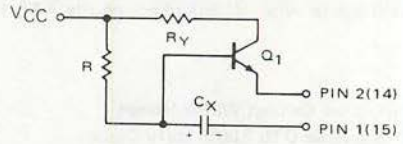
A. Use with low leakage electrolytic capacitors.
The normal RC configuration can be used predictably only if the forward capacitor leakage at 5.0 volts is less than 3 μA, and the inverse capacitor leakage at 1.0 volt is less than 5 μA over the operational temperature range and Rule 3 above is satisfied.



B. Use with high inverse leakage current electrolytic capacitors.
The diode in this configuration prevents high inverse leakage currents through the capacitor by preventing an inverse voltage across the capacitor. The use of this configuration is not recommended with retriggerable operation.



C. Use to obtain extended pulse widths:
$t \approx 0.3\ RC_X$
This configuration can be used to obtain extended pulse widths, because of the larger timing resistor allowed by beta multiplication. Electrolytics with high inverse leakage currents can be used.

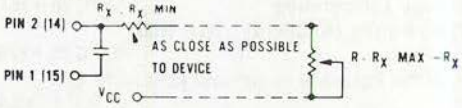


$R < R_X$ (0.7) (h_{FE} Q_1) or <2.5 MΩ whichever is the lesser
R_X (min) < R_Y < R_X (max)

Q_1: NPN silicon transistor with h_{FE} requirements of above equations, such as 2N5961 or 2N5962

$t \approx 0.3\ RC_X$
This configuration is not recommended with retriggerable operation.

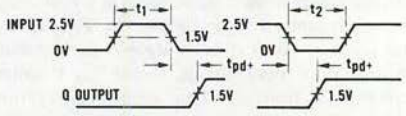
6. To obtain variable pulse width by remote trimming, the following circuit is recommended:



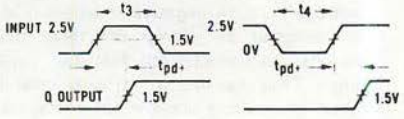
7. Under any operating condition, C_X and R_X (min) must be kept as close to the circuit as possible to minimize stray capacitance and reduce noise pickup.
8. Input Trigger Pulse Rules. See Triggering Truth Table, page 5.

Input to Pin 5 (11)
Pin 4 (12) = Low
Pin 3 (13) = High

t_1, t_3 = Min. Positive Input Pulse Width >40 ns
t_2, t_4 = Min. Negative Input Pulse Width >40 ns

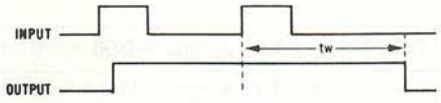


Input to Pin 4 (12)
Pin 5 (11) = High, Pin 3 (13) = High



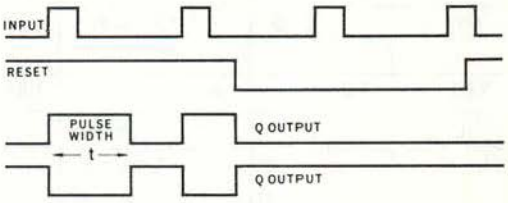
9. The retriggerable pulse width is calculated as shown below:

$$tw = tpw + t_{pd+} = 0.31\ R_X C_X\ (1 + \frac{1}{R_X}) + t_{pd+}.$$



The retrigger pulse width is equal to the pulse width tpw plus a delay time. For pulse widths greater than 500 ns, tw can be approximated as tpw. Retriggering will not occur if the retrigger pulse comes within $\approx 0.3\ C_X$ ns after the initial trigger pulse. (i.e. during the discharge cycle).

10. Reset Operation – An overriding active low level reset is provided on each oneshot. By applying a low to the reset, any timing cycle can be terminated or any new cycle inhibited until the low reset input is removed. Trigger inputs will not produce spikes in the output when the reset is held low.



11. V_{CC} and Ground wiring should conform to good high frequency standards so that switching transients on V_{CC} and Ground leads do not cause interaction between one-shots.

ELECTRICAL CHARACTERISTICS (T_A = –55°C to 125°C, V_{CC} = 5 V ± 10%)

Symbol	–55°C Min.	–55°C Max.	+25°C Min.	+25°C Typ.	+25°C Max.	+125°C Min.	+125°C Max	Units	Conditions (Note 1)
V_{OH}	2.4		2.4	3.3		2.4		Volts	V_{CC} = 4.5 V, I_{OH} = –0.96 mA (Note 2)
V_{OL}		0.4		0.2	0.4		0.4	Volts	V_{CC} = 4.5 V, I_{OL} = 9.62 mA (Note 2) V_{CC} = 5.5 V, I_{OL} = 12.8 mA
V_{IH}	2.0		1.7			1.5		Volts	Guaranteed input high
V_{IL}		0.85			0.90		0.85	Volts	Guaranteed input low
I_{IL}		–1.6		–1.1	–1.6		–1.6	mA	V_{CC} = 5.5 V, V_{IN} = 0.4 V
		–1.24		–0.97	–1.24		–1.24	mA	V_{CC} = 4.5 V, V_{IN} = 0.4 V
I_{IH}				10	60		60	μA	V_{CC} = 5.5 V, V_{IN} = 4.5 V
I_{SC}					–25			mA	V_{CC} = 5.5 V, V_{OUT} = 1.0 V (Note 2)
I_{PD}		45		39	45		45	mA	V_{CC} = 5.0 V
t_{pd+}				25	35			ns	V_{CC} = 5.0 V, R_X = 5.0 kΩ C_X = 0, C_L = 15 pF
t_{pd-}				29	43			ns	V_{CC} = 5.0 V R_X = 5.0 kΩ C_X = 0, C_L = 15 pF
$t_{pw(min)}$				72	90			ns	V_{CC} = 5.0 V R_X = 5.0 kΩ
				78	100			ns	C_X = 0, C_L = 15 pF
t_{pw}			3.08	3.42	3.76			μs	V_{CC} = 5.0 V, R_X = 10 kΩ, C_X = 1000 pF
C_{STRAY}		50			50		50	pF	Pins 2 and 14 to Ground
R_X	5.0	25	5.0		25	5.0	25	kΩ	

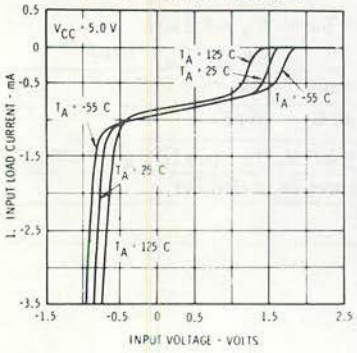
ELECTRICAL CHARACTERISTICS (T_A = 0°C to 75°C, V_{CC} = 5 V ± 5%)

Symbol	−0°C Min.	−0°C Max.	Limits +25°C Min.	+25°C Typ.	+25°C Max.	+75°C Min.	+75°C Max	Units	Conditions (Note 1)
V_{OH}	2.4		2.4	3.4		2.4		Volts	V_{CC} = 4.75 V, I_{OH} = −0.96 mA (Note 2)
V_{OL}		0.45		0.2	0.45		0.45	Volts	V_{CC} = 4.75 V, I_{OL} = 11.3 mA (Note 2) V_{CC} = 5.25 V, I_{OL} = 12.8 mA
V_{IH}	1.9		1.8			1.65		Volts	Guaranteed input high
V_{IL}		0.85			0.85		0.85	Volts	Guaranteed input low
I_{IL}		−1.6		−1.0	−1.6		−1.6	mA	V_{CC} = 5.25 V, V_{IN} = 0.45 V
		−1.41			−1.41		−1.41	mA	V_{CC} = 4.75 V, V_{IN} = 0.45 V
I_{IH}				10	60		60	μA	V_{CC} = 5.25 V, V_{IN} = 4.5 V
I_{SC}					−35			mA	V_{CC} = 5.25 V, V_{OUT} = 1.0 V (Note 2)
I_{PD}		52		39	50		52	mA	V_{CC} = 5.0 V, Ground, Pins 1 and 2
t_{pd+}				25	40			ns	V_{CC} = 5.0 V, R_X = 5.0 kΩ C_X = 0, C_L = 15 pF
t_{pd-}				29	48			ns	V_{CC} = 5.0 V R_X = 5.0 kΩ C_X = 0, C_L = 15 pF
$t_{pw(min)}$				72	100			ns	V_{CC} = 5.0 V R_X = 5.0 kΩ
				78	110			ns	C_X = 0, C_L = 15 pF
t_{pw}			3.08	3.42	3.76			μs	V_{CC} = 5.0 V, R_X = 10 kΩ, C_X = 1000 pF
C_{STRAY}		50			50		50	pF	Pins 2 and 14 to Ground
R_X	5.0	50	5.0		50	5.0	50	kΩ	

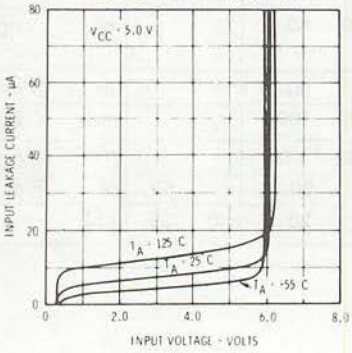
1. Unless otherwise noted, 10 kΩ resistor placed between Pin 2 (14) and V_{CC}, for all tests. (R_X)
2. Ground Pin 1 (15) for V_{OL} on Pin 7 (9), or for V_{OH} on Pin 6 (10), or for I_{SC} on Pin 6 (10); also, apply momentary ground to Pin 4 (12). Open Pin 1 (15) for V_{OL} on Pin 6 (10), or for V_{OH} on Pin 7 (9), or for I_{SC} on Pin 7 (9).

TYPICAL ELECTRICAL CHARACTERISTICS

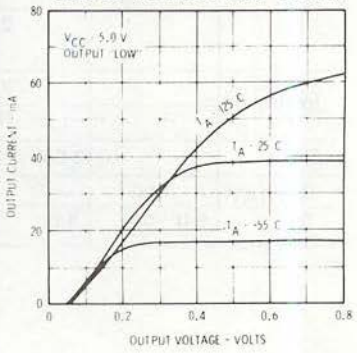
INPUT LOAD CURRENT VERSUS INPUT VOLTAGE



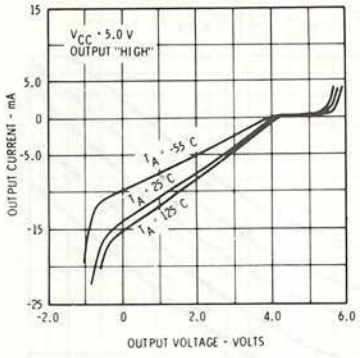
INPUT LEAKAGE CURRENT VERSUS INPUT VOLTAGE



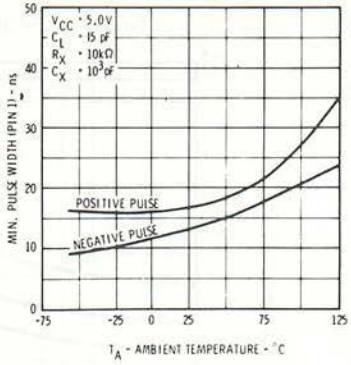
OUTPUT CURRENT VERSUS OUTPUT VOLTAGE (LOW STATE)



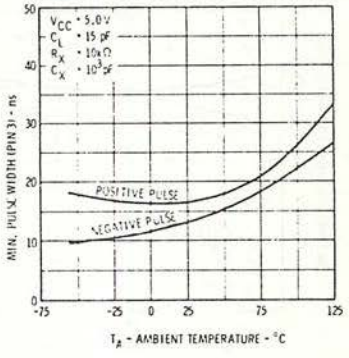
OUTPUT CURRENT VERSUS OUTPUT VOLTAGE (HIGH STATE)



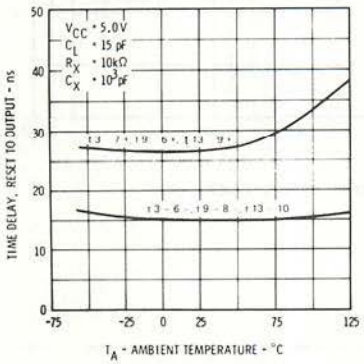
MINIMUM PULSE WIDTH TO TRIGGER VERSUS AMBIENT TEMPERATURE (POSITIVE EDGE TRIGGER INPUT)



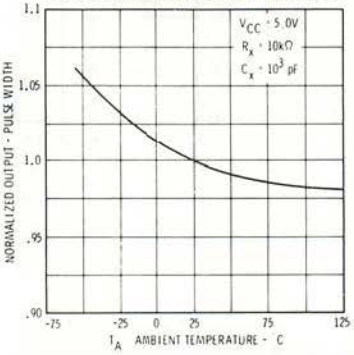
MINIMUM PULSE WIDTH TO TRIGGER VERSUS AMBIENT TEMPERATURE (NEGATIVE EDGE TRIGGER INPUT)



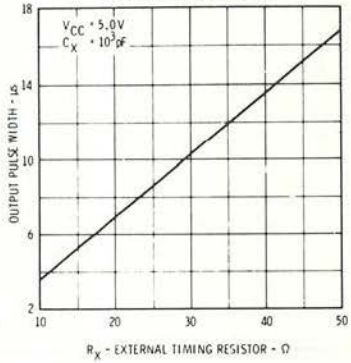
MINIMUM TIME DELAY, RESET TO OUTPUT VERSUS AMBIENT TEMPERATURE



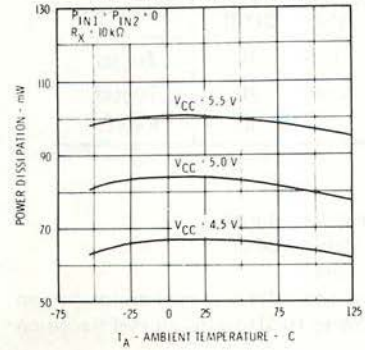
NORMALIZED OUTPUT PULSE WIDTH VERSUS SUPPLY VOLTAGE



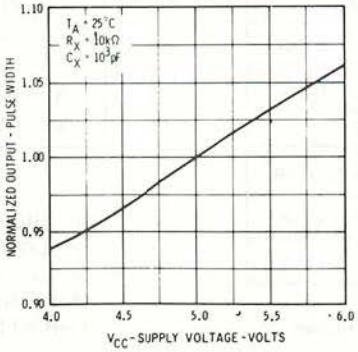
PULSE WIDTH VERSUS TIMING RESISTOR



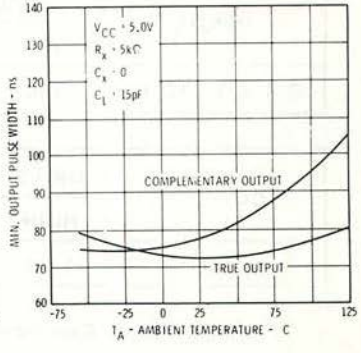
POWER DISSIPATION VERSUS AMBIENT TEMPERATURE



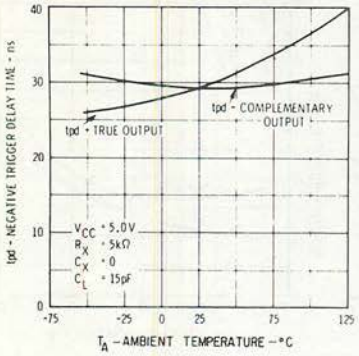
NORMALIZED OUTPUT PULSE WIDTH VERSUS SUPPLY VOLTAGE



MINIMUM OUTPUT PULSE WIDTH VERSUS AMBIENT TEMPERATURE

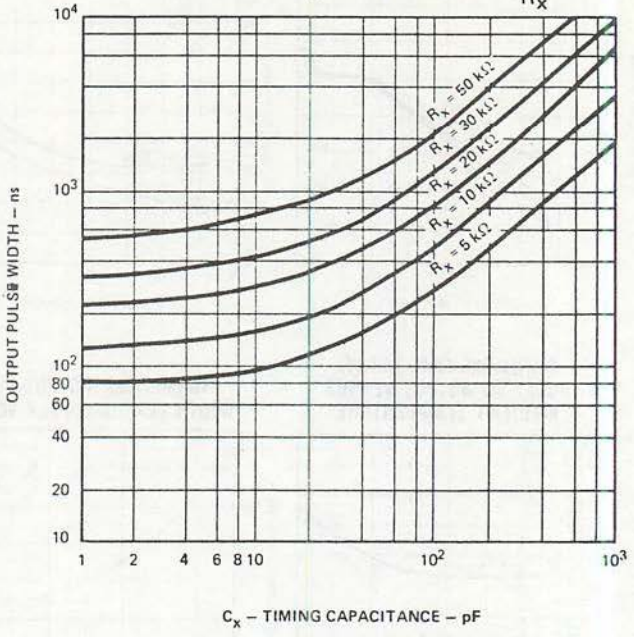


NEGATIVE TRIGGER DELAY TIME VERSUS AMBIENT TEMPERATURE



OUTPUT PULSE WIDTH VERSUS TIMING RESISTANCE AND CAPACITANCE FOR $C_x < 10^3$ pF

For $C_x \geq 10^3$ pF, $t_{pw} = 0.31\ R_x C_x\ (1 + \frac{1}{R_x})$



LOADING RULES

TTμL INPUT LOAD AND DRIVE FACTORS

INPUTS	LOAD	
	HIGH	LOW
3, 4, 5, 11, 12, 13	1 U.L.	1 U.L.

OUTPUTS	DRIVE FACTOR	
	HIGH	LOW
6, 7, 9, 10	16 U.L.	8 U.L.

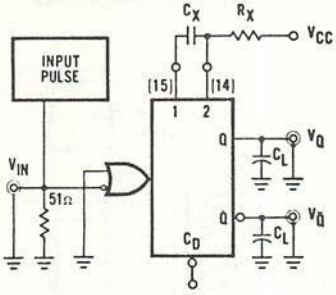
1 U.L. = 1 TTL Gate Input Load

TRIGGERING TRUTH TABLE

PIN NO'S. 5(11)	4(12)	3(13)	Operation
H→L	L	H	Trigger
H	L→H	H	Trigger
X	X	L	Reset

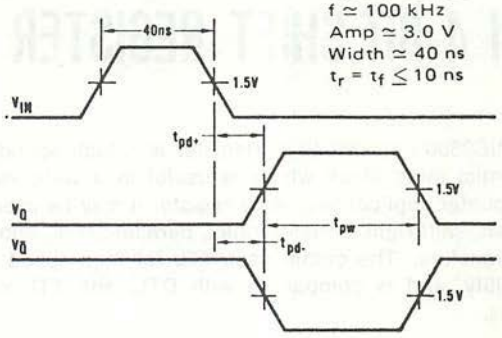
H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
H→L = HIGH to LOW Voltage Level transition
L→H = LOW to HIGH Voltage Level transition

SWITCHING CIRCUITS AND WAVEFORMS

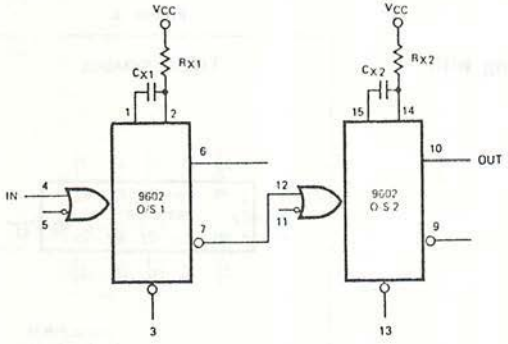


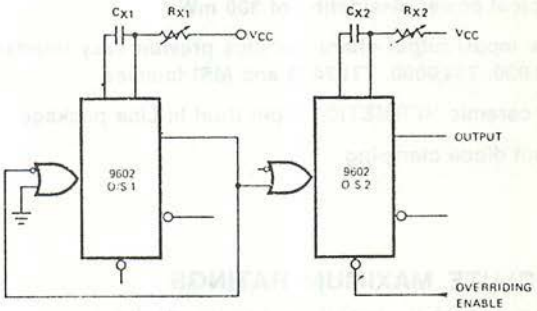
V_{CC} = Pin 16
GND = Pin 8

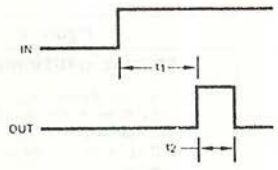
INPUT PULSE
f ≃ 100 kHz
Amp ≃ 3.0 V
Width ≃ 40 ns
$t_r = t_f \leq 10$ ns

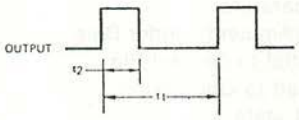


APPLICATIONS









The first one-shot determines the time t_1 before the initiation of the output pulse. The second one-shot determines t_2 the output pulse width.

PULSE GENERATOR

The output frequency produced with the above configuration is determined by C_{X1} and R_{X1}, while the pulse width is determined by C_{X2} and R_{X2}. O/S 1 forms an astable multivibrator with an output pulse width of approximately 25 ns, while O/S 2 extends the pulse width to the required value.

MSI 4-BIT SHIFT REGISTER

The MIC9300 Four Bit Shift Register is a high speed multi-functional sequential logic block which is useful in a wide variety of register and counter applications. As a register it may be used in serial-serial, shift left, shift right, serial-parallel, parallel-serial, and parallel-parallel data transfers. The circuit uses TTL for high speed and high fanout capability, and is compatible with DTL, and TTL digital integrated circuits.

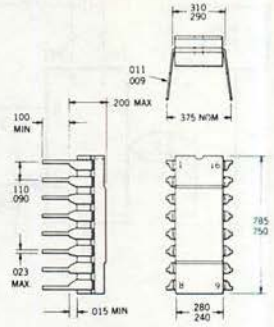
- **15 MHz shift frequency**
- **Synchronous parallel entry**
- **J, $\overline{K}$ inputs to first stage**
- **Asynchronous common reset**
- **Typical power dissipation of 300 mW**
- **The input/output characteristics provide easy interfacing with DTL930, TTL9000, TTL7400 and MSI families**
- **All ceramic HERMETIC 16 pin Dual In-Line package**
- **Input diode clamping**

ABSOLUTE MAXIMUM RATINGS

(above which the useful life may be impaired)

CHARACTERISTICS		UNITS
Storage Temperature	−65°C to +150	°C
Temperature (Ambient) Under Bias	−55°C to +125	°C
V_{CC} Pin Potential to Ground Pin	−0.5V to +7	Volts
Voltage Applied to Outputs for high output state	−0.5V to +V_{CC}	value
Input Voltage (D.C.)	−0.5V to +5.5	Volts

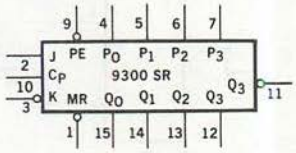
PHYSICAL DIMENSIONS



NOTES:
1. Leads are intended for insertion in hole rows on .300" centers. They are purposely shipped with positive (.375) misalignment to facilitate insertion.
2. Board drilling dimensions should equal your practice for a conventional .020 inch diameter lead.

Figure 1

LOGIC SYMBOL



V_{CC} = PIN 16
GND = PIN 8

Figure 2

SPECIAL ORDERING CODE

Temperature Range:
−55°C to +125°C, add -1 to MIC number.
0°C to +75°C, add -5 to MIC number.

Case Style:
¼" x ⅜" Flat Pack, add "B" following last digit.
Ceramic Dual In-Line, 16 leads, add "D" following last digit.

Example:
MIC9300-1D is −55°C to +125°C. Temperature range in Ceramic Dual-In-Line, 16 lead package.
Flat-pack and Dual-In-Line packages have same pin configuration.

FUNCTIONAL DESCRIPTION

The logic symbol of Figure 2 provides an indication of the functional characteristics of the MIC9300 four bit shift register. Several special logical features of the MIC9300 design which provide a high degree of general usefulness are described below:

1. A J$\overline{K}$ input is provided to the first flip flop in the register. This type of input is the same as the more common JK input except that the low voltage level activates the $\overline{K}$ input. This provides the greater power of the JK type input for more general applications and at the same time the simple D type input that is most appropriate for a shift register can be easily obtained by simply tying the two inputs together.
2. There is no restriction on the activity of the J or $\overline{K}$ inputs for logical operation — except for the set up and release time requirements.
3. Parallel inputs for all four stages are provided. These will determine the next condition of the shift register synchronous with the clock input, whenever the Parallel Enable input is low. With the Parallel Enable input low the element appears as four common clocked D flip flops. When the Parallel Enable is high, or not connected, the shift register performs a one bit shift for each clock input. In both cases the next state of the flip flop occurs after the low to high transition of the clock input.
4. An internal clock buffer provides both reduced clock input loading, and the ability to gate the clock with only a single NAND gate.
5. The active high output is provided for all four stages and an active low output is provided for the last stage.
6. A master asynchronous clear input allows the setting to zero of all stages, independent of the condition of any other inputs.

TABLE I — TRUTH TABLE FOR SERIAL ENTRY
(PE = HIGH, MR = HIGH, (n + 1) indicates state after next clock)

J	$\overline{K}$	Q_0 at t_{n+1}
L	L	L
L	H	Q_0 at t_n (no change)
H	L	$\overline{Q}_0$ at t_n (toggles)
H	H	H

TABLE II — LOADING RULES (1 U.L. = 1 TTL Gate Input Load)

INPUTS	LOADING
J, $\overline{K}$, $\overline{MR}$, P_0, P_1, P_2 & P_3	1 U.L.
$\overline{PE}$	2.3 U.L.
C_P	4 U.L.
OUTPUTS	**FANOUT**
Q_0, Q_1, Q_2, Q_3 & $\overline{Q}_3$	6 U.L.

ELECTRICAL CHARACTERISTICS (MIC9300-1X) ($T_A = -55°C$ to $+125°C$, $V_{CC} = 5.0\ V \pm 10\%$)

SYMBOL	CHARACTERISTICS	LIMITS						UNITS	CONDITIONS & COMMENTS
		−55°C		+25°C			+125°C		
		MIN.	MAX.	MIN.	TYP.	MAX.	MIN.	MAX.	
V_{OH}	Output High Voltage	2.2		2.4	2.7		2.4		Volts	$V_{CC} = 4.5\ V$, $I_{OH} = -0.36$ mA
V_{OL}	Output Low Voltage		0.4		0.2	0.4		0.4	Volts	$V_{CC} = 5.5\ V$, $I_{OL} = 9.6$ mA $V_{CC} = 4.5\ V$, $I_{OL} = 7.44$ mA
V_{IH}	Input High Voltage	2.0		1.7			1.4		Volts	Guaranteed input high threshold for all inputs
V_{IL}	Input Low Voltage		0.8			0.9		0.8	Volts	Guaranteed input low threshold for all inputs
I_F	Input Load Current* J, K, MR, P_0, P_1, P_2 & P_3		−1.6 −1.24		−1.10 −0.97	−1.6 −1.24		−1.6 −1.24	mA mA	$V_{CC} = 5.5\ V$ $V_{CC} = 4.5\ V$, $V_F = 0.4\ V$
I_R	Input Leakage Current* J, $\overline{K}$, $\overline{MR}$, P_0, P_1, P_2 & P_3				15	60		60	μA	$V_{CC} = 5.5\ V$, $V_R = 4.5\ V$

ELECTRICAL CHARACTERISTICS (MIC9300-5X) ($T_A = 0°C$ to $+75°C$, $V_{CC} = 5.0\ V \pm 5\%$)

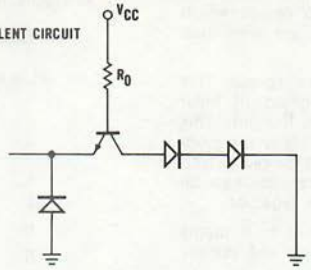
SYMBOL	CHARACTERISTICS	LIMITS						UNITS	CONDITIONS
		0°C		+25°C			+75°C		
		MIN.	MAX.	MIN.	TYP.	MAX.	MIN.	MAX.	
V_{OH}	Output High Voltage	2.4		2.4	3.0		2.4		Volts	$V_{CC} = 4.75\ V$, $I_{OH} = -0.36$ mA
V_{OL}	Output Low Voltage		0.45		0.2	0.45		0.45	Volts	$V_{CC} = 5.25\ V$, $I_{OL} = 9.6$ mA
V_{IH}	Input High Voltage	1.9		1.8			1.6		Volts	$V_{CC} = 4.75\ V$, $I_{OL} = 8.5$ mA Guaranteed input high threshold for all inputs
V_{IL}	Input Low Voltage		0.85			0.85		0.85	Volts	Guaranteed input low threshold for all inputs
I_F	Input Load Current* J, K, MR, P_0, P_1, P_2 & P_3		−1.6 −1.41		−1.0 −0.9	−1.6 −1.41		−1.6 −1.41	mA mA	$V_{CC} = 5.25\ V$ $V_{CC} = 4.75\ V$, $V_F = 0.45\ V$
I_R	Input Leakage Current* J, $\overline{K}$, $\overline{MR}$, P_0, P_1, P_2 & P_3				15	60		60	μA	$V_{CC} = 5.25\ V$, $V_R = 4.5\ V$

*For CP and $\overline{PE}$ input currents, use load factors in Table II

TYPICAL INPUT AND OUTPUT CHARACTERISTICS

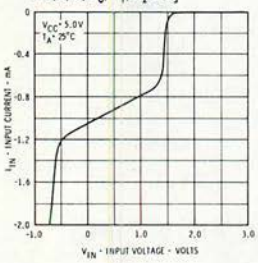
INPUTS

EQUIVALENT CIRCUIT

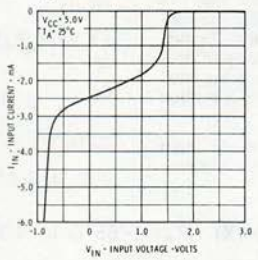


INPUT CURRENT VERSUS INPUT VOLTAGE

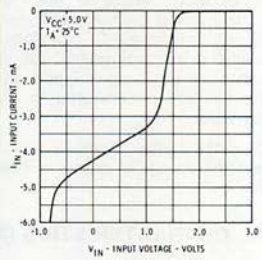
$\overline{MR}$, J, $\overline{K}$, P_0, P_1, P_2 & P_3



$\overline{PE}$

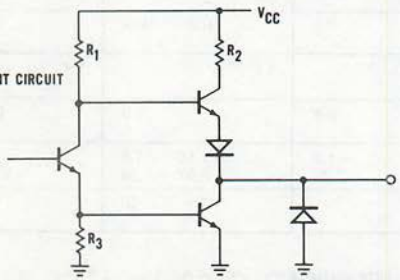


CP



OUTPUTS

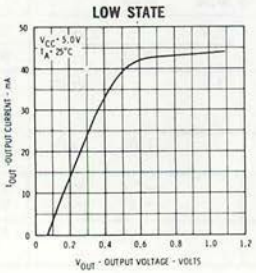
EQUIVALENT CIRCUIT



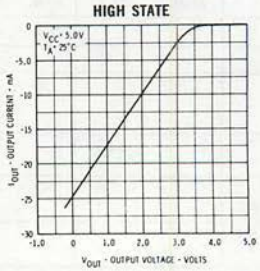
OUTPUT CURRENT VERSUS OUTPUT VOLTAGE

(Q_0, Q_1, Q_2, Q_3 AND $\overline{Q_3}$)

LOW STATE



HIGH STATE



SWITCHING CHARACTERISTICS ($T_A = 25°C$)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNITS	CONDITIONS & COMMENTS
t_{pd+}	Turn Off Delay		20	35	ns	$V_{CC} = 5.0$ V, $C_L = 15$ pF
t_{pd-}	Turn On Delay		25	45	ns	(See Fig. 5 & 6a)
f_{sr}	Shift Right Frequency	15	25		MHz	$V_{CC} = 5.0$ V, $C_L = 15$ pF (See Fig. 5 & 6c)
CP_{pw}	Clock Pulse Width	35	15		ns	
t_s	Set-up Time	35	17		ns	$V_{CC} = 5.0$ V
t_r	Release Time		16	0	ns	$C_L = 15$ pF
$t_s(\overline{PE})$	Set-up Time for $\overline{PE}$	45	26		ns	(See Figs. 6a & 6b)
$t_r(\overline{PE})$	Release Time for $\overline{PE}$		25	10	ns	
$t_{pd-}(\overline{MR})$	Reset Time for $\overline{MR}$		35		ns	
$t_{rec}(\overline{MR})$	Recovery Time for $\overline{MR}$		20		ns	
$\overline{MR}_{pw}$	Min Reset Pulse Width		15		ns	

SET-UP TIME: t_s is defined as the minimum time required for the logic level to be present at the logic input prior to the clock transition from low to high in order for the flip-flop(s) to respond.

RELEASE TIME: t_r is defined as the maximum time allowed for the logic level to be present at the logic input prior to the clock transition from low to high in order for the flip-flop(s) not to respond.

RECOVERY TIME FOR MR: t_{rec}(MR) is defined as the minimum time required between the end of the reset pulse and the clock transition from low to high in order for the flip-flop(s) to respond to the clock.

Figure 3

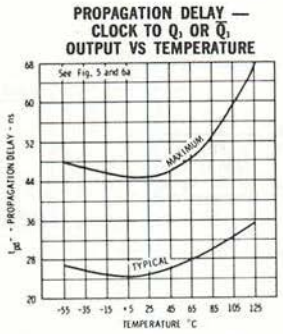
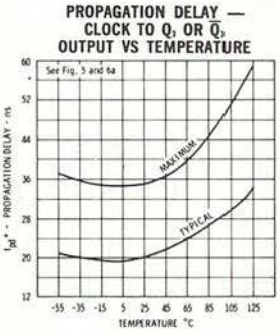
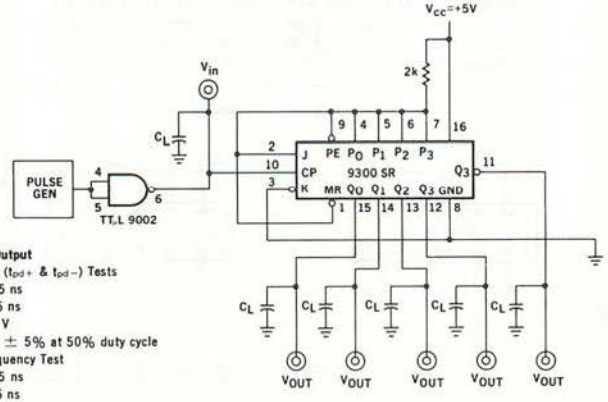


Figure 4





Pulse Generator Output

1. Switching Time (t_{pd+} & t_{pd-}) Tests
   Rise Time < 15 ns
   Fall Time < 15 ns
   Amplitude ≈ 4 V
   Freq. = 2 MHz ± 5% at 50% duty cycle
2. Shift Right Frequency Test
   Rise Time < 15 ns
   Fall Time < 15 ns
   Amplitude ≈ 4 V
   Freq. = 15 MHz with pulse width adjustment so that V_{IN} has duty cycle of approx. 50%.

Figure 5 — SWITCHING TIME & SHIFT RIGHT FREQUENCY TEST CIRCUIT

Fig. 6a

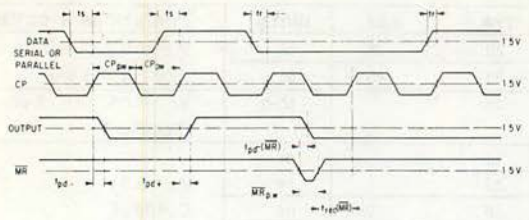


Fig. 6b

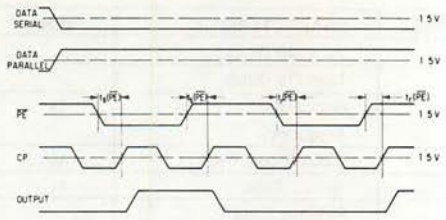
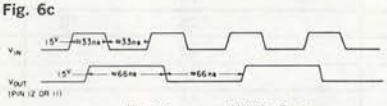


Fig. 6c



V_{OUT} Frequency = ½ X V_{IN} Frequency

Figure 6 — SWITCHING TIME & SHIFT RIGHT FREQUENCY WAVEFORMS

APPLICATIONS — The MIC9300 has been designed to be useful in a wide variety of applications. The multifunctional capability of the MIC9300 is illustrated by the applications shown below. below.

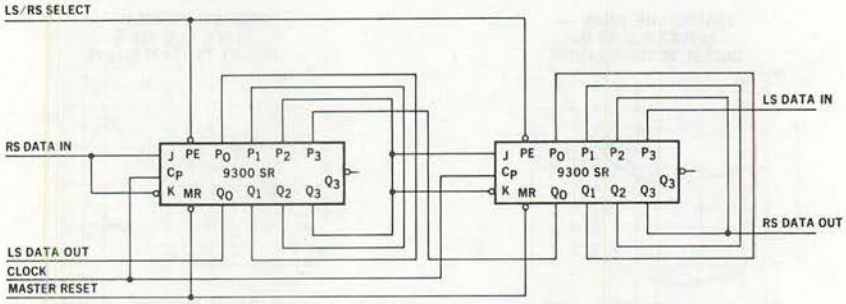


Figure 7 — EIGHT BIT LEFT/RIGHT SHIFT REGISTER

This register shifts Left or Right on each shift clock, depending upon the condition of the LS/RS SELECT input. If this input is high, Right Shift occurs and if low, Left Shift occurs.

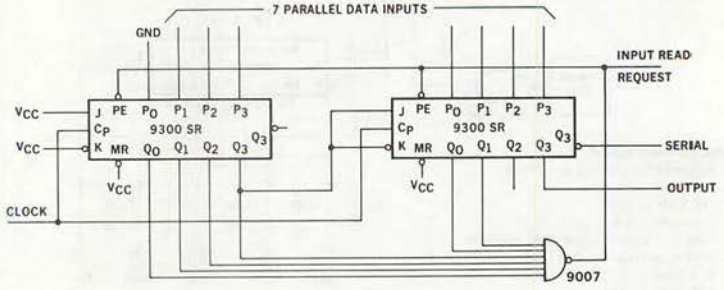


Figure 8 — SEVEN BIT PARALLEL TO SERIAL CONVERTER

This parallel to serial converter uses a marker bit, to count the data bits shifted out, so that a parallel load enable is generated to load the next parallel word for conversion at the correct time.

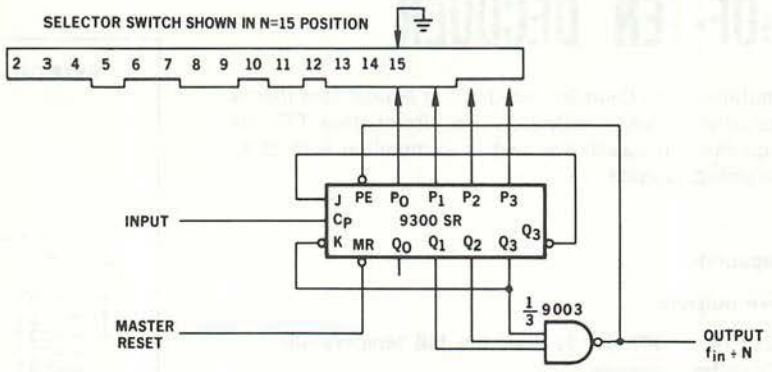
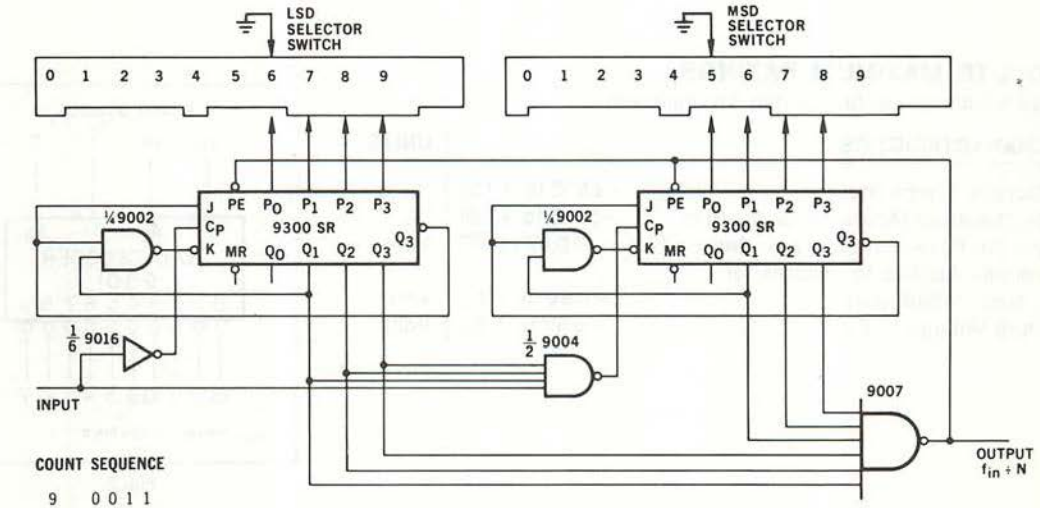


Figure 9 — DIVIDE BY N COUNTER FOR N=2 to 15

This counter produces an output pulse for every N input pulses, where the number N is determined by the setting of the slide selector switch as shown or by logic inputs to the parallel data lines from an external source.



COUNT SEQUENCE

9	0 0 1 1
8	0 0 0 1
7	0 0 0 0
6	1 0 0 0
5	1 1 0 0
4	0 1 1 0
3	1 0 1 1
2	1 1 0 1
1	1 1 1 0
0	0 1 1 1

Figure 10 — TWO DECADE PROGRAMMABLE DIVIDER

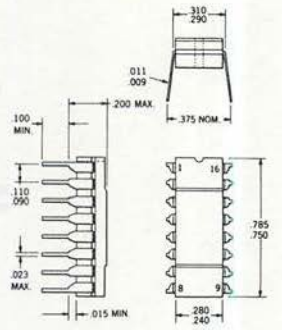
This circuit divides by any number "N" from 1 to 100. The selected N is one greater than is shown on the slide switches. As an example the switches are showing 56, therefore the circuit will divide by 57 with this setting.

MSI ONE-OF-TEN DECODER

The MIC9301 is a multipurpose decoder designed to accept four inputs and provide 10 mutually exclusive outputs. The circuit uses TTL for high speed and high fan out capability, and is compatible with DTL, and TTL digital integrated circuits.

- **Multi-function capability**
- **Mutually exclusive outputs**
- **Guaranteed fanout of 10 TTL loads over the full temperature range and supply voltage ranges**
- **High capacitive drive capability**
- **Demultiplexing capability**
- **Typical power dissipation of 145 mW**
- **The input/output characteristics provide easy interfacing with DTL930, TTL9000, TTL7400 and MSI families**
- **All ceramic HERMETIC 16-pin Dual In-Line package**
- **Input clamp diodes limit high speed line termination effects**

PHYSICAL DIMENSIONS



NOTES:
1. Leads are intended for insertion in hole rows on .300" centers. They are purposely shipped with "positive" (.375) misalignment to facilitate insertion.
2. Board drilling dimensions should equal your practice for a conventional .020 inch diameter lead.

Fig. 1

ABSOLUTE MAXIMUM RATINGS

(above which the useful life may be impaired)

CHARACTERISTICS		UNITS
Storage Temperature	−65°C to +150	°C
Temperature (Ambient) Under Bias	−55°C to +125	°C
V_{CC} Pin Potential to Ground Pin	−0.5V to +7	Volts
Voltage Applied to Outputs for high output state	−0.5V to +V_{CC}	value
Input Voltage (D.C.)	−0.5V to +5.5	Volts

LOGIC SYMBOL

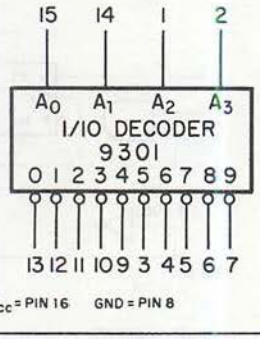


Fig. 2

ELECTRICAL CHARACTERISTICS (MIC9301-1X) ($T_A = -55°C$ to $+125°C$, $V_{CC} = 5.0\ V \pm 10\%$)

SYMBOL	CHARACTERISTICS	LIMITS −55°C MIN.	−55°C MAX.	+25°C MIN.	+25°C TYP.	+25°C MAX.	+125°C MIN.	+125°C MAX.	UNITS	CONDITIONS
V_{OH}	Output High Voltage	2.4		2.4	2.7		2.4		Volts	$V_{CC} = 4.5\ V$, $I_{OH} = -0.6\ mA$
V_{OL}	Output Low Voltage		0.4		0.2	0.4		0.4	Volts	$V_{CC} = 4.5\ V$, $I_{OL} = 12.4\ mA$ $V_{CC} = 5.5\ V$, $I_{OL} = 16.0\ mA$
V_{IH}	Input High Voltage	2.0		1.7			1.4		Volts	Guaranteed input high threshold for all inputs
V_{IL}	Input Low Voltage		0.8			.09		0.8	Volts	Guaranteed input low threshold for all inputs
I_F	Input Load Current		−1.6		−1.10	−1.6		−1.6	mA	$V_{CC} = 5.5\ V$, $V_F = 0.4\ V$
			−1.24		−0.97	−1.24		−1.24	mA	$V_{CC} = 4.5\ V$
I_R	Input Leakage Current				15	60		60	μA	$V_{CC} = 5.5\ V$, $V_R = 4.5\ V$
t_{pd+}	Turn Off Delay Input to Output				23	35			ns	$V_{CC} = 5.0\ V$
t_{pd-}	Turn On Delay Input to Output				20	30			ns	$C_L = 15\ pF$ See Fig. 8

FUNCTIONAL DESCRIPTION

The MIC9301 Decoder accepts four active high BCD inputs and provides ten mutually exclusive active low outputs, as shown by Figure 2. The active low outputs facilitate memory addressing when inverting drivers are used between decoder and memory elements such as the MIC9033.

The logic design of the MIC9301 ensures that all outputs are high when binary codes greater than nine are applied to the inputs.

The most significant A_3 input produces a useful inhibit function when the MIC9301 is used as a 1 out of 8 decoder. This is illustrated in the 1 out of 32 decoder shown in Figure 9.

The Truth Table and Loading Rules for the MIC9301 are shown in Table I and Table II.

SPECIAL ORDERING CODE

Temperature Range:
−55°C to +125°C, add -1 to MIC number.
0°C to +75°C, add -5 to MIC number.

Case Style:
¼" x ⅜" Flat Pack, add "B" following last digit.
Ceramic Dual In-Line, 16 leads, add "D" following last digit.

Example:
MIC9301-1D is −55°C to +125°C. Temperature range in Ceramic Dual-In-Line, 16 lead package. Flat-pack and Dual-In-Line packages have same pin configuration.

TABLE I — TRUTH TABLE

A_0	A_1	A_2	A_3	0	1	2	3	4	5	6	7	8	9
L	L	L	L	L	H	H	H	H	H	H	H	H	H
H	L	L	L	H	L	H	H	H	H	H	H	H	H
L	H	L	L	H	H	L	H	H	H	H	H	H	H
H	H	L	L	H	H	H	L	H	H	H	H	H	H
L	L	H	L	H	H	H	H	L	H	H	H	H	H
H	L	H	L	H	H	H	H	H	L	H	H	H	H
L	H	H	L	H	H	H	H	H	H	L	H	H	H
H	H	H	L	H	H	H	H	H	H	H	L	H	H
L	L	L	H	H	H	H	H	H	H	H	H	L	H
H	L	L	H	H	H	H	H	H	H	H	H	H	L
L	H	L	H	H	H	H	H	H	H	H	H	H	H
H	H	L	H	H	H	H	H	H	H	H	H	H	H
L	L	H	H	H	H	H	H	H	H	H	H	H	H
H	L	H	H	H	H	H	H	H	H	H	H	H	H
L	H	H	H	H	H	H	H	H	H	H	H	H	H
H	H	H	H	H	H	H	H	H	H	H	H	H	H

H = High Voltage Level
L = Low Voltage Level

TABLE II — LOADING RULES (1U.L. = TTL Gate Input Load)

INPUTS	LOADING
A_0, A_1, A_2 & A_3	1 U.L.

OUTPUTS	FANOUT
0, 1, 2, 3, 4, 5, 6, 7, 8, & 9	10 U.L.

ELECTRICAL CHARACTERISTICS (MIC9301-5X) (T_A = 0°C to +75°C, V_{CC} = 5.0 V ±5%)

SYMBOL	CHARACTERISTICS	LIMITS 0°C MIN.	0°C MAX.	+25°C MIN.	+25°C TYP.	+25°C MAX.	+75°C MIN.	+75°C MAX.	UNITS	CONDITIONS
V_{OH}	Output High Voltage	2.4		2.4	3.0		2.4		Volts	V_{CC} = 4.75 V, I_{OH} = −0.6 mA
V_{OL}	Output Low Voltage		0.45		0.2	0.45		0.45	Volts	V_{CC} = 4.75 V, I_{OL} = 14.1 mA V_{CC} = 5.25 V, I_{OL} = 16.0 mA
V_{IH}	Input High Voltage	1.9		1.8			1.6		Volts	Guaranteed input high threshold for all inputs
V_{IL}	Input Low Voltage		0.85			0.85		0.85	Volts	Guaranteed input low threshold for all inputs
I_F	Input Load Current		−1.6		−1.0	−1.6		−1.6	mA	V_{CC} = 5.25 V, V_F = 0.45 V
			−1.41		−0.9	−1.41		−1.41	mA	V_{CC} = 4.75 V, V_F = 0.45 V
I_R	Input Leakage Current				15	60		60	µA	V_{CC} = 5.25 V, V_R = 4.5 V
t_{pd+}	Turn Off Delay Input to Output				23	35			ns	V_{CC} = 5.0 V
t_{pd-}	Turn On Delay				20	30			ns	C_L = 15 pF See Fig. 8

TYPICAL INPUT AND OUTPUT CHARACTERISTICS

Fig. 3

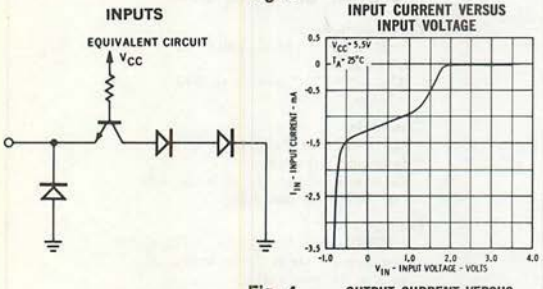


Fig. 4

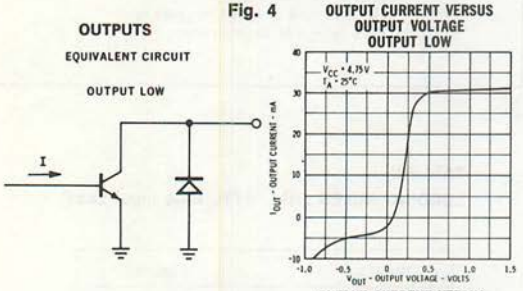
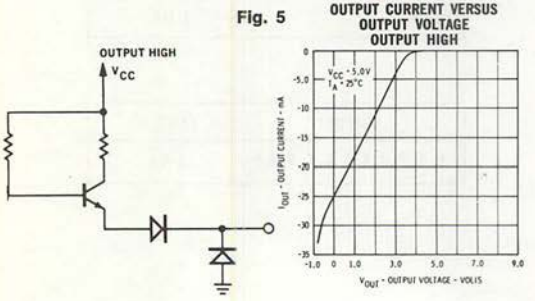


Fig. 5



SWITCHING PERFORMANCE

Fig. 6

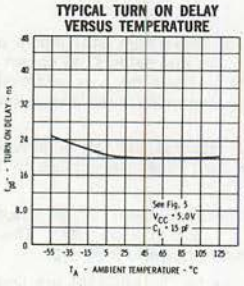
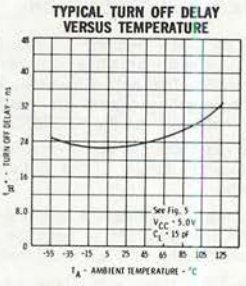
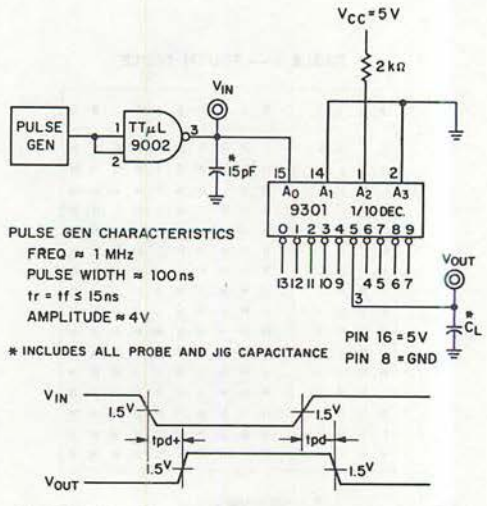


Fig. 7





SWITCHING TIME TEST CIRCUIT AND WAVEFORMS

Fig. 8

APPLICATIONS — The MIC9301 decoder may be used for BCD to Decimal or 3 bit binary to octal conversion as well as many other applications. The general purpose nature of the MIC9301 is indicated by its use in the following applications.

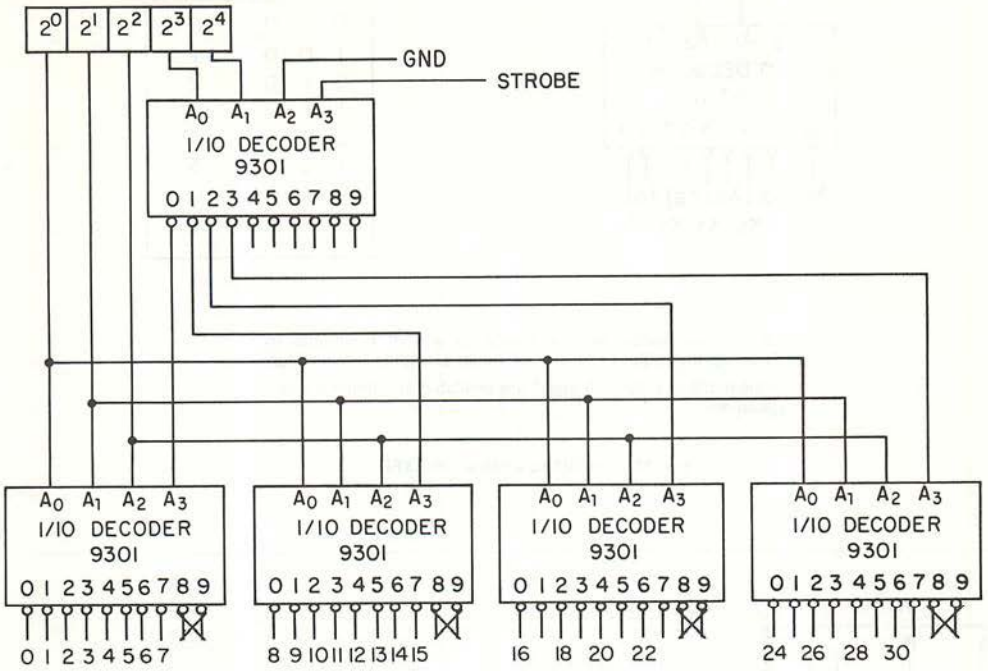
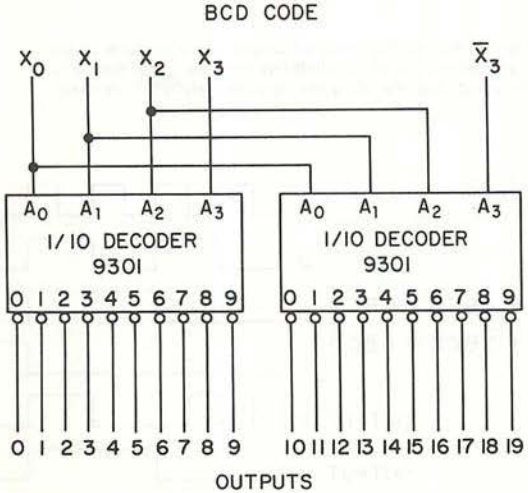


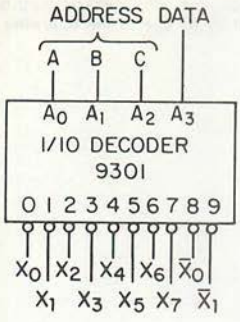
Fig. 9 — ONE-OUT-OF-THIRTY-TWO DECODING



DECIMAL DIGIT	OUTPUT SELECTION BCD CODE 8421	5421	EXCESS 3	4221
0	0, 18	0, 18	3	0, 18
1	1, 19	1, 19	4	1, 19
2	2	2	5	2
3	3	3	6	3
4	4	4	7	6
5	5	8, 10	8, 10	9, 11
6	6	9, 11	9, 11	14
7	7	12	12	15
8	8, 10	13	13	16
9	9, 11	14	14	17

Decode any BCD code using two 9301 elements. Any 4 bit BCD code may be decoded by selecting outputs as shown in the table.

Fig. 10 — DECODE ANY BCD CODE

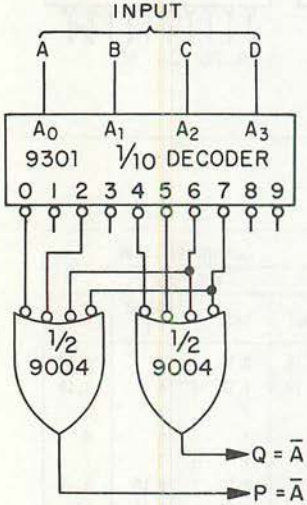


ADDRESS			OUTPUT LINE
A	B	C	
0	0	0	0
1	0	0	1
0	1	0	2
1	1	0	3
0	0	1	4
1	0	1	5
0	1	1	6
1	1	1	7

Data may be routed from a source to any of 8 outputs by addressing that output. All non-addressed outputs remain high.

Complements of outputs 0 and 1 are available at outputs 8 and 9 respectively.

Fig. 11 — DIGITAL DEMULTIPLEXER



Each output of the MIC9301 may be considered a minterm of the input code. Several sums of minterms may be generated economically using discrete IC gates and one MIC9301 decoder.

$Q = \bar{A}\bar{B}C\bar{D} + A\bar{B}C\bar{D} + \bar{A}BC\bar{D} + ABC\bar{D}$

$P = \bar{A}\bar{B}\bar{C}\bar{D} + \bar{A}B\bar{C}\bar{D} + \bar{A}BC\bar{D} + ABC\bar{D}$

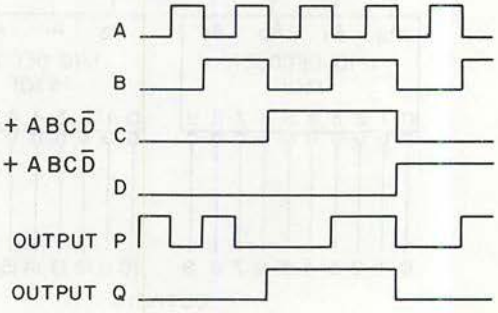


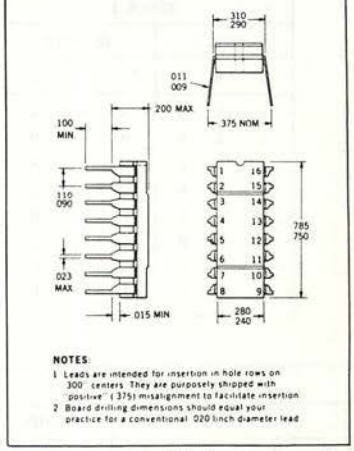
Fig. 12 — MINTERM GENERATOR

MSI DUAL FULL ADDER

- **Multi-function capability**
- **8ns carry propagation delay**
- **Complementary inputs and outputs available**
- **Typical power dissipation of 150mW**
- **The input/output characteristics provide easy interfacing with DTL930, TTL9000, TTL7400 and MSI families**
- **All ceramic HERMETIC 16-pin Dual In-Line package**
- **Input clamp diodes limit high speed termination effects**

The MIC9304 consists of two independent, high speed, binary full adders. The adders are useful in a wide variety of applications including multiple bit parallel add/serial carry addition, parity generation and checking, code conversion, and majority gating. The circuit uses TTL for high speed, high fanout operation and is compatible with DTL, and TTL digital integrated circuits.

PHYSICAL DIMENSIONS



NOTES:
1 Leads are intended for insertion in hole rows on .300" centers. They are purposely shipped with "positive" (.375) misalignment to facilitate insertion.
2 Board drilling dimensions should equal your practice for a conventional .020 inch diameter lead.

Fig. 1

LOGIC SYMBOL

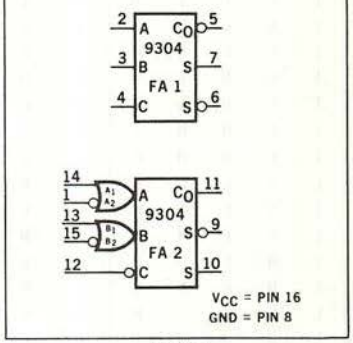


Fig. 2

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

CHARACTERISTICS		UNITS
Storage Temperature	−65°C to +150	°C
Temperature (Ambient) Under Bias	−55°C to +125	°C
V_{CC} Pin Potential to Ground Pin	−0.5V to +7	Volts
Voltage Applied to Outputs for high output state	−0.5V to +V_{CC}	value
Input Voltage (D.C.)	−0.5V to +5.5	Volts

TABLE I — TRUTH TABLES

ADDER 1					
INPUTS			OUTPUTS		
C	B	A	$\overline{C}_O$	$\overline{S}$	S
L	L	L	H	H	L
L	L	H	H	L	H
L	H	L	H	L	H
L	H	H	L	H	L
H	L	L	H	L	H
H	L	H	L	H	L
H	H	L	L	H	L
H	H	H	L	L	H

ADDER 2							
INPUTS					OUTPUTS		
$\overline{C}$	B_1	A_1	$\overline{B}_2$	$\overline{A}_2$	C_O	S	$\overline{S}$
L	L	L	L	L	H	H	L
L	L	L	L	H	H	L	H
L	L	L	H	L	H	L	H
L	L	L	H	H	L	H	L
L	L	H	L	L	H	H	L
L	L	H	L	H	H	H	L
L	L	H	H	L	H	L	H
L	L	H	H	H	H	L	H
L	H	L	L	L	H	H	L
L	H	L	L	H	H	L	H
L	H	L	H	L	H	H	L
L	H	L	H	H	H	L	H
L	H	H	L	L	H	H	L
L	H	H	L	H	H	H	L
L	H	H	H	L	H	H	L
L	H	H	H	H	H	H	L
H	L	L	L	L	H	L	H
H	L	L	L	H	L	H	L
H	L	L	H	L	L	H	L
H	L	L	H	H	L	L	H
H	L	H	L	L	H	L	H
H	L	H	L	H	H	L	H
H	L	H	H	L	L	H	L
H	L	H	H	H	L	H	L
H	H	L	L	L	H	L	H
H	H	L	L	H	L	H	L
H	H	L	H	L	H	L	H
H	H	L	H	H	L	H	L
H	H	H	L	L	H	L	H
H	H	H	L	H	H	L	H
H	H	H	H	L	H	L	H
H	H	H	H	H	H	L	H

H = High Voltage Level
L = Low Voltage Level

TABLE II —

LOADING RULES (1 U.L. = TTL Gate Input Unit Load)

INPUTS		LOADING
FA 1	A, B & C	4 U.L.
FA 2	$\overline{A}_2$, $\overline{B}_2$ & $\overline{C}$	4 U.L.
	A_1 & B_1	1 U.L.

OUTPUTS		FANOUT
FA 1	$\overline{C}_O$	7 U.L.
	$\overline{S}$	9 U.L.
	S	10 U.L.
FA 2	C_O	7 U.L.
	S	9 U.L.
	$\overline{S}$	10 U.L.

FUNCTIONAL DESCRIPTION

The MIC9304 logic block consists of two separate high speed carry dependent sum full adders. This design allows a minimum carry propagation time when the adders are used in ripple carry applications. The adders are identical except that adder 2 has provision for either active high or active low inputs at the A and B terminals. The adders produce a low carry and both low and high sum with active high inputs, a high carry and both high and low sum when active low inputs are used. This principle of duality is shown in Figure 12, where the adders are drawn as functional blocks.

The Truth Table and Loading Rules for the MIC9304 are shown in Table I and Table II.

SPECIAL ORDERING CODE

Temperature Range:
−55°C to +125°C, add -1 to MIC number.
0°C to +75°C, add -5 to MIC number.

Case Style:
¼" x ⅜" Flat Pack, add "B" following last digit.
Ceramic Dual In-Line, 16 leads, add "D" following last digit.

Example:
MIC9304-1D is −55°C to +125°C. Temperature range in Ceramic Dual-In-Line, 16 lead package. Flat-pack and Dual-In-Line packages have same pin configuration.

ELECTRICAL CHARACTERISTICS (MIC9304-1X) ($T_A = -55°C$ to $+125°C$, $V_{CC} = 5.0\ V \pm 10\%$)

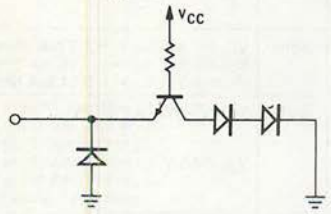
SYMBOL	CHARACTERISTICS	LIMITS −55°C MIN.	LIMITS −55°C MAX.	LIMITS +25°C MIN.	LIMITS +25°C TYP.	LIMITS +25°C MAX.	LIMITS +125°C MIN.	LIMITS +125°C MAX.	UNITS	CONDITIONS
V_{OH}	Output High Voltage	2.2		2.4	2.7		2.4		Volts	$V_{CC} = 4.5\ V$, $I_{OH} = -1.2\ mA$ (Pins 7 & 9) $V_{CC} = 4.5\ V$, $I_{OH} = -1.08\ mA$ (Pins 6 & 10) $V_{CC} = 4.5\ V$, $I_{OH} = -0.84\ mA$ (Pins 5 & 11)
V_{OL}	Output Low Voltage		0.4		0.21	0.4		0.4	Volts	$V_{CC} = 5.5\ V$, $I_{OL} = 16\ mA$ (Pins 7 & 9) $I_{OL} = 14.4\ mA$ (Pins 6 & 10) $I_{OL} = 11.2\ mA$ (Pins 5 & 11) $V_{CC} = 4.5\ V$, $I_{OL} = 12.4\ mA$ (Pins 7 & 9) $I_{OL} = 11.2\ mA$ (Pins 6 & 10) $I_{OL} = 8.7\ mA$ (Pins 5 & 11)
V_{IH}	Input High Voltage	2.0		1.7			1.4		Volts	Guaranteed input high threshold for all inputs
V_{IL}	Input Low Voltage		0.8			0.9		0.8	Volts	Guaranteed input low threshold for all inputs
I_F 4 I_F	Input Load Current Input Load Current		−1.6 −6.4		−1.1 −4.4	−1.6 −6.4		−1.6 −6.4	mA	$V_{CC} = 5.5\ V$; $V_F = 0.4\ V$, $V_R = 5.5\ V$ on other inputs
I_F 4 I_F	Input Load Current Input Load Current		−1.24 −4.96		−0.97 −3.88	−1.24 −4.96		−1.24 −4.96	mA	$V_{CC} = 4.5\ V$; $V_F = 0.4\ V$, $V_R = 5.5\ V$ on other inputs
I_R 4 I_R	Input Leakage Current Input Leakage Current				15 60	60 240		60 240	µA	$V_{CC} = 5.5\ V$, $V_R = 4.5\ V$ Ground on other inputs
t_{pd+}	C to C_O				8	13			ns	$V_{CC} = 5.0\ V$ $C_L = 15\ pF$ See Fig. 11
t_{pd-}	C to C_O				8	13			ns	
t_{pd+}	A_I to S				28	40			ns	
t_{pd-}	A_I to S				25	35			ns	

ELECTRICAL CHARACTERISTICS (MIC9304-5X) ($T_A = 0°C$ to $+75°C$, $V_{CC} = 5.0\ V \pm 5\%$)

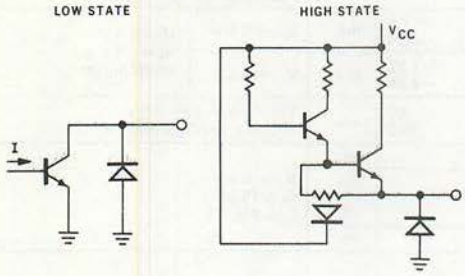
SYMBOL	CHARACTERISTICS	LIMITS 0°C MIN.	LIMITS 0°C MAX.	LIMITS +25°C MIN.	LIMITS +25°C TYP.	LIMITS +25°C MAX.	LIMITS +75°C MIN.	LIMITS +75°C MAX.	UNITS	CONDITIONS
V_{OH}	Output High Voltage	2.4		2.4	3.0		2.4		Volts	$V_{CC} = 4.75\ V$, $I_{OH} = -1.2\ mA$ (Pins 7 & 9) $V_{CC} = 4.75\ V$, $I_{OH} = -1.08\ mA$ (Pins 6 & 10) $V_{CC} = 4.75\ V$, $I_{OH} = -0.84\ mA$ (Pins 5 & 11)
V_{OL}	Output Low Voltage		0.45		0.21	0.45		0.45	Volts	$V_{CC} = 5.25\ V$, $I_{OL} = 16\ mA$ (Pins 7 & 9) $I_{OL} = 14.4\ mA$ (Pins 6 & 10) $I_{OL} = 11.2\ mA$ (Pins 5 & 11) $V_{CC} = 4.75\ V$, $I_{OL} = 14.1\ mA$ (Pins 7 & 9) $I_{OL} = 12.7\ mA$ (Pins 6 & 10) $I_{OL} = 9.85\ mA$ (Pins 5 & 11)
V_{IH}	Input High Voltage	1.9		1.8			1.6		Volts	Guaranteed input high threshold for all inputs
V_{IL}	Input Low Voltage		0.85			0.85		0.85	Volts	Guaranteed input low threshold for all inputs
I_F 4 I_F	Input Load Current Input Load Current		−1.6 −6.4		−1.0 −4.0	−1.6 −6.4		−1.6 −6.4	mA	$V_{CC} = 5.25\ V$, $V_F = 0.45\ V$ $V_R = 5.25\ V$ on other inputs
I_F 4 I_F	Input Load Current Input Load Current		−1.41 −5.64		−0.9 −3.6	−1.41 −5.64		−1.41 −5.64	mA	$V_{CC} = 4.75\ V$, $V_F = 0.45\ V$ $V_R = 5.25\ V$ on other inputs
I_R 4 I_R	Input Leakage Current Input Leakage Current				15 60	60 240		60 240	µA	$V_{CC} = 5.25\ V$, $V_R = 4.5\ V$ Ground on other inputs
t_{pd+}	C to C_O				8.0	15			ns	$V_{CC} = 5.0\ V$ $C_L = 15\ pF$ See Fig. 11
t_{pd-}	C to C_O				8.0	15			ns	
t_{pd+}	A_I to S				28	45			ns	
t_{pd-}	A_I to S				25	40			ns	

INPUTS

EQUIVALENT CIRCUIT



OUTPUTS



INPUT CURRENT VS INPUT VOLTAGE

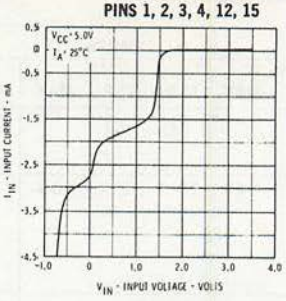


FIG. 4

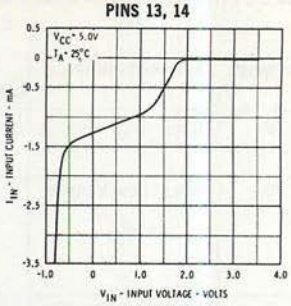


FIG. 3

OUTPUT CURRENT VS OUTPUT VOLTAGE

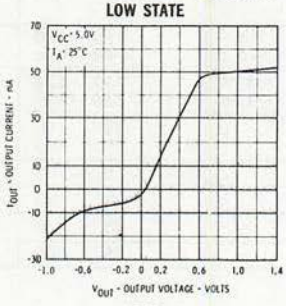


FIG. 5

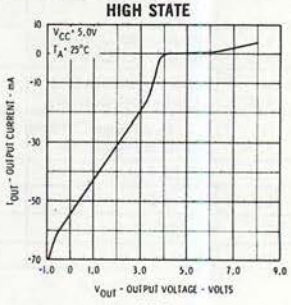


FIG. 6

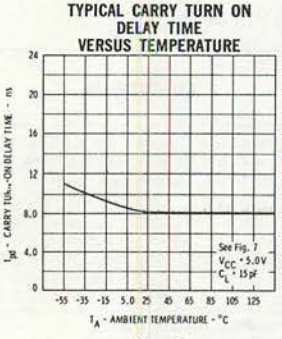


Fig. 7

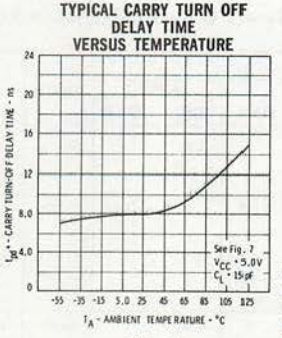


Fig. 8

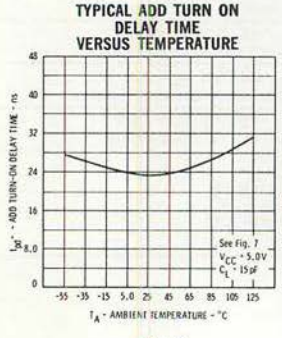


Fig. 9

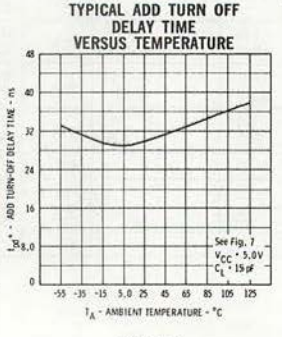
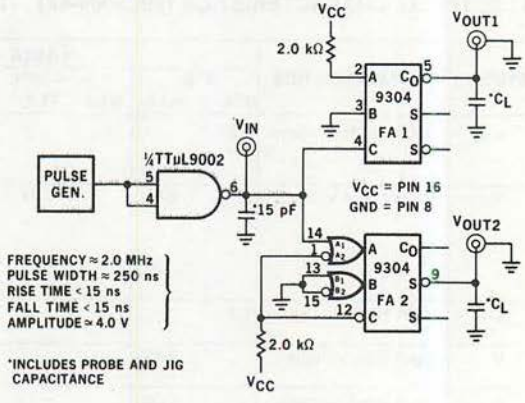


Fig. 10



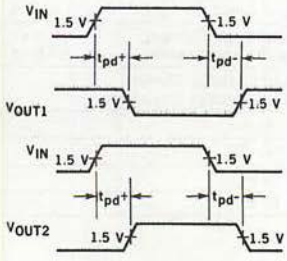


Fig. 11 — SWITCHING TIME TEST CIRCUIT AND WAVEFORMS

APPLICATIONS — The MIC9304 dual adder has been designed to be useful in a wide variety of applications such as addition, parity generation and checking, code conversion, majority gating and other applications for which this combination of logic gates may be useful. The multifunctional capabilities of the MIC9304 dual adder can be seen from reference to the applications shown.

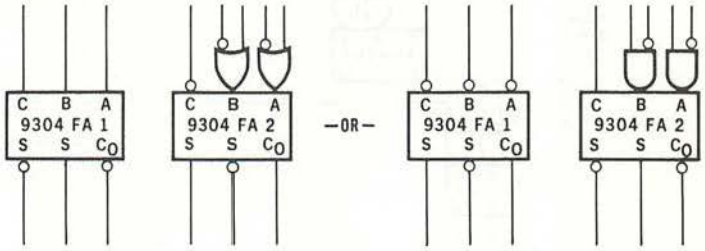


Fig. 12 — FUNCTIONAL BLOCK REPRESENTATION

The principle of duality allows 2 ways of representing each adder. The circuit is the same in both cases but the logic diagrams differ. The dual diagrams facilitate logic design and allow a greater understanding of the capabilities of the device.

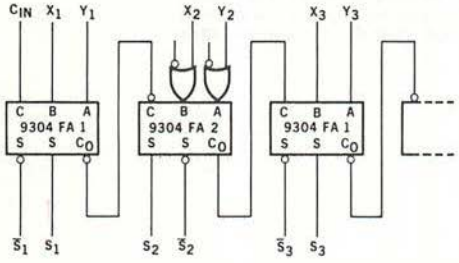


Fig. 13 — RIPPLE CARRY PARALLEL ADDITION

Shown above is a high speed ripple carry parallel addition scheme. Only one and-or-not gate delay is incurred at each stage allowing a typical addition speed of (N+1) x 8 ns, where N is the number of bits in the word. A similar scheme will work if the negation inputs are used, and the design acts as a subtractor when the complement of one variable is provided.

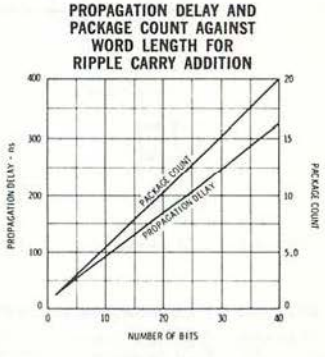


Fig. 14

The curve shows propagation delay of the ripple Carry Adder drawn in Figure 5. Plotted on the same diagram is a curve showing the low package count resulting from this Ripple Scheme.

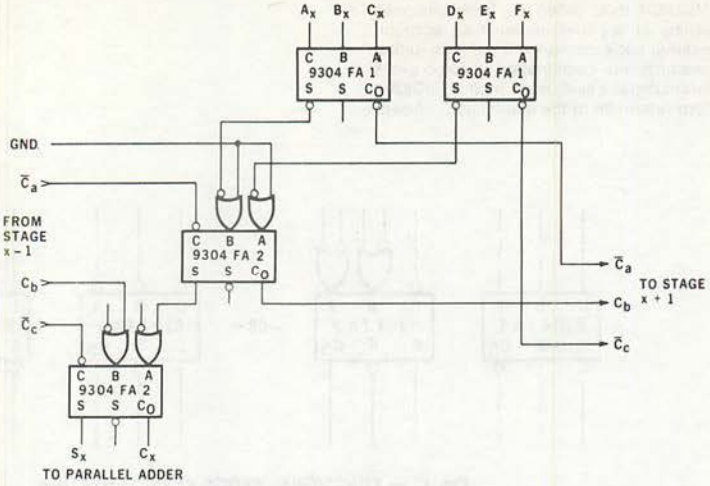


Fig. 15 — ADDITION OF SIX VARIABLES

The above design shows how the MIC9304 can be used in carry save arithmetic. Six input variable are reduced to two where they can be added in a parallel adder. Delay between inputs and outputs is typically 50 ns, allowing extremely high speed computation. Additional variables may be added or the concept can be extended to multiplication, division, and various other arithmetic operations.

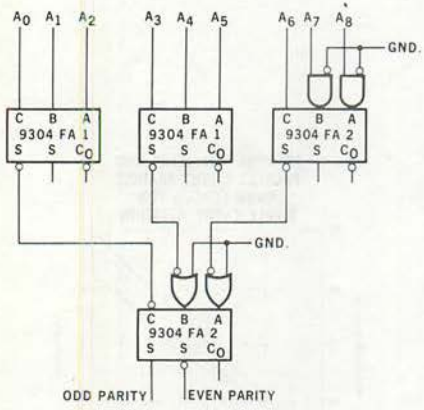


Fig. 16 — BYTE PARITY GENERATION OR CHECKING

The MIC9304 can be used for parity checking or generating. The above design uses 2 MIC9304's to generate parity for an 8 bit byte or check parity over 9 bits. The delay from input to odd parity is typically 35 ns. Additional adder blocks can be used to generate or check parity over larger word lengths. The concept can also be used for hamming and cyclic code generation and checking.

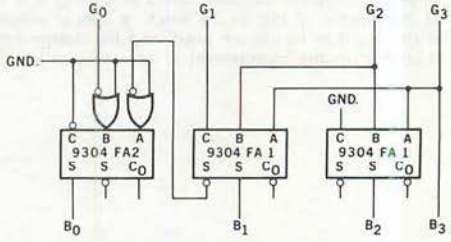


Fig. 17 — 4 BIT PARALLEL GRAY TO BINARY CONVERSION

A 4 bit parallel binary to gray conversion is shown. The adders can also be used for other cyclic code manipulations.

MSI DUAL FOUR-BIT LATCH

- **Active Level Low Enable Gate Inputs**
- **Overriding Master Reset**
- **25 ns Through Delay**
- **The Input/Output Characteristics Provide Direct Interfacing With Fairchild DTμL, LPDTμL, TTμL, and MSI Families (CCSL).**
- **Input Clamp Diodes Limit High Speed Termination Effects.**

The MSI MIC9308 is a Dual 4-Bit Latch designed for general purpose storage applications in high speed digital systems. The MIC9308 uses TTμL technology and is CCSL compatible. All inputs incorporate diode clamps to ground to reduce negative line transients. All outputs have active pull-up circuitry to provide high capacitive drive and low impedance outputs in both logic states to provide good A.C. noise immunity.

ABSOLUTE MAXIMUM RATINGS

(above which the useful life may be impaired)

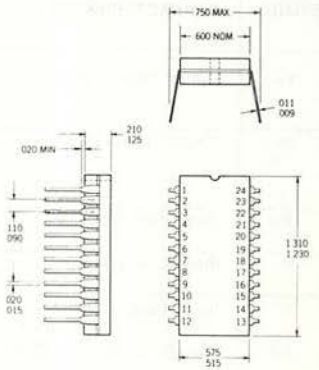
CONDITIONS		UNITS
Storage Temperature	−65 to +150	°C
Temperature (Ambient) Under Bias	−55 to +125	°C
V_{CC} Pin Potential to Ground Pin	−0.5 to +7	Volts
Input Voltage (D.C.) (See Note 1)	−0.5 to +5.5	Volts
Input Current (D.C.) (See Note 1)	−30 to +5	mA
Voltage Applied to Outputs (Output High)	−0.5 to +V_{CC}	value
Output Current (D.C.) (Output Low)	+30	mA

NOTE 1: Either Input Voltage limit or Input Current limit is sufficient to protect the inputs.

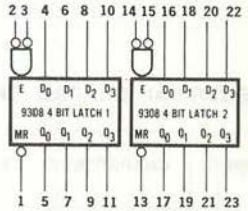
Description of Latch Operation—Data can be entered into the latch when both of the enable inputs are low. As long as this logic condition exists, the output of the latch will follow the input. If either of the enable inputs goes high, the data present in the latch at that time is held in the latch and is no longer affected by the data input.

The master reset overrides all other input conditions and forces the outputs of all the latches low when a low signal is applied to the master reset input.

PHYSICAL DIMENSIONS



LOGIC DIAGRAM



V_{CC} = Pin 24
Gnd = Pin 12

SPECIAL ORDERING CODE

Temperature Range:
−55°C to +125°C, add -1 to MIC number.
0°C to +75°C, add -5 to MIC number.

Case Style:
Ceramic Dual In-Line, 24 leads, add "D" following last digit.

Example:
MIC9301-1D is −55°C to +125°C.
Temperature range in Ceramic Dual-In-Line, 24 lead package.

ELECTRICAL CHARACTERISTICS (T_A = −55°C to +125°C, V_{CC} = 5.0 V ±10%, See Note 1)

SYMBOL	CHARACTERISTICS	LIMITS −55°C MIN.	LIMITS −55°C MAX.	LIMITS +25°C MIN.	LIMITS +25°C TYP.	LIMITS +25°C MAX.	LIMITS +125°C MIN.	LIMITS +125°C MAX.	UNITS	CONDITIONS
V_{OH}	Output High Voltage	2.4		2.4	2.8		2.4		Volts	V_{CC} = 4.5 V, I_{OH} = −0.6 mA Inputs at threshold voltages (V_{IL} or V_{IH}) (See Note 2)
V_{OL}	Output Low Voltage		0.4		0.21	0.4		0.4	Volts	V_{CC} = 5.5 V, I_{OL} = 14.4 mA V_{CC} = 4.5 V, I_{OL} = 11.2 mA Inputs at threshold voltages (V_{IL} or V_{IH}) (See Note 2)
V_{IH}	Input High Voltage	2.0		1.7			1.4		Volts	Guaranteed input high threshold for all inputs
V_{IL}	Input Low Voltage		0.8			0.9		0.8	Volts	Guaranteed input low threshold for all inputs
I_F	Input Load Current E_0, E_I and MR Inputs		−1.6		−1.1	−1.6		−1.6	mA	V_{CC} = 5.5 V, V_F = 0.4 V
1.5 I_F	Input Load Current D Inputs		−2.7		−1.9	−2.7		−2.7		V_F = 0.0 V (See Note 3)
I_R	Input Leakage Current E_0, E_I and MR Inputs				10	60		60	μA	V_{CC} = 5.5 V, V_R = 4.5 V
1.5 I_R	Input Leakage Current D Inputs				15	90		90		
I_{PD}	Power Supply Current		90		65	90		90	mA	V_{CC} = 5.0 V all outputs low inputs disabled

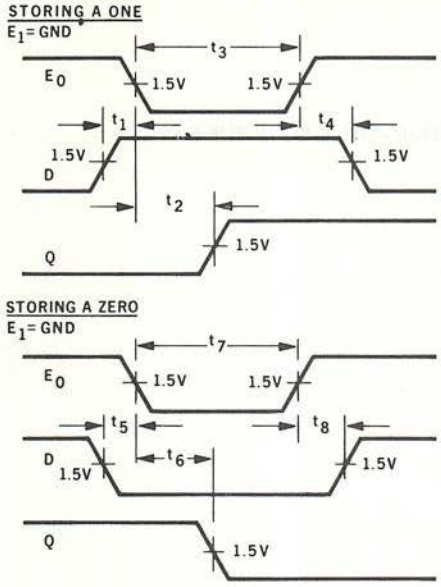
ELECTRICAL CHARACTERISTICS (T_A = 0°C to +75°C, V_{CC} = 5.0 V ±5%, See Note 1)

SYMBOL	CHARACTERISTICS	LIMITS 0°C MIN.	LIMITS 0°C MAX.	LIMITS +25°C MIN.	LIMITS +25°C TYP.	LIMITS +25°C MAX.	LIMITS +75°C MIN.	LIMITS +75°C MAX.	UNITS	CONDITIONS
V_{OH}	Output High Voltage	2.4		2.4	3.1		2.4		Volts	V_{CC} = 4.75 V, I_{OUT} = −0.6 mA Inputs at threshold voltages (V_{IL} or V_{IH}) (See Note 2)
V_{OL}	Output Low Voltage		0.45		0.21	0.45		0.45	Volts	V_{CC} = 5.25 V, I_{OUT} = 14.4 mA V_{CC} = 4.75 V, I_{OUT} = 12.7 mA Inputs at threshold voltages (V_{IL} or V_{IH}) (See Note 2)
V_{IH}	Input High Voltage	1.9		1.8			1.6		Volts	Guaranteed input high threshold for all inputs
V_{IL}	Input Low Voltage		0.85			0.85		0.85	Volts	Guaranteed input low threshold for all inputs
I_F	Input Load Current E_0, E_I and MR Inputs		−1.6		−1.0	−1.6		−1.6	mA	V_{CC} = 5.25 V, V_F = 0.45 V
1.5 I_F	Input Load Current D Inputs		−2.7		−1.8	−2.6		−2.7		V_F = 0.0 V (See Note 3)
I_R	Input Leakage Current E_0, E_I and MR Inputs				10	60		60	μA	V_{CC} = 5.25 V, V_F = 4.5 V
1.5 I_R	Input Leakage Current D Inputs				15	90		90		
I_{PD}	Power Supply Current		117		65	117		117	mA	V_{CC} = 5.0 V all outputs low inputs disabled

NOTE 1: Units are pulse tested.
NOTE 2: Output Voltages are guaranteed for either the input enabled or input disabled case.
NOTE 3: This current is measured at V_{IN} = 0.0 V to insure that no current is being absorbed by the device internally. The maximum value given guarantees that the maximum instantaneous current that can flow out of the input at V_{IN} = 0.4 V is 2.4 mA.

A.C. CHARACTERISTICS

9308 SWITCHING WAVEFORMS



TIME	DEFINITION	LIMIT (See Note 4)			
		MIN.	TYP.	MAX.	UNITS
t_1	Min. time that data must be present before enable to not increase t_2	X	minus 4	—	ns
t_2	Delay from enable to output turning off	—	22	X	ns
t_3	Min. enable pulse width to store a ONE	X	15	—	ns
t_4	Min. time that data must remain constant after removal of enable	X	5	—	ns
t_5	Min. time that data must be present before enable to not increase t_6	X	0	—	ns
t_6	Delay from enable to output turning on	—	15	X	ns
t_7	Min. enable pulse width to store a ZERO	X	15	—	ns
t_8	Min. time that data must remain constant after removal of enable	X	2	—	ns

NOTE 4: Limits indicated by X will be shown on final data sheets.

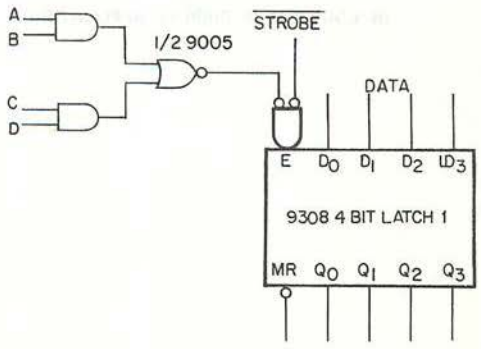
All delays are measured with V_{CC} = 5.0 V applied to Pin 24 and Pin 12 grounded. The active input is driven by a 9002 TT$_\mu$L gate with the output loaded with 15 pF. All outputs are loaded with 15 pF.

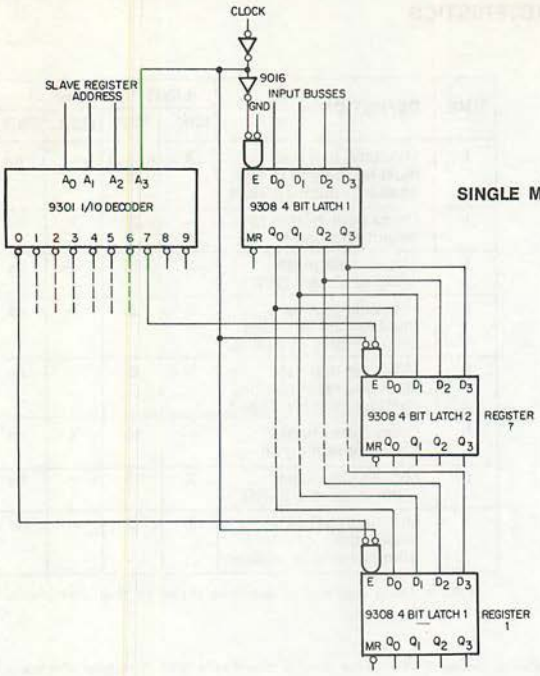
LOADING RULES

	PIN	LOADING
INPUTS	D_0, D_1, D_2, D_3	1.5
	MR, E_0, E_1	1.0
OUTPUTS	Q_0, Q_1, Q_2, Q_3	9.0

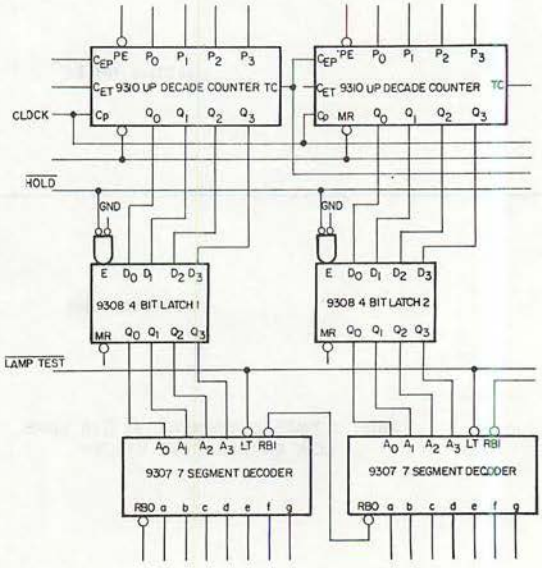
APPLICATIONS

AND-OR ENABLE SHOWING ACTIVE LEVEL LOW ENABLE GATE UTILITY





SINGLE MASTER/MULTIPLE SLAVE FLIP-FLOP



MIC9308 AS A HOLDING REGISTER IN COUNTING & DISPLAY APPLICATION

MSI DUAL FOUR-INPUT MULTIPLEXER

- **Multifunction Capability**
- **25 ns Through Delay**
- **On-Chip Select Logic Decoding**
- **Fully Buffered Complementary Outputs**
- **The Input/Output Characteristics Provide Easy Interfacing with DTL930, TTL9000, TTL7400 and MSI Families**
- **Input Clamp Diodes Limit High Speed Termination Effects**

The MIC9309 is a monolithic, high speed, dual four-input digital multiplexer circuit, constructed with a planar epitaxial process. It consists of two multiplexing circuits with common input select logic, each circuit contains four inputs and fully buffered complementary outputs. In addition to operating as a multiplexer, the MIC9309 can generate any two functions of three variables. Active pullups in the outputs ensure high drive and high speed performance. Because of its high speed performance and on-chip select decoding, the MIC9309 may be cascaded to multiple levels so that any number of lines can be multiplexed onto a single output buss. The circuit uses TTL for high speed, high fanout operation and is compatible with all DTL, and TTL digital integrated circuits.

ABSOLUTE MAXIMUM RATINGS

(above which the useful life may be impaired)

CHARACTERISTICS		UNITS
Storage Temperature	−65°C to +150	°C
Temperature (Ambient) Under Bias	−55°C to +125	°C
V_{CC} Pin Potential to Ground Pin	−0.5 V to +7	Volts
Voltage Applied to Output when output is high	0.V to +V_{CC}	value
Input Voltage (DC) (See Note 1)	−0.5 V to +5.5	Volts
Input Current (DC) (See Note 1)	−30 mA to +5	mA
Current into Output when output is low	+30	mA

Note 1: Either Input Voltage limit or Input Current limit is sufficient to protect the inputs.

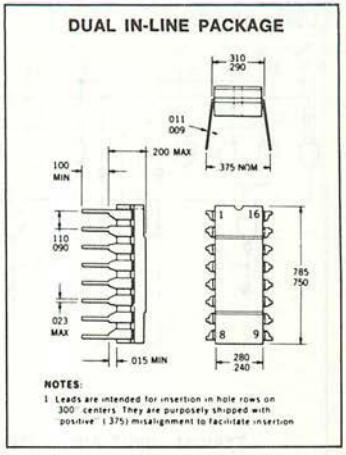


Fig. 1

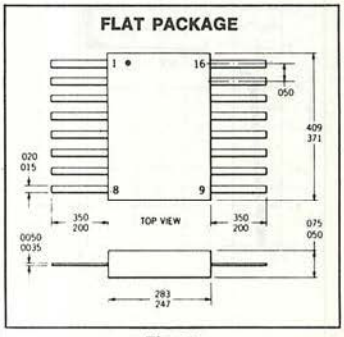


Fig. 2

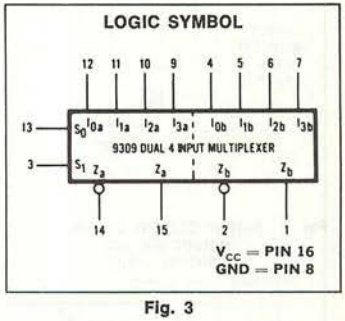


Fig. 3

LOGIC DIAGRAM

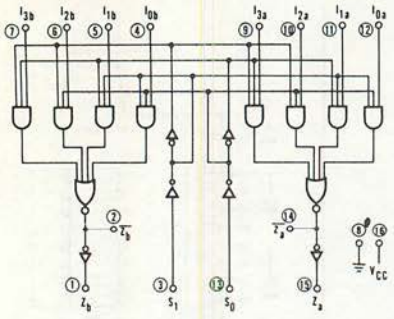


Fig. 4

FUNCTIONAL DESCRIPTION

The MIC9309 dual four input multiplexer is a member of the ITT family of compatible Medium Scale Integrated (MSI) digital building blocks. It provides this family with the ability to select two bits of either data or control from up to four sources, in one package.

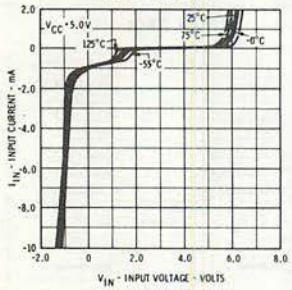
The MIC9309 dual four input multiplexer is the logical implementation of a two-pole four-position switch, with the position of the switch being set by the logic levels supplied to the two select inputs. Both assertion and negation outputs are provided for both multiplexers. The logic equations for the outputs are shown below:

$$Z_a = I_{0a} \cdot \overline{S}_1 \cdot \overline{S}_0 + I_{1a} \cdot \overline{S}_1 \cdot S_0 + I_{2a} \cdot S_1 \cdot \overline{S}_0 + I_{3a} \cdot S_1 \cdot S_0$$
$$Z_b = I_{0b} \cdot \overline{S}_1 \cdot \overline{S}_0 + I_{1b} \cdot \overline{S}_1 \cdot S_0 + I_{2b} \cdot S_1 \cdot \overline{S}_0 + I_{3b} \cdot S_1 \cdot S_0$$

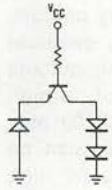
A common use of the MIC9309 would be the moving of data from a group of registers to a common output buss. The particular register from which the data came would be determined by the state of the select inputs. A less obvious use is as a function generator. The MIC9309 can generate any two functions of three variables. This is useful for implementing random gating functions.

TYPICAL INPUT AND OUTPUT CHARACTERISTICS

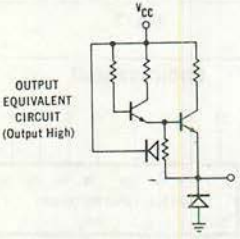
Fig. 5 INPUT CURRENT VERSUS INPUT VOLTAGE



INPUT EQUIVALENT CIRCUIT



OUTPUT EQUIVALENT CIRCUIT (Output High)



OUTPUT EQUIVALENT CIRCUIT (Output Low)

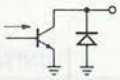


Fig. 6 OUTPUT CURRENT VERSUS OUTPUT VOLTAGE (OUTPUT HIGH)

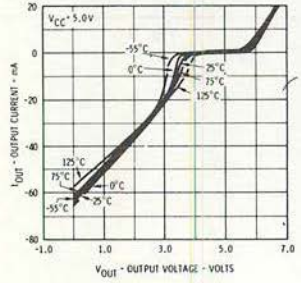
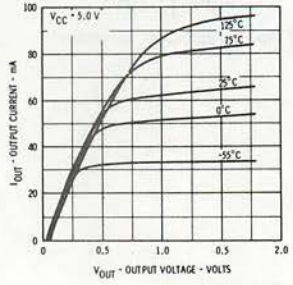


Fig. 7 OUTPUT CURRENT VERSUS OUTPUT VOLTAGE (OUTPUT LOW)



TRUTH TABLE

SELECT INPUTS		INPUTS				OUTPUTS	
S_0	S_1	I_{0a}	I_{1a}	I_{2a}	I_{3a}	Z_a	$\overline{Z}_a$
L	L	L	X	X	X	L	H
L	L	H	X	X	X	H	L
H	L	X	L	X	X	L	H
H	L	X	H	X	X	H	L
L	H	X	X	L	X	L	H
L	H	X	X	H	X	H	L
H	H	X	X	X	L	L	H
H	H	X	X	X	H	H	L
S_0	S_1	I_{0b}	I_{1b}	I_{2b}	I_{3b}	Z_b	$\overline{Z}_b$
L	L	L	X	X	X	L	H
L	L	H	X	X	X	H	L
H	L	X	L	X	X	L	H
H	L	X	H	X	X	H	L
L	H	X	X	L	X	L	H
L	H	X	X	H	X	H	L
H	H	X	X	X	L	L	H
H	H	X	X	X	H	H	L

L = low voltage level
H = high voltage level
X = either high or low logic level

LOADING RULES

(1 U.L. = 1 TTL gate input load)

INPUTS	LOADING
I_{0a}, I_{1a}, I_{2a}, I_{3a}, I_{0b}, I_{1b}, I_{2b}, I_{3b}, S_0, S_1	1 U.L.

	FANOUT AT LOGIC LEVEL	
OUTPUTS	HIGH	LOW
Z_a, Z_b	20 U.L.	10 U.L.
$\overline{Z}_a$, $\overline{Z}_b$	18 U.L.	9 U.L.

ELECTRICAL CHARACTERISTICS* (MIC9309-1X) ($T_A = -55°C$ to $+125°C$, $V_{CC} = 5.0\ V \pm 10\%$)

SYMBOL	CHARACTERISTICS	LIMITS −55°C MIN.	LIMITS −55°C MAX.	LIMITS +25°C MIN.	LIMITS +25°C TYP.	LIMITS +25°C MAX.	LIMITS +125°C MIN.	LIMITS +125°C MAX.	UNITS	CONDITIONS
V_{OH}	Output High Voltage	2.4		2.4	2.7		2.4		Volts	$V_{CC} = 4.5\ V$ $I_{OH} = -1.2$ mA (Pins 1 & 15) $V_{CC} = 4.5\ V$ $I_{OH} = -1.08$ mA (Pins 2 & 14) Inputs at threshold voltages (V_{IL} or V_{IH}) as per truth table
V_{OL}	Output Low Voltage		0.4		0.21	0.4		0.4	Volts	$V_{CC} = 5.5\ V$ $I_{OL} = 16.0$ mA (Pins 1 & 15) $I_{OL} = 14.4$ mA (Pins 2 & 14) $V_{CC} = 4.5\ V$ $I_{OL} = 12.4$ mA (Pins 1 & 15) $I_{OL} = 11.2$ mA (Pins 2 & 14) Inputs at threshold voltages (V_{IL} or V_{IH}) as per truth table
V_{IH}	Input High Voltage	2.0		1.7			1.4		Volts	Guaranteed input high threshold for all inputs
V_{IL}	Input Low Voltage		0.8			0.9		0.8	Volts	Guaranteed input low threshold for all inputs
I_F (all inputs)	Input Load Current		−1.6 −1.24		−1.1 −.85	−1.6 −1.24		−1.6 −1.24	mA mA	$V_{CC} = 5.5\ V$ $V_F = 0.4\ V$ $V_{CC} = 4.5\ V$ Input selected
I_R (all inputs)	Input Leakage Current				15	60		60	μA	$V_{CC} = 5.5\ V$ $V_R = 4.5\ V$ Input not selected
I_{PDH}	V_{CC} Current		40		30	40		40	mA	$V_{CC} = 5.0\ V$ All inputs high
t_{pd+} (S_0 to Z_n)	Switching Speed				24	32			ns	$V_{CC} = 5.0\ V$, $C_L = 15$ pF, See Figure 8
t_{pd-} (S_0 to Z_n)	Switching Speed				24	32			ns	

*Pulse tested

ELECTRICAL CHARACTERISTICS* (MIC9309-5X) ($T_A = 0°C$ to $+75°C$, $V_{CC} = 5.0\ V \pm 5\%$)

SYMBOL	CHARACTERISTICS	LIMITS 0°C MIN.	LIMITS 0°C MAX.	LIMITS +25°C MIN.	LIMITS +25°C TYP.	LIMITS +25°C MAX.	LIMITS +75°C MIN.	LIMITS +75°C MAX.	UNITS	CONDITIONS
V_{OH}	Output High Voltage	2.4		2.4	3.0		2.4		Volts	$V_{CC} = 4.75\ V$ $I_{OH} = -1.2$ mA (Pins 1 & 15) $V_{CC} = 4.75\ V$ $I_{OH} = -1.08$ mA (Pins 2 & 14) Inputs at threshold voltages (V_{IL} or V_{IH}) as per truth table
V_{OL}	Output Low Voltage		0.45		0.21	0.45		0.45	Volts	$V_{CC} = 5.25\ V$ $I_{OL} = 16.0$ mA (Pins 1 & 15) $I_{OL} = 14.4$ mA (Pins 2 & 14) $V_{CC} = 4.75\ V$ $I_{OL} = 14.1$ mA (Pins 1 & 15) $I_{OL} = 12.7$ mA (Pins 2 & 14) Inputs at threshold voltages (V_{IL} or V_{IH}) as per truth table
V_{IH}	Input High Voltage	1.9		1.8			1.6		Volts	Guaranteed input high threshold for all inputs
V_{IL}	Input Low Voltage		0.85			0.85		0.85	Volts	Guaranteed input low threshold for all inputs
I_F (all inputs)	Input Load Current		−1.6 −1.41		−1.0 −.91	−1.6 −1.41		−1.6 −1.41	mA mA	$V_{CC} = 5.25\ V$ $V_F = 0.45\ V$ $V_{CC} = 4.75\ V$ Input selected
I_R (all inputs)	Input Leakage Current				15	60		60	μA	$V_{CC} = 5.25\ V$ $V_R = 4.5\ V$ Input not selected
I_{PDH}	V_{CC} Current		43		30	43		43	mA	$V_{CC} = 5.0\ V$ All inputs high
t_{pd+} (S_0 to Z_n)	Switching Speed				24	36			ns	$V_{CC} = 5.0\ V$, $C_L = 15$ pF, See Figure 8
t_{pd-} (S_0 to Z_n)	Switching Speed				24	36			ns	

*Pulse tested

A.C. CHARACTERISTICS

SWITCHING WAVEFORMS

All inputs are outputs of TTL MIC9000 series gates loaded with 15 pF. All outputs are loaded with the same capacitance (referred to as C_L) and only with capacitance.

t_{pd}; S_0 to Z_a
CONDITIONS
Pins 3, 12 = GND.
Pin 11 = V_{CC}

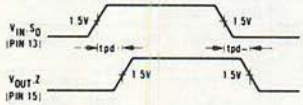


Fig. 8

t_{pd}; S_0 to $\overline{Z}_a$
CONDITIONS
Pins 3, 12 = GND.
Pin 11 = V_{CC}

Fig. 9

t_{pd}; I_{a0} to $\overline{Z}_a$
CONDITIONS
Pins 3, 13 = GND.

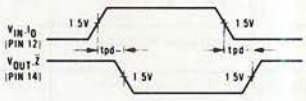


Fig. 10

SWITCHING CHARACTERISTICS

TURN OFF DELAY TIME VERSUS AMBIENT TEMPERATURE (S_0 to Z_a)

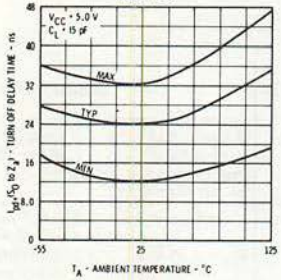


Fig. 11

TURN ON DELAY TIME VERSUS TEMPERATURE (S_0 to Z_a)

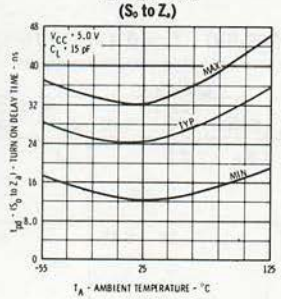


Fig. 12

TURN OFF DELAY TIME VERSUS AMBIENT TEMPERATURE (I_{0e} to $\overline{Z}_a$)

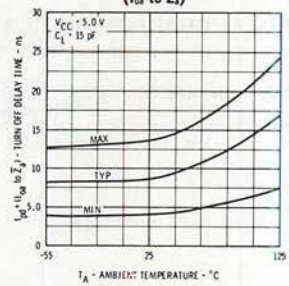


Fig. 13

TURN ON DELAY TIME VERSUS AMBIENT TEMPERATURE (I_{0e} to $\overline{Z}_a$)

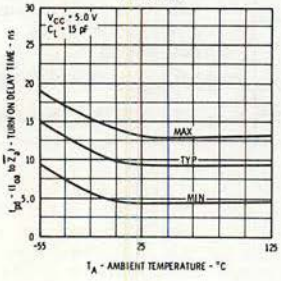


Fig. 14

TURN OFF DELAY TIME VERSUS AMBIENT TEMPERATURE (S_0 to $\overline{Z}_a$)

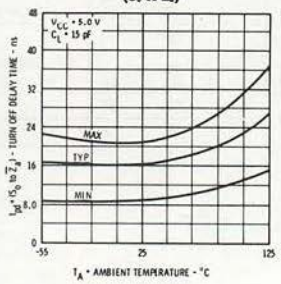


Fig. 15

TURN ON DELAY TIME VERSUS AMBIENT TEMPERATURE (S_0 to $\overline{Z}_a$)

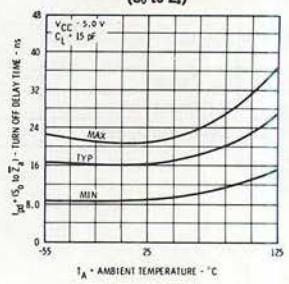


Fig. 16

APPLICATIONS

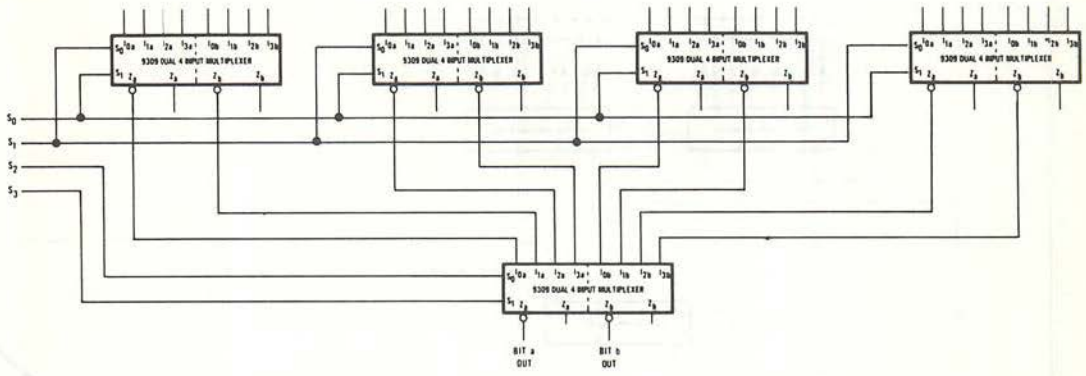
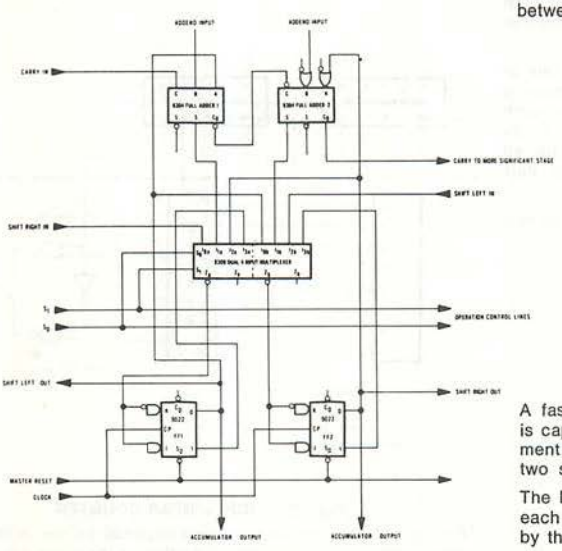


Fig. 12 — MULTIPLEXING TWO BITS FROM SIXTEEN SOURCES

This diagram shows the interconnection of five MIC9309 dual four bit multiplexers to provide switching of two bits of data from one of sixteen words onto a two bit data buss. The selection of which word will be transferred to the buss is made by the address supplied to the S_0, S_1, S_2 and S_3 inputs. As an example: if twelve bit words are to be transferred to a twelve bit buss, the above diagram would be repeated six times. Notice that the negative outputs are used at both levels resulting in the assertion output (negation of the negation) at a higher speed due to the fact that the through delay is less on the negation output.

If the word selecting address is held in four TTL flip flops (two dual packages) enough load capability is available to select between sixteen, sixteen bit words.



OPERATION CODE LIST

S_0	S_1	INSTRUCTION
0	0	SHIFT LEFT
1	0	ADD
0	1	SHIFT RIGHT
1	1	COMPLEMENT

H = "1", L = "0"

Fig. 13 — GENERAL PURPOSE ACCUMULATOR

A fast, general purpose accumulator for computer applications is capable of : 1) shift left; 2) add; 3) shift right and 4) complement operations. Only three packages are required to construct two stages of the general purpose accumulator shown above.

The D input capability of the MIC9022 is utilized here to allow each flip flop of the accumulator to accept the data as presented by the MIC9309 multiplexer.

Under the operation code instructions the multiplexer provides an input to the MIC9022 from: 1) adjacent stage to the right for a shift left operation; 2) adjacent stage to the left for a shift right operation; 3) output of adders for add operation and 4) Q outputs of MIC9022 for the complement operation. The operation code at the right of Figure 13 shows the instruction codes to perform the various operations. The accumulator should be capable of 20-25MHz operation.

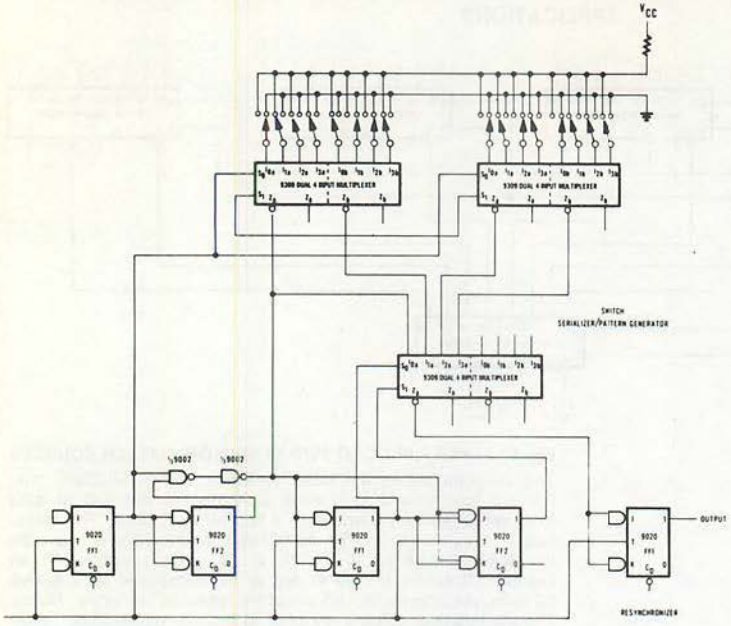


Fig. 14 — 16-BIT PATTERN GENERATOR

This application illustrates the use of MIC9309 and MIC9020 in the design of one channel of a 16 bit pattern generator. Each channel requires ½ MIC9020, ½ MIC9002 and 2½ MIC9309. Each channel consists of a switch serializer/pattern generator and resynchronizer sections with a modulo 16 binary counter common to all channels.

The two least significant bits and two most significant bits of the counter control the first and second stages of multiplexing respectively. In this manner four bits are multiplexed on each of the four lines from the first stage to the second stage. Every four clock times a new input line containing four multiplexed bits is selected by the second stage of the serializer thus serializing the 16 input bits from the switches.

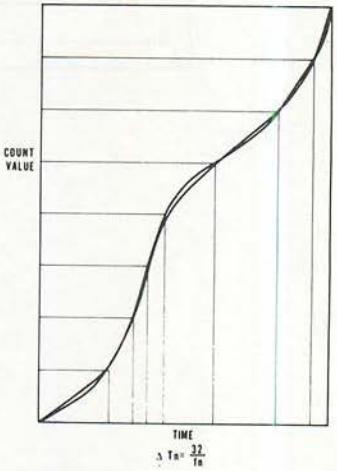
The resynchronizer flip flop is used to eliminate decoding spikes.

SPECIAL ORDERING CODE

Temperature Range:
−55°C to +125°C, add -1 to MIC number.
0°C to +75°C, add -5 to MIC number.

Case Style:
¼" x ⅜" Flat Pack, add "B" following last digit.
Ceramic Dual In-Line, 16 leads, add "D" following last digit.

Example:
MIC9309-1D is −55°C to +125°C. Temperature range in Ceramic Dual-In-Line, 16 lead package.
Flat-pack and Dual-In-Line packages have same pin configuration.



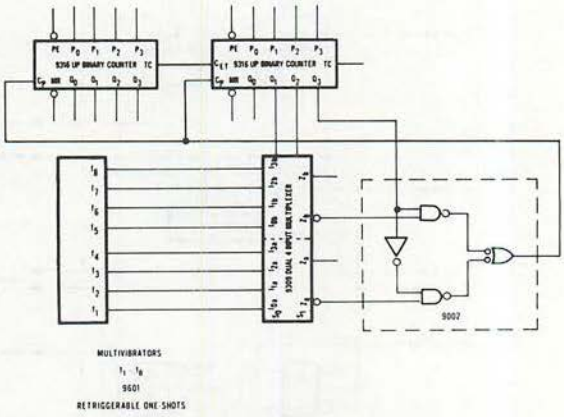


Fig. 15 — NON-LINEAR COUNTER

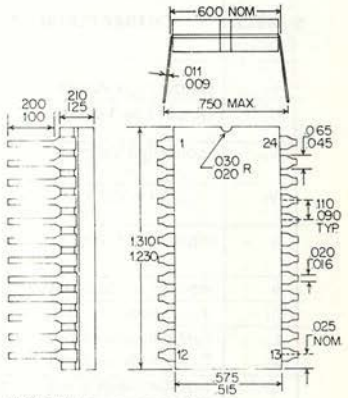
The rate of the non-linear counter depends on the multivibrator clock frequency selected under control of the three most significant bits of the counter. This makes the count rate a function of both the count value of counter and frequency of clock multivibrator selected.

Clock multiplexing is accomplished by a MIC9309 dual 4-input multiplexer and one MIC9002 quad gate. Eight line segments representing clock rates of the multivibrators may be adjusted in slope to approximate a non-linear function.

MSI ONE-OF-SIXTEEN DECODER

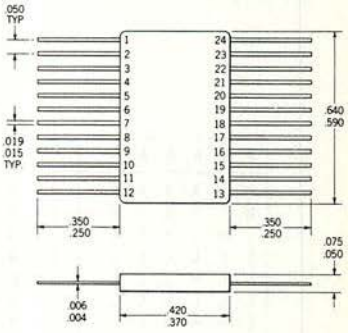
- **Multi-function capability**
- **Mutually exclusive outputs**
- **Guaranteed fanout of 10 TTL loads over the full temperature range and supply voltage ranges**
- **High capacitive drive capability**
- **Demultiplexing capability**
- **Typical power dissipation of 175 mW**
- **The input/output characteristics provide easy interfacing with DTL, 930 and TTL 54/7400 and 9300 families**
- **All ceramic "Hermetic" 24-pin dual in-line package**
- **Input clamp diodes limit high speed line termination effects**
- **Two input enable gate**

DUAL IN-LINE PACKAGE

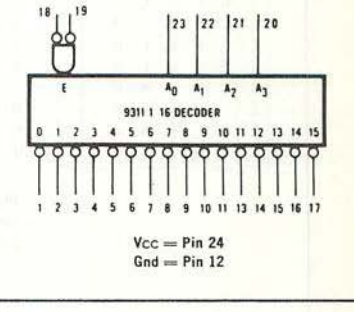


NOTES: All dimensions are in inches. Leads are intended for insertion in hole rows on .600 centers. They are purposely shipped with "positive" misalignment to facilitate insertion. Board drilling dimensions should equal your practice for .020 inch diameter lead. Leads are gold-plated Kovar. Package weight is 6.5 grams.

FLAT PACKAGE



LOGIC SYMBOL



Vcc = Pin 24
Gnd = Pin 12

The MIC9311 is a multi-purpose decoder designed to accept four inputs and provide 16 mutually exclusive outputs. The circuit uses TTL for high speed and high fan-out capability, and is compatible with all members of the 930 DTL, 54/7400 and 9300 families.

ABSOLUTE MAXIMUM RATINGS

(above which the useful life may be impaired)

CHARACTERISTICS		UNITS
Storage Temperature	−65 to +150	°C
Temperature (Ambient) Under Bias	−55 to +125	°C
V_{CC} Pin Potential to Ground Pin	−0.5 to +7	Volts
Voltage Applied to Outputs for high output state	−0.5 V to +V_{CC}	value
Input Voltage (D.C.)	−0.5 to +5.5	Volts

FUNCTIONAL DESCRIPTION — The 9311 decoder accepts four active high BCD inputs and provides 16 mutually exclusive active low outputs, as shown by Figure 1. The active low outputs facilitate memory addressing when inverting drivers are used between decoder and memory elements such as the 9033.

The most significant A_3 input produces a useful inhibit function when the 9311 is used as a 1 out of 8 decoder.

ELECTRICAL CHARACTERISTICS ($T_A = -55°C$ to $+125°C$, $V_{CC} = 5.0\ V \pm 10\%$) See Note 1

SYMBOL	CHARACTERISTICS	LIMITS −55°C MIN.	LIMITS −55°C MAX.	LIMITS +25°C MIN.	LIMITS +25°C TYP.	LIMITS +25°C MAX.	LIMITS +125°C MIN.	LIMITS +125°C MAX.	UNITS	CONDITIONS
V_{OH}	Output High Voltage	2.4		2.4	2.7		2.4		Volts	$V_{CC} = 4.5\ V$, $I_{OH} = -0.6\ mA$
V_{OL}	Output Low Voltage		0.4		0.2	0.4		0.4	Volts	$V_{CC} = 4.5\ V$, $I_{OL} = 12.4\ mA$ $V_{CC} = 5.5\ V$, $I_{OL} = 16.0\ mA$
V_{IH}	Input High Voltage	2.0		1.7			1.4		Volts	Guaranteed input high threshold for all inputs
V_{IL}	Input Low Voltage		0.8			0.9		0.8	Volts	Guaranteed input low threshold for all inputs
I_F	Input Load Current		−1.6		−1.10	−1.6		−1.6	mA	$V_{CC} = 5.5\ V$, $V_F = 0.4\ V$
			−1.24		−0.97	−1.24		−1.24	mA	$V_{CC} = 4.5\ V$
I_R	Input Leakage Current				15	60		60	μA	$V_{CC} = 5.5\ V$, $V_R = 4.5\ V$
I_{PD}	V_{CC} Current				35	55			mA	$V_{CC} = 5.0\ V$
t_{pd+}	Turn Off Delay A Input to Output				23	35			ns	$V_{CC} = 5.0\ V$ $C_L = 15\ pF$ See test circuit
t_{pd-}	Turn On Delay A Input to Output				20	30			ns	
t_{pd+}	Turn Off Delay E Input to Output				17	26			ns	
t_{pd-}	Turn On Delay E Input to Output				16	21			ns	

Note 1: Units are pulse tested.

TRUTH TABLE

Eo	EI	A_0	A_1	A_2	A_3	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
H	H	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
H	L	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	H	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	H	L	L	L	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	H	L	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	H	H	L	L	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	H	L	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H
L	L	H	L	H	L	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H
L	L	L	H	H	L	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H
L	L	H	H	H	L	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H
L	L	L	L	L	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H
L	L	H	L	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H
L	L	L	H	L	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H
L	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H
L	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H
L	L	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H
L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H
L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L

H = High Voltage Level
L = Low Voltage Level
X = Level Does Not Affect Output

TTL INPUT LOAD AND DRIVE FACTORS

INPUTS	LOADING
All Inputs	1 U.L.

OUTPUTS	DRIVE FACTOR
All Outputs	10 U.L.

(1 U.L. = TTL Gate Input Load)

INPUT LOAD AND DRIVE FACTORS

GRADE	INPUTS	LOADING
59	All Inputs	12/11
51	All Inputs	12/10

GRADE	OUTPUTS	DRIVE FACTOR
59	All Outputs	120/94
51	All Outputs	120/78

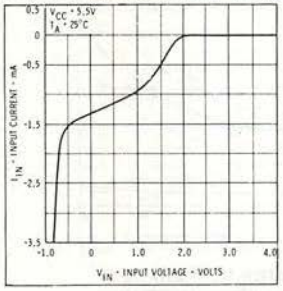
ELECTRICAL CHARACTERISTICS ($T_A = 0°C$ to $+75°C$, $V_{CC} = 5.0\ V \pm 5\%$) See Note 1

SYMBOL	CHARACTERISTICS	LIMITS 0°C MIN.	0°C MAX.	+25°C MIN.	+25°C TYP.	+25°C MAX.	+75°C MIN.	+75°C MAX.	UNITS	CONDITIONS
V_{OH}	Output High Voltage	2.4		2.4	3.0		2.4		Volts	$V_{CC} = 4.75\ V$, $I_{OH} = -0.6\ mA$
V_{OL}	Output Low Voltage		0.45		0.2	0.45		0.45	Volts	$V_{CC} = 4.75\ V$, $I_{OL} = 14.1\ mA$ $V_{CC} = 5.25\ V$, $I_{OL} = 16.0\ mA$
V_{IH}	Input High Voltage	1.9		1.8			1.6		Volts	Guaranteed input high threshold for all inputs
V_{IL}	Input Low Voltage		0.85			0.85		0.85	Volts	Guaranteed input low threshold for all inputs
I_F	Input Load Current		−1.6		−1.0	−1.6		−1.6	mA	$V_{CC} = 5.25\ V$, $V_F = 0.45\ V$
			−1.41		−0.9	−1.41		−1.41	mA	$V_{CC} = 4.75\ V$
I_R	Input Leakage Current				15	60		60	μA	$V_{CC} = 5.25\ V$, $V_R = 4.5\ V$
I_{PD}	V_{CC} Current				35	60			mA	$V_{CC} = 5.0\ V$
t_{pd+}	Turn Off Delay A Input to Output			10	23	40			ns	$V_{CC} = 5.0\ V$ $C_L = 15\ pF$ See test circuit
t_{pd-}	Turn On Delay A Input to Output			7.0	20	35			ns	
t_{pd+}	Turn Off Delay E Input to Output			10	17	31			ns	
t_{pd-}	Turn On Delay E Input to Output			7.0	17	26			ns	

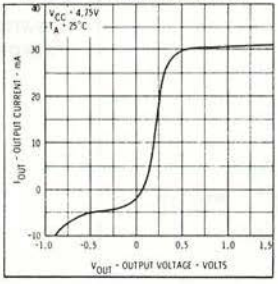
Note 1: Units are pulse tested.

TYPICAL INPUT AND OUTPUT CHARACTERISTICS

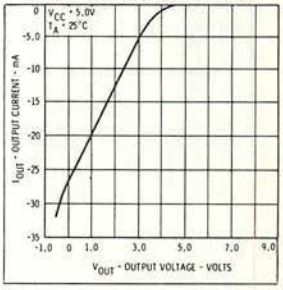
INPUT CURRENT VERSUS INPUT VOLTAGE

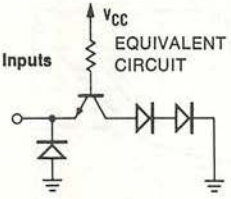


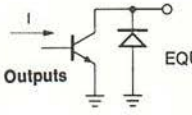
OUTPUT CURRENT VERSUS OUTPUT VOLTAGE OUTPUT LOW

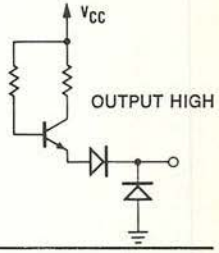


OUTPUT CURRENT VERSUS OUTPUT VOLTAGE OUTPUT HIGH





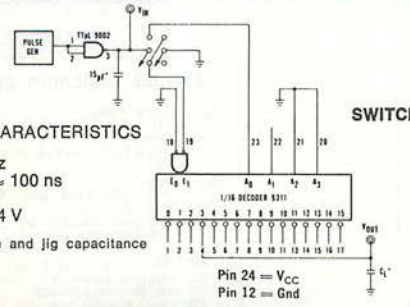




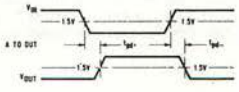
PULSE GEN CHARACTERISTICS

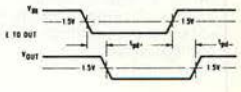
Freq. ≈ 1 MHz
Pulse Width ≈ 100 ns
$t_r = t_f \leq 15$ ns
Amplitude ≈ 4 V

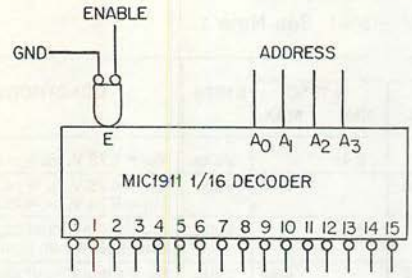
*Includes all probe and jig capacitance



SWITCHING TIME TEST CIRCUIT AND WAVEFORMS



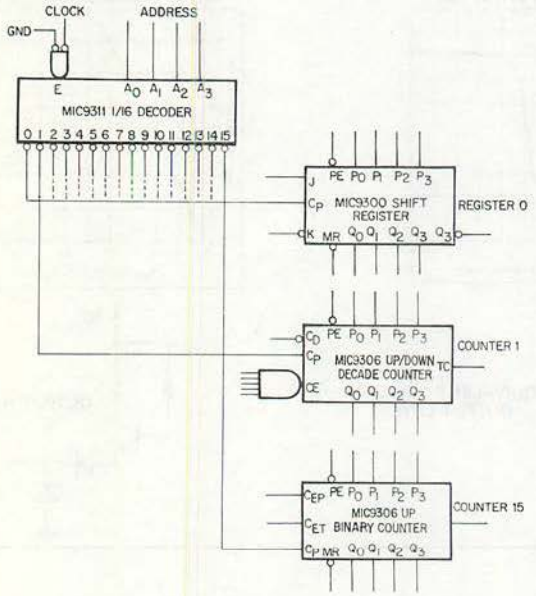




DECODE ANY BCD CODE

Decode any BCD code using a 9311 element. Any 4 bit BCD code may be decoded by selecting outputs, examples are shown in the table.

DECIMAL DIGIT	OUTPUT SELECTION			
	BCD CODE			
	8421	5421	EXCESS 3	GRAY
0	0	0	3	0
1	1	1	4	1
2	2	2	5	3
3	3	3	6	2
4	4	4	7	6
5	5	8	8	7
6	6	9	9	5
7	7	10	10	4
8	8	11	11	12
9	9	12	12	13

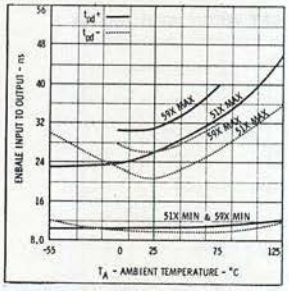


CLOCK DEMULTIPLEXING

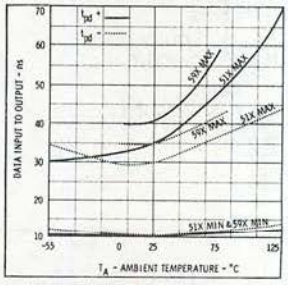
The 9311 can be used as a clock demultiplexer. The binary address designates to which register or counter the clock is sent. Up to 5 register counter stages can be driven by one decoder output allowing word lengths of 20 bits to be controlled. Any sequential circuit in the 9300 MSI family can be used in this configuration.

SWITCHING PERFORMANCE

PROPAGATION DELAY ENABLE INPUT TO OUTPUT VERSUS TEMPERATURE



PROPAGATION DELAY DATA INPUT TO OUTPUT VERSUS TEMPERATURE



SPECIAL ORDERING CODE

Temperature Range:
−55° C to +125° C, add -1 to MIC number.
0° C to +75° C, add -5 to MIC number.

Case Style:
½" x ⅜" Flat Pack, add "B" following last digit.
Ceramic Dual In-Line, 24 leads, add "D" following last digit.

Example:
MIC9311-1D is −55°C to +125°C. Temperature range in Ceramic Dual-In-Line, 24 lead package.
Flat-pack and Dual-In-Line packages have same pin configuration.

MSI EIGHT-INPUT MULTIPLEXER

- **Multifunction Capability**
- **25 ns Through Delay**
- **On-Chip Select Logic Decoding**
- **Fully Buffered Complementary Outputs**
- **The Input/Output Characteristics Provide Easy Interfacing with DTL930, TTL9000, TTL7400 and MSI Families**
- **Input Clamp Diodes Limit High Speed Termination Effects**

The MIC9312 is a monolithic, high speed, eight input digital multiplexer circuit. It provides in one package the ability to select one bit of data from up to eight sources. The MIC9312 can be used as a universal function generator to generate any logic function of four variables. Both assertion and negation outputs are provided. TTL circuitry with active pullups on the outputs provides high speed, high fanout operation and is compatible with all DTL and TTL digital integrated circuits.

ABSOLUTE MAXIMUM RATINGS
(above which the useful life may be impaired)

CHARACTERISTICS		UNITS
Storage Temperature	−65°C to +150	°C
Temperature (Ambient) Under Bias	−55°C to +125	°C
V_{CC} Pin Potential to Ground Pin	−0.5 V to +7	Volts
Voltage applied to Output when output is high	0 V to +V_{CC}	value
Input Voltage (DC) (See Note 1)	−0.5 V to +5.5	Volts
Input Current (DC) (See Note 1)	−30 mA to +5	mA
Current into Output when output is low	+30	mA

Note 1: Either Input Voltage limit or Input Current limit is sufficient to protect the inputs.

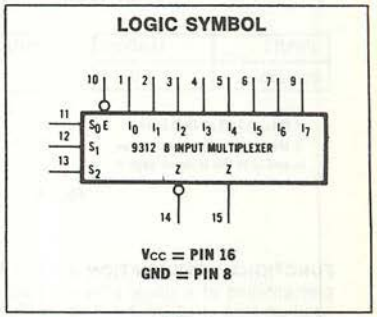


Fig. 1

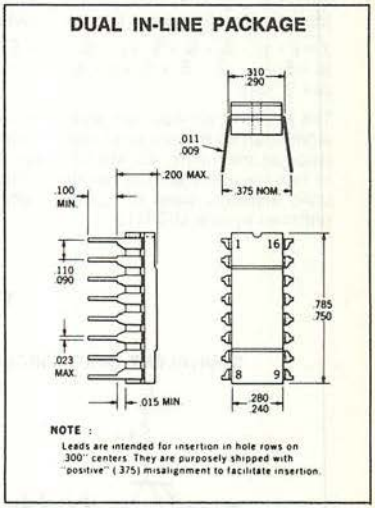


Fig. 2

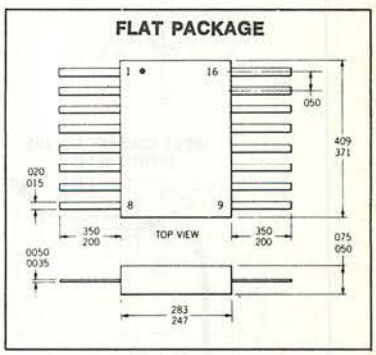


Fig. 3

LOADING RULES

INPUTS	LOADING
All Inputs	1 U.L.

OUTPUTS	FAN-OUT	
	High State	Low State
$\overline{Z}$	18	9
Z	20	10

1 U.L. = 1 TTμL Unit Load
1 U.L. is defined by the entries I_R and I_F in the table on page 3.

Fig. 4

FUNCTIONAL DESCRIPTION — The MIC9312 is a logical implementation of a single pole - 8 position switch with the switch position controlled by the state of three select inputs, S_0, S_1, S_2. Both assertion and negation outputs are provided. The enable input (E) is active low. When it is not activated the negation output is high and the assertion output is low regardless of all other inputs. The logic function provided at the output is:

$Z = E \cdot (I_0 \cdot \overline{S}_0 \cdot \overline{S}_1 \cdot \overline{S}_2 + I_1 \cdot S_0 \cdot \overline{S}_1 \cdot \overline{S}_2 + I_2 \cdot \overline{S}_0 \cdot S_1 \cdot \overline{S}_2 + I_3 \cdot S_0 \cdot S_1 \cdot \overline{S}_2 + I_4 \cdot \overline{S}_0 \cdot \overline{S}_1 \cdot S_2 + I_5 \cdot S_0 \cdot \overline{S}_1 \cdot S_2 + I_6 \cdot \overline{S}_0 \cdot S_1 \cdot S_2 + I_7 \cdot S_0 \cdot S_1 \cdot S_2)$.

The MIC9312 provides the ability, in one package, to select from eight sources of data or control information. By proper manipulation of the inputs, the MIC9312 can provide any logic function of four variables and its negation. Thus any number of random topic elements used to generate unusual truth tables can be replaced by one MIC9312.

TRUTH TABLE

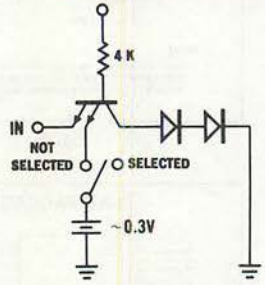
E	S_2	S_1	S_0	I_0	I_1	I_2	I_3	I_4	I_5	I_6	I_7	$\overline{Z}$	Z
H	X	X	X	X	X	X	X	X	X	X	X	H	L
L	L	L	L	L	X	X	X	X	X	X	X	H	L
L	L	L	L	H	X	X	X	X	X	X	X	L	H
L	L	L	H	X	L	X	X	X	X	X	X	H	L
L	L	L	H	X	H	X	X	X	X	X	X	L	H
L	L	H	L	X	X	L	X	X	X	X	X	H	L
L	L	H	L	X	X	H	X	X	X	X	X	L	H
L	L	H	H	X	X	X	L	X	X	X	X	H	L
L	L	H	H	X	X	X	H	X	X	X	X	L	H
L	H	L	L	X	X	X	X	L	X	X	X	H	L
L	H	L	L	X	X	X	X	H	X	X	X	L	H
L	H	L	H	X	X	X	X	X	L	X	X	H	L
L	H	L	H	X	X	X	X	X	H	X	X	L	H
L	H	H	L	X	X	X	X	X	X	L	X	H	L
L	H	H	L	X	X	X	X	X	X	H	X	L	H
L	H	H	H	X	X	X	X	X	X	X	L	H	L
L	H	H	H	X	X	X	X	X	X	X	H	L	H

H = High voltage level
L = Low voltage level
X = Level does not affect output

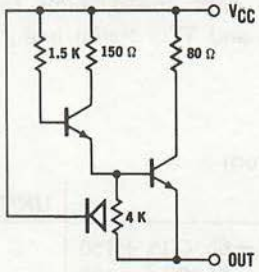
Fig. 5

TYPICAL INPUT AND OUTPUT CHARACTERISTICS

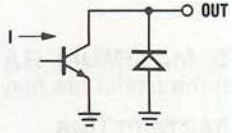
EQUIVALENT INPUT CIRCUIT



OUTPUT HIGH EQUIVALENT CIRCUIT



OUTPUT LOW EQUIVALENT CIRCUIT



INPUT CURRENT VERSUS INPUT VOLTAGE

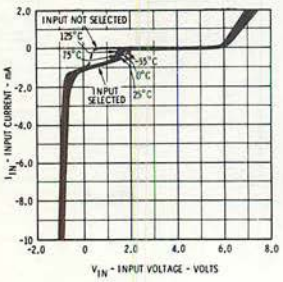


Fig. 6

OUTPUT CURRENT VERSUS OUTPUT VOLTAGE (OUTPUT HIGH)

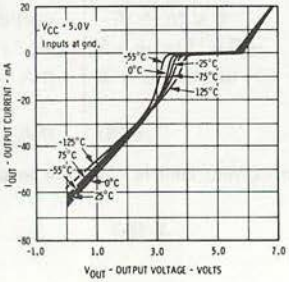


Fig. 7

OUTPUT CURRENT VERSUS OUTPUT VOLTAGE (OUTPUT LOW)

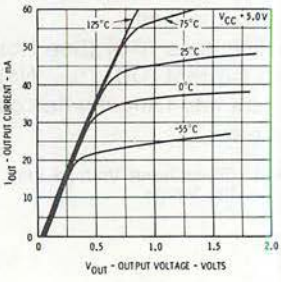


Fig. 8

ELECTRICAL CHARACTERISTICS* (MIC9312-1X) ($T_A = -55°C$ to $+125°C$, $V_{CC} = 5.0\ V \pm 10\%$)

SYMBOL	CHARACTERISTICS	LIMITS						UNITS	CONDITIONS
		−55°C		+25°C		+125°C			
		MIN.	MAX.	MIN.	TYP. MAX.	MIN.	MAX.		
V_{OH}	Output High Voltage	2.4		2.4	2.7	2.4		Volts	$V_{CC} = 4.5\ V$ $I_{OH} = -1.2$ mA (Pin 15) $V_{CC} = 4.5\ V$ $I_{OH} = -1.08$ mA (Pin 14) Inputs at threshold voltages (V_{IL} or V_{IH}) as per truth table
V_{OL}	Output Low Voltage		0.4		0.21 0.4		.04	Volts	$V_{CC} = 5.5\ V$ $I_{OL} = 16.0$ mA (Pin 15) $I_{OL} = 14.4$ mA (Pin 14) $V_{CC} = 4.5\ V$ $I_{OL} = 12.4$ mA (Pin 15) $I_{OL} = 11.2$ mA (Pin 14) Inputs at threshold voltages (V_{IL} or V_{IH}) as per truth table
V_{IH}	Input High Voltage	2.0		1.7		1.4		Volts	Guaranteed input high threshold for all inputs
V_{IL}	Input Low Voltage		0.8		0.9		0.8	Volts	Guaranteed input low threshold for all inputs
I_F (all inputs)	Input Load Current		−1.6 −1.24		−1.1 −1.6 −0.85 −1.24		−1.6 −1.24	mA mA	$V_{CC} = 5.5\ V$ $V_F = 0.4\ V$ $V_{CC} = 4.5\ V$ Input Selected
I_R (all inputs)	Input Leakage Current				15 60		60	μA	$V_{CC} = 5.5\ V$ $V_R = 4.5\ V$ Input not selected
I_{PDH}	V_{CC} Current		40		27 40		40	mA	$V_{CC} = 5.0\ V$
t_{pd+} (S_0 to Z)	Switching Speed				23 34			ns	$V_{CC} = 5.0\ V$, See Page 4
t_{pd-} (S_0 to Z)	Switching Speed				25 36			ns	$C_L = 15$ pF

*Pulse tested

ELECTRICAL CHARACTERISTICS* (MIC9312-5X) ($T_A = 0°C$ to $+75°C$, $V_{CC} = 5.0\ V \pm 5\%$)

SYMBOL	CHARACTERISTICS	LIMITS						UNITS	CONDITIONS
		0°C		+25°C		+75°C			
		MIN.	MAX.	MIN.	TYP. MAX.	MIN.	MAX.		
V_{OH}	Output High Voltage	2.4		2.4	3.0	2.4		Volts	$V_{CC} = 4.75\ V$ $I_{OH} = -1.2$ mA (Pin 15) $V_{CC} = 4.75\ V$ $I_{OH} = -1.08$ mA (Pin 14) Inputs at threshold voltages (V_{IL} or V_{IH}) as per truth table
V_{OL}	Output Low Voltage		0.45		0.21 0.45		0.45	Volts	$V_{CC} = 5.25\ V$ $I_{OL} = 16.0$ mA (Pin 15) $I_{OL} = 14.4$ mA (Pin 14) $V_{CC} = 4.75\ V$ $I_{OL} = 14.1$ mA (Pin 15) $I_{OL} = 12.7$ mA (Pin 14) Inputs at threshold voltages (V_{IL} or V_{IH}) as per truth table
V_{IH}	Input High Voltage	1.9		1.8		1.6		Volts	Guaranteed input high threshold for all inputs
V_{IL}	Input Low Voltage		0.85		0.85		0.85	Volts	Guaranteed input low threshold for all inputs
I_F (all inputs)	Input Load Current		−1.6 −1.41		−1.0 −1.6 −0.91 −1.41		−1.6 −1.41	mA mA	$V_{CC} = 5.25\ V$ $V_F = 0.45\ V$ $V_{CC} = 4.75\ V$ Input Selected
I_R (all inputs)	Input Leakage Current				15 60		60	μA	$V_{CC} = 5.25\ V$ $V_R = 4.5\ V$ Input not selected
I_{PDH}	V_{CC} Current		43		27 43		43	mA	$V_{CC} = 5.0\ V$
t_{pd+} (S_0 to Z)	Switching Speed				23 34			ns	$V_{CC} = 5.0\ V$, See Page 4
t_{pd-} (S_0 to Z)	Switching Speed				25 36			ns	$C_L = 15$ pF

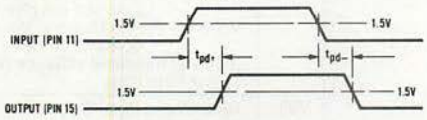
*Pulse tested

A.C. CHARACTERISTICS

A.C. CHARACTERISTICS

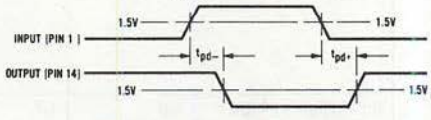
All measurements are made with $V_{CC} = 5.0$ V applied to pin 16 and with pin 8 grounded. The active input is driven by a MIC9002 TTL gate with the output loaded with 15 pF. Both outputs of the MIC9312 are loaded with 15 pF.

t_{pd}: S_0 to Z



Other Conditions: Pins 1, 8, 10, 12, 13 = Gnd
Pin 2 = V_{CC} through 1.0 kΩ
Pin 16 = V_{CC}

t_{pd}: I_0 to $\overline{Z}$



Other Conditions: Pins 8, 10, 11, 12, 13 = Gnd
Pin 16 = V_{CC}

TURN OFF DELAY VERSUS AMBIENT TEMPERATURE; S_0 to Z

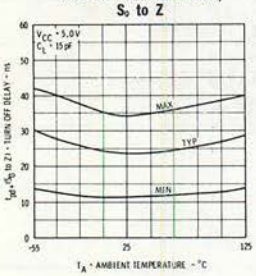


Fig. 9

TURN ON DELAY VERSUS AMBIENT TEMPERATURE; S_0 to Z

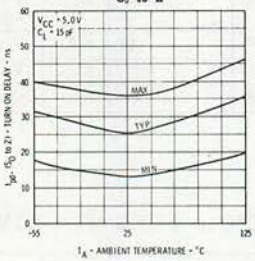


Fig. 10

TURN OFF DELAY VERSUS AMBIENT TEMPERATURE; I_0 to $\overline{Z}$

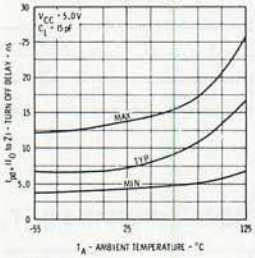


Fig. 11

TURN ON DELAY VERSUS AMBIENT TEMPERATURE; I_0 to $\overline{Z}$

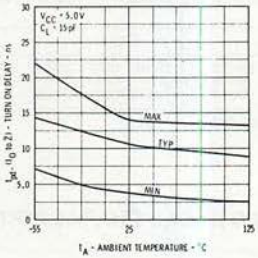
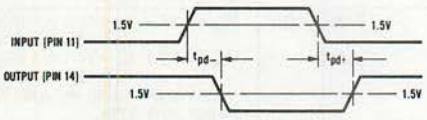


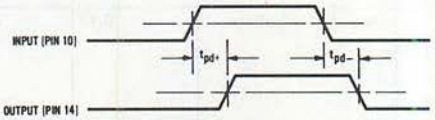
Fig. 12

t_{pd}: S_0 to $\overline{Z}$



Other Conditions: Pins 1, 8, 10, 12, 13 = Gnd
Pin 2 = V_{CC} through 1.0 kΩ
Pin 16 = V_{CC}

t_{pd}: E to $\overline{Z}$



Other Conditions: Pins 8, 11, 12, 13 = Gnd
Pin 1 = V_{CC} through 2.0 kΩ
Pin 16 = V_{CC}

TURN OFF DELAY VERSUS AMBIENT TEMPERATURE; S_0 to $\overline{Z}$

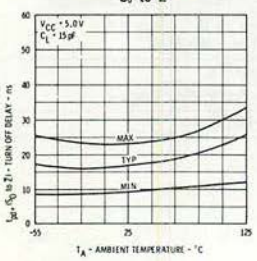


Fig. 13

TURN ON DELAY VERSUS AMBIENT TEMPERATURE; S_0 to $\overline{Z}$

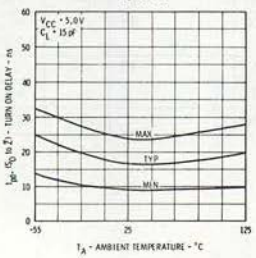


Fig. 14

TURN OFF DELAY VERSUS AMBIENT TEMPERATURE; E to Z

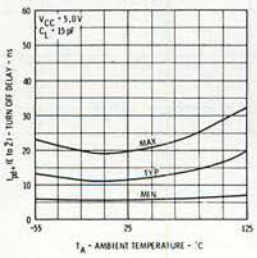


Fig. 15

TURN ON DELAY VERSUS AMBIENT TEMPERATURE; E to Z

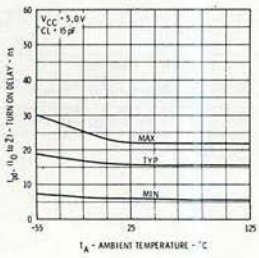


Fig. 16

APPLICATIONS

A MULTI-PORT MEMORY MODULE

The four bit by eight word multi-port memory module shown in the diagram below uses only thirteen MSI packages; four MIC9308 24 pin dual four bit latches, eight MIC9312 eight input multiplexers, and one MIC9301 one-out-of-ten decoder.

The module as shown is capable of simultaneously reading from two independently specified locations and writing into a third independently selected location. The necessary enables are provided so that a number of these modules may be connected together to produce a larger memory. As an example a sixteen bit by sixty-four word memory would require thirty-two of the modules shown below.

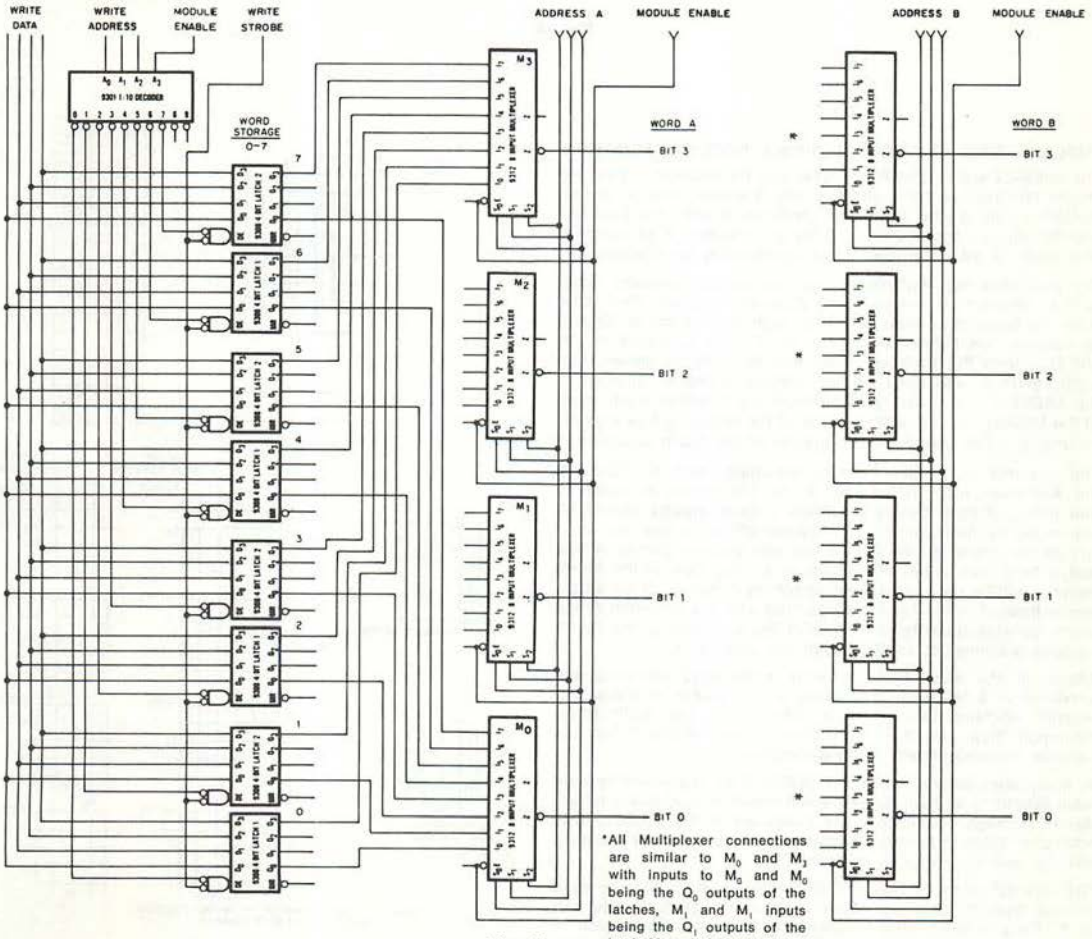
By connecting this type of memory to a function generator unit, a processor could be constructed that would execute three address instructions at a very high speed on the data contained in this type of memory. In order to utilize the speed of the memory the instructions would also have to be contained in fast semiconductor memory.

SPECIAL ORDERING CODE

Temperature Range:
−55°C to +125°C, add -1 to MIC number.
0°C to +75°C, add -5 to MIC number.

Case Style:
¼" x ⅜" Flat Pack, add "B" following last digit.
Ceramic Dual In-Line, 16 leads, add "D" following last digit.

Example:
MIC9312-1D is −55°C to +125°C. Temperature range in Ceramic Dual-In-Line, 16 lead package.
Flat-pack and Dual-In-Line packages have same pin configuration.



*All Multiplexer connections are similar to M_0 and M_3 with inputs to M_0 and M_0 being the Q_0 outputs of the latches, M_1 and M_1 inputs being the Q_1 outputs of the latch, M_2 and M_2 inputs being Q_0 outputs of the latch, etc.

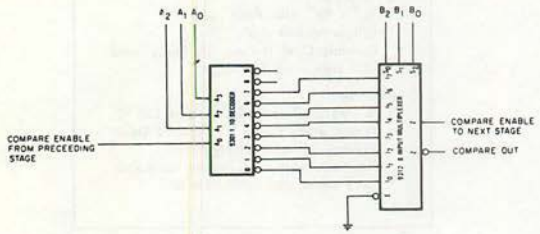
Fig. 17

APPLICATIONS

3 BIT COMPARATOR

Three bits of data to be compared are supplied to the address and select inputs of the MIC9301 and MIC9312 respectively. If A_0, A_1, A_2, and B_0, B_1, B_2 compare, the mutually exclusive active low output of the MIC9301 1/10 decoder and the selected input of the MIC9312 multiplexer will be coincidental and COMPARE OUT will be high. . The COMPARE ENABLE must be low to permit compare operation.

3 BIT COMPARATOR



INTERCONNECTION DIAGRAM FOR 9 BITS

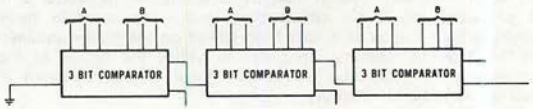


Fig. 18

IMPLEMENTING ANY FOUR-VARIABLE BOOLEAN FUNCTION

The MIC9312 eight input multiplexer can (in addition to performing its nominal function) produce any Boolean function of four variables without any additional elements if both the assertion and negation of one of the variables are present. If an assertion and negation are not present, one inverter may be required.

The procedure for implementing a four-variable function, along with an example, is shown in the attached diagram. First, consider the function in terms of a Karnaugh map. If the Q_0, Q_1 and Q_2 variable are connected to the S_0, S_1 and S_2 inputs of the MIC9312 then the Karnaugh map will be split, as shown, into eight sections, with each section corresponding to an input to the MIC9312. In order to implement the function each input of the MIC9312 is connected to one of the following four signals: ground, V_{CC}, the assertion, or negation of the fourth variable.

The contents of the two squares associated with an input, on the Karnaugh map, determine which connection is made to that input. If both squares contain a zero, ground should be connected to the input; if both squares contain a one, the input should be connected to V_{CC}. If the two squares contain a one and a zero then either the assertion or negation of the fourth variable will be required to implement the function. If the single one is located in the square associated with the assertion of the fourth variable then the assertion of the assertion of the fourth variable is connected to that input, and vice versa.

Shown in the illustration below is a MIC9312 decoding the condition of a MIC9300, producing a one output whenever the register contains two or more transitions. The truth table, Karnaugh map and the connection to the MIC9312 for this function are also shown in the illustration.

In many applications, using the MIC9312 to implement general logic functions of four variables will result in a sizeable reduction in package count. In many cases use of the MIC9312 with additional gates to produce functions of more than four variables will also reduce the package count.

The concept of using the MIC9312 eight input-multiplexer as a general logic function generator is described by S. S. Yau and C. K. Tang of Northwestern University in a paper presented at the 1968 Spring Joint Computer Conference in Atlantic City, New Jersey.

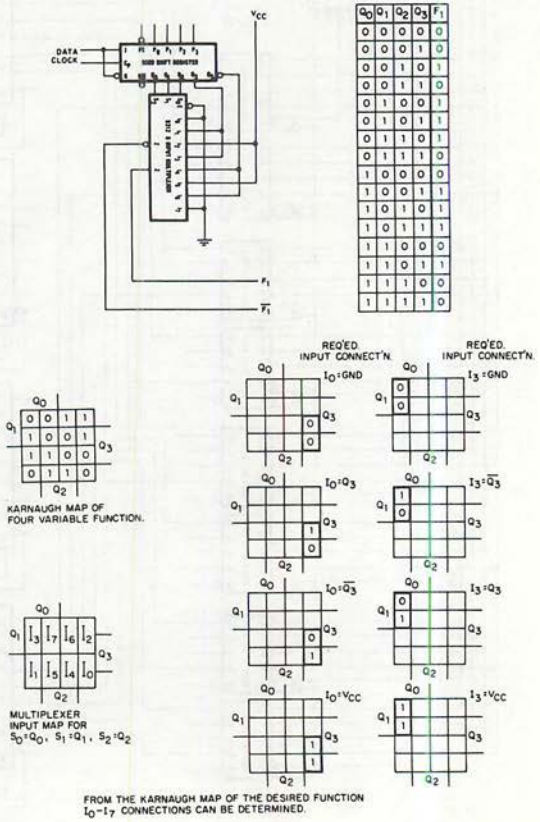


Fig. 19

MSI 4-BIT BINARY COUNTER

The MIC9316 is a high speed synchronous 4-bit binary decade counter. It is a synchronously presettable, multifunctional MSI building block useful in a large number of counting, digital integration, and conversion applications. Several stages of synchronous operation are obtainable with no external gating packages required through an internal carry look-ahead counting technique.

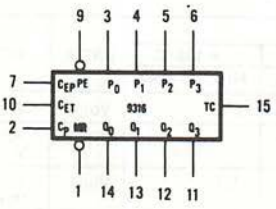
- **Synchronous Counting and Parallel Entry**
- **Decoded Terminal Count**
- **Built-In Carry Circuitry**
- **Typical Power Dissipation of 300 mW**
- **The Input/Output Characteristics Provide Easy Interfacing with DTL930, TTL9000, TTL7400 and MSI Families**
- **All Ceramic Hermetic 16 Pin Dual In-Line Package and Flat Package**
- **Input Diode Clamps Limit High Speed Line Termination Effects**

ABSOLUTE MAXIMUM RATINGS

(above which the useful life may be impaired)

CHARACTERISTICS		UNITS
Storage Temperature	−65°C to +150	°C
Temperature (Ambient) Under Bias	−55°C to +125	°C
V_{CC} Pin Potential to Ground Pin	−0.5 V to +7	Volts
Voltage Applied to Outputs for high output state	−0.5 V to V_{CC}	value
Input Voltage (D.C.)	−0.5 V to +5.5	Volts

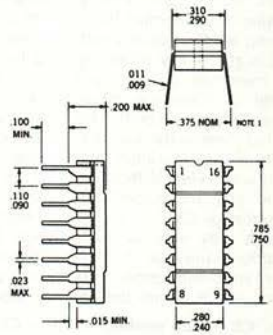
LOGIC DIAGRAM



V_{CC} = Pin 16
Gnd = Pin 8

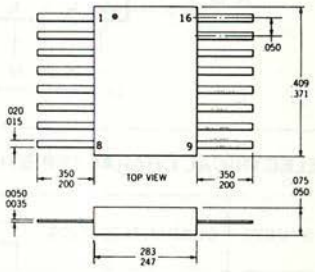
PHYSICAL DIMENSIONS

DUAL IN-LINE PACKAGE



NOTE:
1. Leads are intended for insertion in hole rows on .300" centers. They are purposely shipped with "positive" (.375) misalignment to facilitate insertion.

FLAT PACKAGE



FUNCTIONAL DESCRIPTION — A clock buffer and inverter drives the four clocked RS master-slave flip flops in parallel, so that synchronous operation is obtained. When the clock input (CP) is low, the slave is steady, but data can enter the master via the R and the S inputs. During the low to high transition of CP, first the data inputs (R and S) are inhibited, so that a later change in the input data will not affect the master; secondly, the now trapped information in the master is transferred to the slave and is reflected at the outputs. When the transfer is completed both the master and the slave are steady as long as the clock input remains high, and regardless of the logic state at any other input to the device. During the high to low transition of the clock input, first the transfer path from master to slave are inhibited, leaving the slave steady in its present state, secondly, the data inputs (R and S) are enabled so that new data can enter the master. As a result of this synchronous operation higher clock frequency is possible and much less external logic is required in most applications. Some restrictions are placed on the manner of selection. First, the transition of CEP or CET from high to low or of $\overline{PE}$ from low to high may only be done when CP is high. The remaining transitions may be made by following the setup and release times specified under "Switching Characteristics." The asynchronous $\overline{MR}$ clears the counter independent of any other input.

Note: CE (count enable) = CEP · CET
TC = CET · Q_0 · Q_1 · Q_2 · Q_3

SPECIAL ORDERING CODE

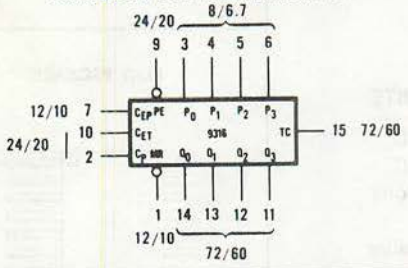
Temperature Range:
−55°C to +125°C, add -1 to MIC number.
0°C to +75°C, add -5 to MIC number.

Case Style:
¼" x ⅜" Flat Pack, add "B" following last digit.
Ceramic Dual In-Line, 16 leads, add "D" following last digit.

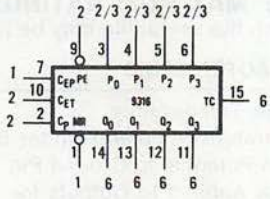
Example:
MIC9316-1D is −55°C to +125°C. Temperature range in Ceramic Dual-In-Line, 16 lead package.
Flat-pack and Dual-In-Line packages have same pin configuration.

LOADING RULES

CCSL LOAD AND DRIVE FACTORS



TTL LOAD AND DRIVE FACTORS



ELECTRICAL CHARACTERISTICS (MIC9316-1X) (T_A = −55°C to +125°C, V_{CC} = 5.0 V ±10%)

SYMBOL	CHARACTERISTICS	LIMITS −55°C MIN.	LIMITS −55°C MAX.	LIMITS +25°C MIN.	LIMITS +25°C TYP.	LIMITS +25°C MAX.	LIMITS +125°C MIN.	LIMITS +125°C MAX.	UNITS	CONDITIONS & COMMENTS
V_{OH}	Output High Voltage	2.4		2.4	2.7		2.4		Volts	V_{CC} = 4.5 V, I_{OH} = −0.36 mA
V_{OL}	Output Low Voltage		0.4		0.2	0.4		0.4	Volts	V_{CC} = 5.5 V, I_{OL} = 9.6 mA V_{CC} = 4.5 V, I_{OL} = 7.44 mA
V_{IH}	Input High Voltage	2.0		1.7			1.4		Volts	Guaranteed input high threshold for all inputs
V_{IL}	Input Low Voltage		0.8			0.9		0.8	Volts	Guaranteed input low threshold for all inputs
I_F	Input Load Current $\overline{MR}$, CEP		−1.6		−1.0	−1.6		−1.6	mA	
2 I_F	Input Load Current CP, $\overline{PE}$, CET		−3.2		−2.0	−3.2		−3.2	mA	V_{CC} = 5.5 V V_F = 0.4 V
⅔ I_F	Input Load Current P_0, P_1, P_2, P_3		−1.07		−0.7	−1.07		−1.07	mA	
I_R	Input Leakage Current $\overline{MR}$, CEP		60		10	60		60	μA	
2 I_R	Input Leakage Current CP, $\overline{PE}$, CET		120		20	120		120	μA	V_{CC} = 5.5 V V_R = 4.5 V
⅔ I_R	Input Leakage Current P_0, P_1, P_2, P_3		40		7.0	40		40	μA	

ELECTRICAL CHARACTERISTICS (MIC9316-5X) ($T_A = 0°C$ to $+75°C$, $V_{CC} = 5.0\ V \pm 5\%$)

SYMBOL	CHARACTERISTICS	LIMITS						UNITS	CONDITIONS & COMMENTS
		0°C		+25°C			+75°C		
		MIN.	MAX.	MIN.	TYP.	MAX.	MIN.	MAX.	
V_{OH}	Output High Voltage	2.4		2.4	3.0		2.4		Volts	$V_{CC} = 4.75\ V$, $I_{OH} = -0.36\ mA$
V_{OL}	Output Low Voltage		0.45		0.2	0.45		0.45	Volts	$V_{CC} = 5.25\ V$, $I_{OL} = 9.6\ mA$ $V_{CC} = 4.75\ V$, $I_{OL} = 8.5\ mA$
V_{IH}	Input High Voltage	1.9		1.8			1.6		Volts	Guaranteed input high threshold for all inputs
V_{IL}	Input Low Voltage		0.85			0.85		0.85	Volts	Guaranteed input low threshold for all inputs
I_F	Input Load Current $\overline{MR}$, CEP		−1.6		−1.0	−1.6		−1.6	mA	
$2\ I_F$	Input Load Current CP, $\overline{PE}$, CET		−3.2		−2.0	−3.2		−3.2	mA	$V_{CC} = 5.25\ V$ $V_F = 0.4\ V$
$⅔\ I_F$	Input Load Current P_0, P_1, P_2, P_3		−1.07		−0.7	−1.07		−1.07	mA	
I_R	Input Leakage Current $\overline{MR}$, CEP		60		10	60		60	μA	
$2\ I_R$	Input Leakage Current CP, $\overline{PE}$, CET		120		20	120		120	μA	$V_{CC} = 5.25\ V$ $V_R = 4.5\ V$
$⅔\ I_R$	Input Leakage Current P_0, P_1, P_2, P_3		40		7.0	40		40	μA	

SWITCHING CHARACTERISTICS ($T_A = 25°C$)

SYMBOL	CHARACTERISTICS	MIN.	TYP.	MAX.	UNITS	CONDITIONS & COMMENTS
t_{pd+} (Q)	Turn-Off Delay		20		ns	$V_{CC} = 5.0\ V$ $C_L = 15\ pF$ (Fig. 1)
t_{pd-} (Q)	Turn-On Delay		15		ns	
t_{pd+} (TC)	Turn-Off Delay for TC		35		ns	
t_{pd-} (TC)	Turn-On Delay for TC		20		ns	
t_s(CE)	Set-Up Time for CE		14		ns	$V_{CC} = 5.0\ V$
t_r (CE)	Release Time for CE		12		ns	$C_L = 15\ pF$ (Fig. 2)
t_s	Set-Up Time for Data		18		ns	$V_{CC} = 5.0\ V$ $C_L = 15\ pF$ (Fig. 3)
t_r	Release Time for Data		17		ns	
t_s ($\overline{PE}$)	Set-Up Time for $\overline{PE}$		30		ns	
t_r ($\overline{PE}$)	Release Time for $\overline{PE}$		28		ns	
t_{pd-} ($\overline{MR}$)	Turn-On Delay for $\overline{MR}$		33		ns	$V_{CC} = 5.0\ V$, $C_L = 15\ pF$ (Fig. 4)
t_{p+}	Propagation Delay for CET to TC		14		ns	$V_{CC} = 5.0\ V$, $C_L = 15\ pF$ (Fig. 5)

SET-UP TIME: t_s is defined as the minimum time required for the logic level to be present at the logic input prior to the clock transition from low to high in order for the flip-flop(s) to respond.

RELEASE TIME: t_r is defined as the maximum time allowed for the logic level to be present at the logic input prior to the clock transition from low to high in order for the flip-flop(s) not to respond.

SWITCHING TIME WAVEFORMS

Fig. 1

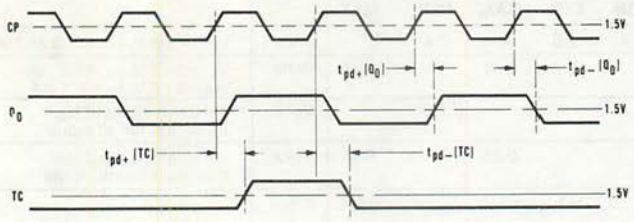


Fig. 2

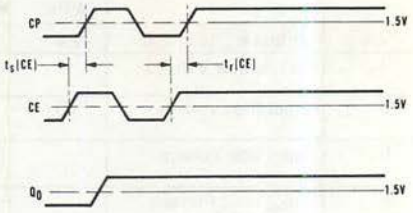


Fig. 3

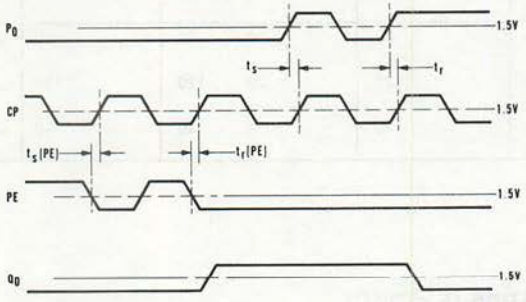


Fig. 4

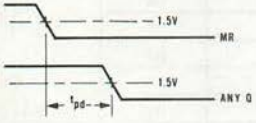
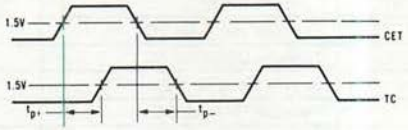
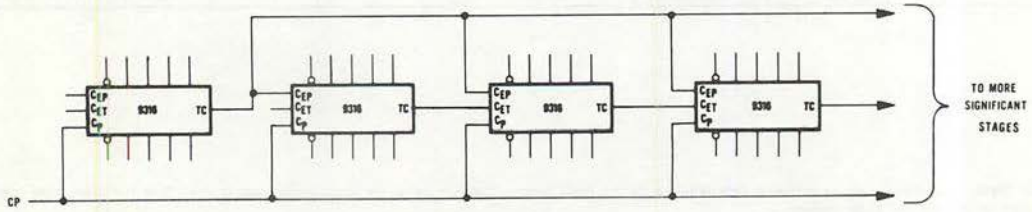


Fig. 5



APPLICATIONS



SYNCHRONOUS COUNTING SCHEME

MSI QUAD TWO-INPUT MULTIPLEXER

- **Multifunction Capability**
- **20 ns Through Delay**
- **On-Chip Select Logic Decoding**
- **Fully Buffered Outputs**
- **The Input/Output Characteristics Provide Easy Interfacing with ITT DTL 930, ITT TTL9000, MSI and other DTL and TTL Families.**
- **Input Clamp Diodes Limit High Speed Termination Effects.**

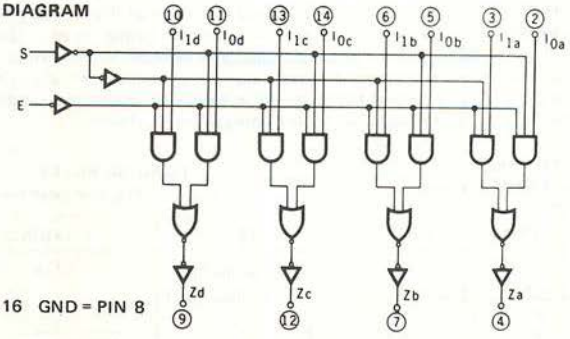
The ITT9322 is a monolithic, high speed, quad two-input digital multiplexer circuit, constructed with the ITT epitaxial process. It consists of four multiplexing circuits with common select and enable logic, each circuit contains two inputs and one output. The circuit uses TTL for high speed, high fanout operation and is compatible with all other members of the DTL and TTL family of digital integrated circuits.

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

CHARACTERISTICS		UNITS
Storage Temperature	−65°C to +150	°C
Temperature (Ambient) Under Bias	−55°C to +125	°C
V_{CC} Pin Potential to Ground Pin	0.5 V to +7.0	V
Voltage Applied to Output when output is high	0 V to +V_{CC}	value
Input Voltage (DC) (See Note 1)	−0.5 V to +5.5	V
Input Current (DC) (See Note 1)	−30 mA to +5	mA
Current into Output when output is low	+30	mA

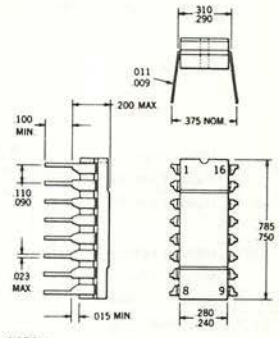
Note 1 – either Input Voltage limit or Input Current limit is sufficient to protect the inputs.

LOGIC DIAGRAM



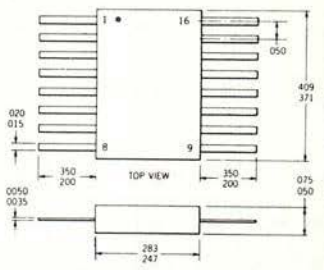
V_{CC} = PIN 16 GND = PIN 8

DUAL IN-LINE PACKAGE



NOTE :
Leads are intended for insertion in hole rows on .300" centers. They are purposely shipped with "positive" (.375) misalignment to facilitate insertion.

FLAT PACKAGE



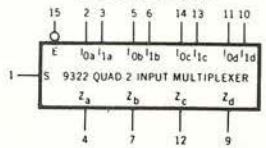
SPECIAL ORDERING CODE

Temperature Range:
1 = −55° + 125°C
5 = 0° to +75C

Package:
B = Flat Pack
D = Dual In-Line, 16 leads

Example:
MIC9322 - 1B means operating temperature range of −55° to +125°C, supplied in a Flat Pack

LOGIC SYMBOL



V_{CC} = PIN 16 GND = PIN 8

ELECTRICAL CHARACTERISTICS* (T_A = –55°C to +125°C, V_{CC} = 5.0 V ± 10%)

SYMBOL	CHARACTERISTICS	LIMITS –55°C MIN.	LIMITS –55°C MAX.	LIMITS +25°C MIN.	LIMITS +25°C TYP.	LIMITS +25°C MAX.	LIMITS +125°C MIN.	LIMITS +125°C MAX.	UNITS	CONDITIONS
V_{OH}	Output High Voltage	2.4		2.4	2.7		2.4		Volts	V_{CC} = 4.5 V I_{OH} = –1.2 mA Inputs at threshold voltages (V_{IL} or V_{IH}) as per truth table
V_{OL}	Output Low Voltage		0.4		0.21	0.4		0.4	Volts	V_{CC} = 5.5 V I_{OL} = 16.0 mA V_{CC} = 4.5 V I_{OL} = 12.4 mA Inputs at threshold voltages (V_{IL} or V_{IH}) as per truth table
V_{IH}	Input High Voltage	2.0		1.7			1.4		Volts	Guaranteed input high threshold for all inputs
V_{IL}	Input Low Voltage		0.8			0.9		0.8	Volts	Guaranteed input low threshold for all inputs
I_F (all inputs)	Input Load Current		–1.6		–1.1	–1.6		–1.6	mA	V_{CC} = 5.5 V, V_F = 0.4 V
			–1.24		–0.85	–1.24		–1.24	mA	V_{CC} = 4.5 V, Input selected
I_R (all inputs)	Input Leakage Current				8.0	60		60	µA	V_{CC} = 5.5 V, V_R = 4.5 V
I_{PDH}	V_{CC} Current		43		30	43		43	mA	V_{CC} = 5.0 V, All inputs high
t_{pd+} (S to Z_a)	Switching Speed				17	25			ns	V_{CC} = 5.0 V, C_L = 15 pF, See Figure (A)
t_{pd-} (S to Z_a)	Switching Speed				20	27			ns	

*Pulse Tested

ELECTRICAL CHARACTERISTICS* (T_A = 0°C to +75°C, V_{CC} = 5.0 V ± 5%)

SYMBOL	CHARACTERISTICS	LIMITS 0°C MIN.	LIMITS 0°C MAX.	LIMITS +25°C MIN.	LIMITS +25°C TYP.	LIMITS +25°C MAX.	LIMITS +125°C MIN.	LIMITS +125°C MAX.	UNITS	CONDITIONS
V_{OH}	Output High Voltage	2.4		2.4	3.0		2.4		Volts	V_{CC} = 4.75 V I_{OH} = –1.2 mA Inputs at threshold voltages (V_{IL} or V_{IH}) as per truth table
V_{OL}	Output Low Voltage		0.45		0.21	0.45		0.45	Volts	V_{CC} = 5.25 V I_{OL} = 16.0 mA V_{CC} = 4.75 V I_{OL} = 14.1 mA Inputs at threshold voltages (V_{IL} or V_{IH}) as per truth table
V_{IH}	Input High Voltage	1.9		1.8			1.6		Volts	Guaranteed input high threshold for all inputs
V_{IL}	Input Low Voltage		0.85			0.85		0.85	Volts	Guaranteed input low threshold for all inputs
I_F (all inputs)	Input Load Current		–1.6		–1.0	–1.6		–1.6	mA	V_{CC} = 5.25 V, V_F = 0.45 V
			–1.41		–0.91	–1.41		–1.41	mA	V_{CC} = 4.75 V, Input selected
I_R (all inputs)	Input Leakage Current				8.0	60		60	µA	V_{CC} = 5.25 V, V_R = 4.5 V
I_{PDH}	V_{CC} Current		45		30	45		45	mA	V_{CC} = 5.0 V, All inputs high
t_{pd+} (S to Z_a)	Switching Speed				17	30			ns	V_{CC} = 5.0 V, C_L = 15 pF, See Figure (A)
t_{pd-} (S to Z_a)	Switching Speed				20	31			ns	

*Pulse Tested

FUNCTIONAL DESCRIPTION — The MIC9322 quad two input multiplexer is a member of the ITT family of compatible Medium Scale Integrated (MSI) digital building blocks. It provides this family with the ability to select four bits of either data or control from two sources, in one package. The enable input ($\overline{E}$) is active low. When not activated all outputs (Z) are low regardless of all other inputs.

The MIC9322 quad two input multiplexer is the logical implementation of a four-pole two-position switch, with the position of the switch being set by the logic levels supplied to the one select input. The logic equations for the outputs are shown below:

$$Z_a = E \cdot (I_{1a} \cdot S + I_{0a} \cdot \overline{S}) \qquad Z_b = E \cdot (I_{1b} \cdot S + I_{0b} \cdot \overline{S})$$

$$Z_c = E \cdot (I_{1c} \cdot S + I_{0c} \cdot \overline{S}) \qquad Z_d = E \cdot (I_{1d} \cdot S + I_{0d} \cdot \overline{S})$$

A common use of the MIC9322 would be the moving of data from a group of registers to four common output busses. The particular register from which the data came would be determined by the state of the select input. A less obvious use is a function generator. The MIC9322 can generate four functions of two variables with one variable common. This is useful for implementing gating functions.

TRUTH TABLE
Identical for Each Multiplexer

ENABLE	SELECT INPUT	INPUTS		OUTPUT
$\overline{E}$	S	I_{0X}	I_{1X}	Z_X
H	X	X	X	L
L	H	X	L	L
L	H	X	H	H
L	L	L	X	L
L	L	H	X	H

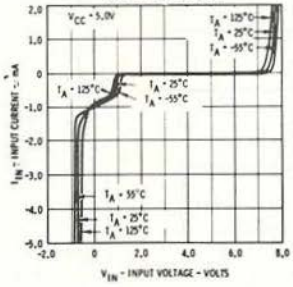
L = low voltage level
H = high voltage level
X = either high or low logic level

LOADING RULES
(1 U.L. = 1 TTL gate input load)

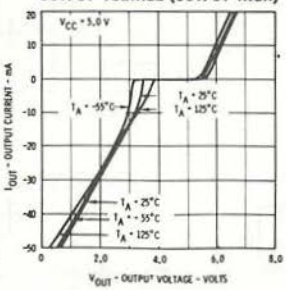
INPUTS	LOADING	
$I_{0a}, I_{1a}, I_{0b}, I_{1b}, I_{0c}, I_{1c}, I_{0d}, I_{1d}$ S, E	1 U.L.	
OUTPUTS	FANOUT AT LOGIC LEVEL	
	HIGH	LOW
Z_a, Z_b, Z_c, Z_d	20 U.L.	10 U.L.

TYPICAL INPUT AND OUTPUT CHARACTERISTICS

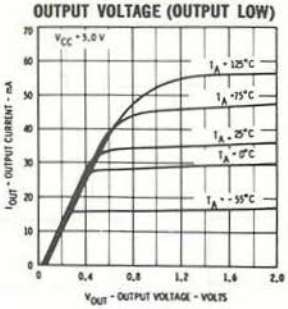
INPUT CURRENT VERSUS INPUT VOLTAGE



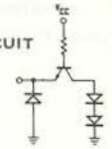
OUTPUT CURRENT VERSUS OUTPUT VOLTAGE (OUTPUT HIGH)



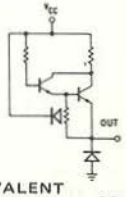
OUTPUT CURRENT VERSUS OUTPUT VOLTAGE (OUTPUT LOW)



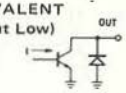
INPUT EQUIVALENT CIRCUIT



OUTPUT EQUIVALENT CIRCUIT (Output High)



OUTPUT EQUIVALENT CIRCUIT (Output Low)

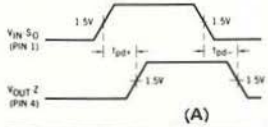


A. C. CHARACTERISTICS

SWITCHING WAVEFORMS – All inputs are outputs of TTL 9000 series gates loaded with 15 pf. All outputs are loaded with the same capacitance (referred to as C_L) and only with capacitance.

t_{pd}; S to Z_a

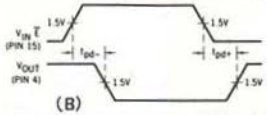
CONDITIONS – Pins 2, 15 = GND
Pin 3 = V_{CC}



(A)

t_{pd}; $\overline{E}$ to Z_a

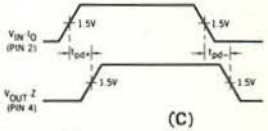
CONDITIONS – All Other Inputs High



(B)

t_{pd}; I_{0a} to Z_a

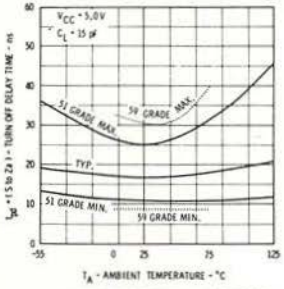
CONDITIONS – Pins 1, 15 = GND.



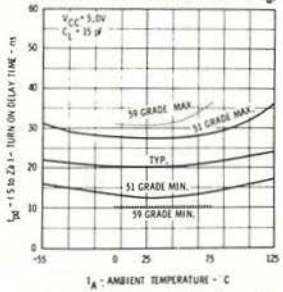
(C)

SWITCHING CHARACTERISTICS

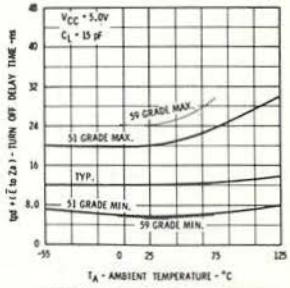
TURN OFF DELAY TIME VERSUS AMBIENT TEMPERATURE (S to Z_a)



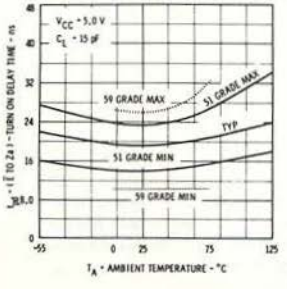
TURN ON DELAY TIME VERSUS AMBIENT TEMPERATURE (S to Z_a)



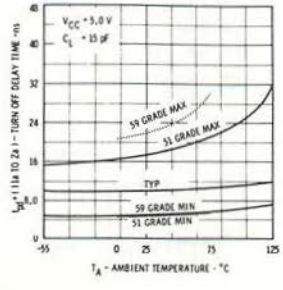
TURN OFF DELAY TIME VERSUS AMBIENT TEMPERATURE ($\overline{E}$ to Z_a)



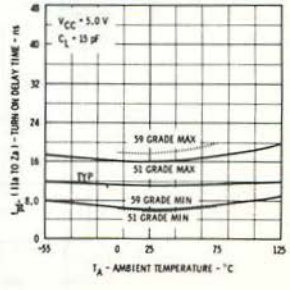
TURN ON DELAY TIME VERSUS AMBIENT TEMPERATURE ($\overline{E}$ to Z_a)



TURN OFF DELAY TIME VERSUS AMBIENT TEMPERATURE (I_{1a} to Z_a)

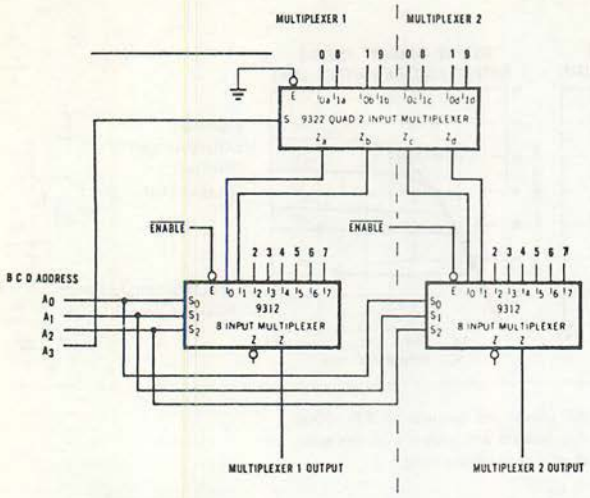


TURN ON DELAY TIME VERSUS AMBIENT TEMPERATURE (I_{1a} to Z_a)

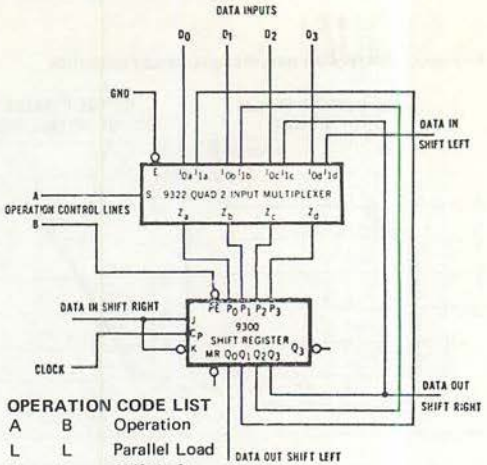


APPLICATIONS

DUAL 10 INPUT MULTIPLEXER



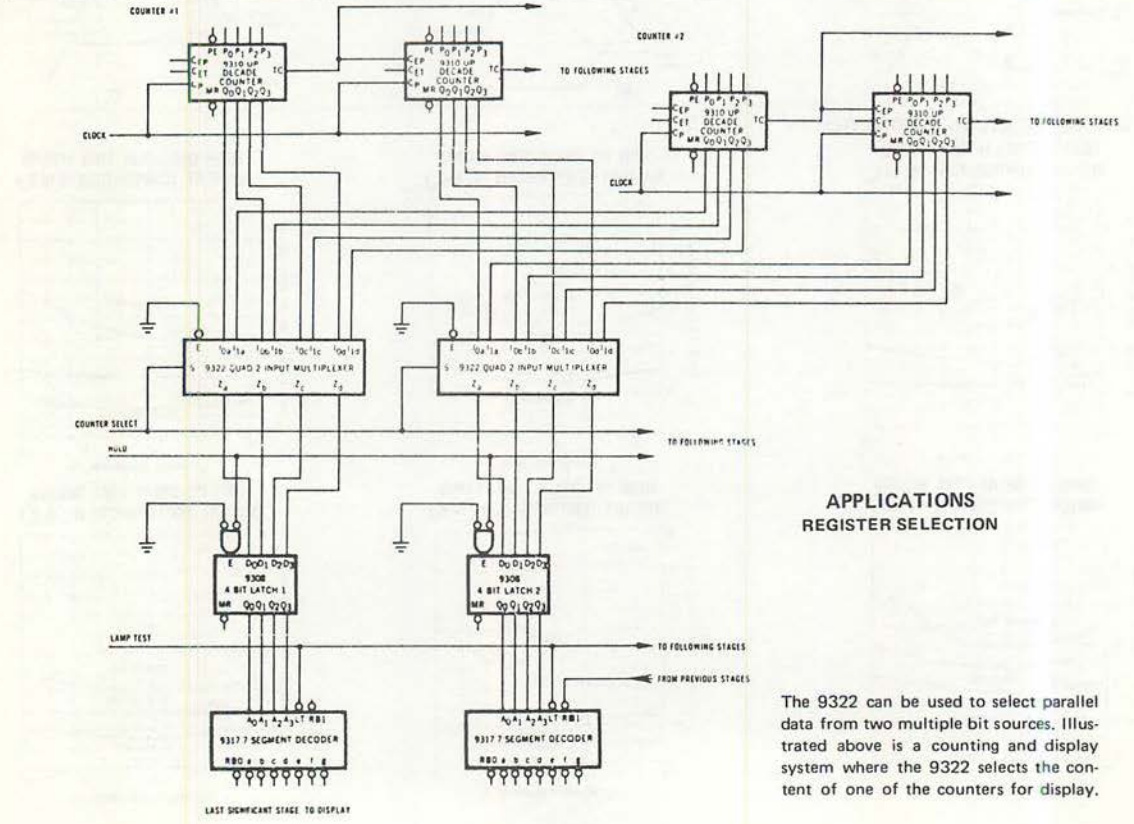
SHIFT LEFT, SHIFT RIGHT, PARALLEL LOAD REGISTER



OPERATION CODE LIST

A	B	Operation
L	L	Parallel Load
H	L	Shift Left
L	H	Shift Right
H	H	Shift Right

This register will shift left, shift right, and load 4 bits of parallel data according to the operation code applied to A and B.



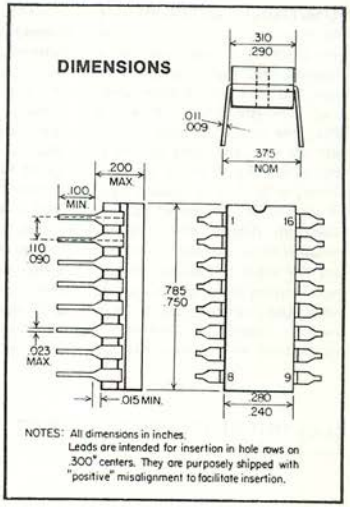
APPLICATIONS

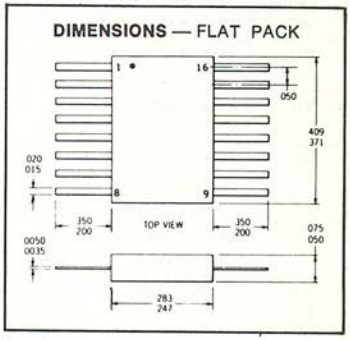
REGISTER SELECTION

The 9322 can be used to select parallel data from two multiple bit sources. Illustrated above is a counting and display system where the 9322 selects the content of one of the counters for display.

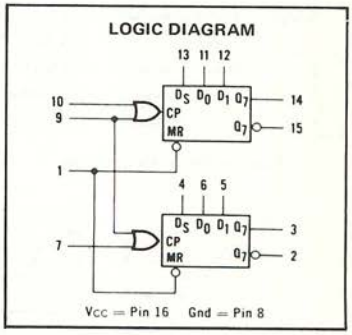
MSI DUAL 8-BIT SHIFT REGISTER

- 20 MHz Shift Frequency
- Two Input Multiplexer Provided at Data Input of Each Register
- Gated Clock Input Circuitry
- Both True and Complementary Outputs Provided from Last Bit of Each Register
- Asynchronous Master Reset Common to Both Registers
- Typical Power Dissipation of 300 mW
- Compatible with TTL and DTL families
- Input Diode Clamping





The ITT9328 is a high speed serial storage element providing sixteen bits of storage in the form of two eight bit registers that will shift at greater than 20 MHz rates. The multi-functional capability of this device is provided by several features: 1) Additional gating is provided at the input to both shift registers so that the input is easily multiplexed between two sources. 2) The clock of each register may be provided separately or together. 3) Both the true and complementary outputs are provided from each eight bit register, and both registers may be master cleared from a common input.



ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

CHARACTERISTICS	UNITS
Storage Temperature . . . . . −65°C to +150	°C
Temperature (Ambient) Under Bias . . . . . −55°C to + 125	°C
Vcc Pin Potential to Ground Pin . . . . . −0.5V to + 7	V
Voltage Applied to Outputs for high output state . −0.5V to + Vcc	value
Input Voltage (D.C.) . . . . . −0.5V to + 5.5	V

SPECIAL ORDERING CODE

Temperature Range:
1 = −55° + 125°C
5 = 0° to +75C

Package:
B = Flat Pack
D = Dual In-Line, 16 leads

Example:
ITT9328 - 1B means operating temperature range of −55° to +125°C, supplied in a Flat Pack

FUNCTIONAL DESCRIPTION – The two 8 bit shift registers have a common clock input (pin 9) and separate clock inputs (pins 10 & 7). The clocking of each register is controlled by the OR function of the separate and the common clock input. Each register is composed of eight clocked RS master-slave flip-flops and a number of gates. The clock OR gate drives the eight clock inputs of the flip-flop in parallel. When the two clock inputs (the separate and the common) to the OR gate are low, the slave latches are steady, but data can enter the master latches via the R and S input. During the first low to high transition of either, or both simultaneously, of the two clock inputs, the data inputs (R and S) are inhibited so that a later change in input data will not affect the master; then the now trapped information in the master is transferred to the slave. When the transfer is complete, both the master and the slave are steady as long as either or both clock inputs remain high. During the high to low transition of the last remaining high clock input, the transfer path from master to slave is inhibited first, leaving the slave steady in its present state; second the data inputs (R and S) are enabled so that new data can enter the master. Either of the clock inputs can be used as clock inhibit inputs by applying a logic high signal. Each 8 bit shift register has a two input multiplexer in front of the serial data input. The two data inputs Do and D1 are controlled by the data select input Ds following the Boolean expression:

Serial data in: $S_D = D_S D_O + D_S D_I$

An asynchronous master reset is provided which, when activated by a low logic level, will clear all sixteen stages independently of any other input signal.

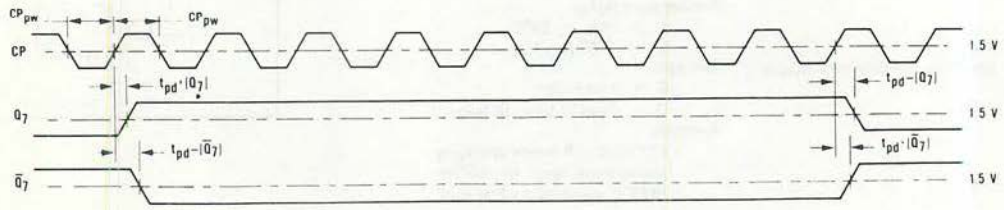
LOADING RULES (1 U.L. = TTL input gate load)

INPUT	FAN IN
MR, D_O, D_I	1 Unit Load
Separate CP (pins & & 10)	1.5 Unit Loads
D_S	2 Unit Loads
Common CP (pin 9)	3 Unit Loads
OUTPUT	**FAN OUT**
Q_7, $\bar{Q}_7$	6 Unit Loads

ELECTRICAL CHARACTERISTICS (T_A = −55°C to + 125°C, V_{CC} = 5.0V ± 10%)

		LIMITS							
		−55°C		+ 25°C			+ 125°C		
SYMBOL	CHARACTERISTICS	MIN.	MAX.	MIN.	TYP.	MAX.	MIN.	MAX.	UNITS	TEST CONDITIONS
V_{OH}	Output High Voltage	2.4		2.4	2.7		2.4		Volts	V_{CC}=4.5V, I_{OH}=−0.36mA
V_{OL}	Output Low Voltage		0.4		0.2	0.4		0.4	Volts	V_{CC}=5.5V, I_{OL}=9.6mA V_{CC}=4.5V, I_{OL}=7.44mA
V_H	Input High Voltage	2.0		1.7			1.4		Volts	Guaranteed input high threshold for all inputs
V_L	Input Low Voltage		0.8			0.9		0.8	Volts	Guaranteed input low threshold for all inputs
I_F	Input Load Current (MR, D_O, D_1)		−1.6		−1.0	−1.6		−1.6	mA	
1.5I_F	Input Load Current (separate CP pins 7 & 10		−2.4		−1.5	−2.4		−2.4	mA	V_{CC}=5.5V
2 I_F	Input Load Current (D_S)		−3.2		−2.0	−3.2		−3.2	mA	V_F=0.4V
3 I_F	Input Load Current (common CP pin 9)		−4.8		−3.0	−4.8		−4.8	mA	
I_p	Input Leakage Current (MR, D_O, D_1)		60		10	60		60	μA	
1.5I_p	Input Leakage Current (separate CP pins 7 & 10)		90		15	90		90	μA	V_{CC}=5.5V
2 I_p	Input Leakage Current (D_S)		120		20	120		120	μA	V_R=4.5V
3 I_p	Input Leakage Current (common CP pin 9)		1801		30	180		180	μA	
I_{PD}	Power Dissipation		365		300	365		365	mW	V_{CC}=5.0V

SWITCHING WAVEFORMS



Note: Q_7 is connected to D_1. Other clock is grounded.

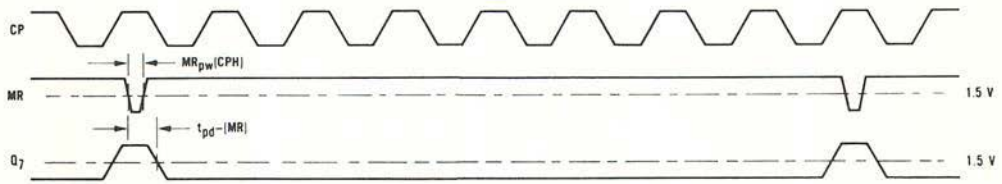
Fig. 1

ELECTRICAL CHARACTERISTICS (T_A = 0°C to + 75°C, V_{cc} = 5.0V ± 5%)

SYMBOL	CHARACTERISTICS	LIMITS 0°C MIN.	0°C MAX.	+25°C MIN.	+25°C TYP.	+25°C MAX.	+75°C MIN.	+75°C MAX.	UNITS	TEST CONDITIONS
V_{OH}	Output High Voltage	2.4		2.4	3.0		2.4		Volts	V_{CC}=4.75V, I_{OH}=−0.36mA
V_{OL}	Output Low Voltage		0.45		0.2	0.45		0.45	Volts	V_{CC}=5.25V, I_{OL}=9.6mA V_{CC}=4.75V, I_{OL}=8.5mA
V_{IH}	Input High Voltage	1.9		1.8			1.6		Volts	Guaranteed input high threshold for all inputs
V_{IL}	Input Low Voltage		0.85			0.85		0.85	Volts	Guaranteed input low threshold for all inputs
I_F	Input Load Current (MR,D_0,D_1)		−1.6		−1.0	−1.6		−1.6	mA	
1.5I_F	Input Load Current (separate CP pins 7 & 10)		−2.4		−1.5	−2.4		−2.4	mA	V_{CC}=5.25V
2 I_F	Input Load Current (D_S)		−3.2		−2.0	−3.2		−3.2	mA	V_F=0.4V
3 I_F	Input Load Current (common CP pin 9)		−4.8		−3.0	−4.8		−4.8	mA	
I_R	Input Leakage Current (MR,D_0,D_1)		60		10	60		60	μA	
1.5 I_R	Input Leakage Current (separate CP pins 7 & 10)		90		15	90		90	μA	V_{CC}=5.25V
2 I_R	Input Leakage Current (D_S)		120		20	120		120	μA	V_R=4.5V
3 I_R	Input Leakage Current (common CP pin 9)		180		30	180		180	μA	
I_{PD}	Power Dissipation		365		300	365		365	mW	V_{CC}=5.0V

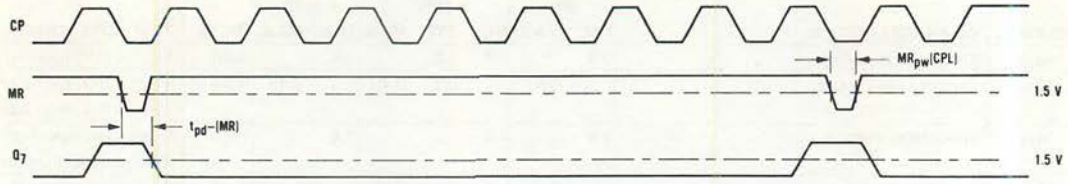
SWITCHING CHARACTERISTICS (T_A= 25°C)

SYMBOL	CHARACTERISTICS	MIN.	TYP.	MAX.	UNITS	TEST CONDITIONS
t_{pd}−(Q_7& Q_7	Turn-Off Delay (clock to output)		13		ns	V_{cc}=5.0V, C_L=15 pF Fig.1
t_{pd}−(Q_7&$\bar{Q}_7$)	Turn-On Delay (clock to output)		22		ns	
t_{pd}−(MR)	Turn-On Delay (Master reset to output)		35		ns	V_{cc}=5.0V, C_L=15pF Fig. 2 & 3
CP_{pw}	Min. Clock Pulse Width		14		ns	V_{cc}=5.0V, C_l=15 pF Fig. 1
MR_{pw}(CPH)	Min. Master Reset pulse width with clock high		15		ns	V_{cc}5.0V, C_L=15 pF Fig. 2
MR_{pw}(CPL)	Min. Master Reset pulse width with clock low		28		ns	V_{cc}=5.0V, C_L=15pF Fig. 3



Note: D_S, D_1, D_0, are high. Other clock input is grounded.

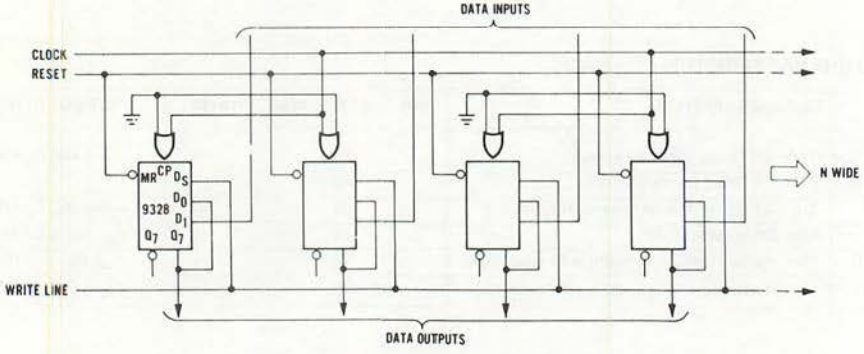
Fig. 2



Note: D_S, D_1, D_0 are high. Other clock input is grounded.

Fig. 3

APPLICATION:



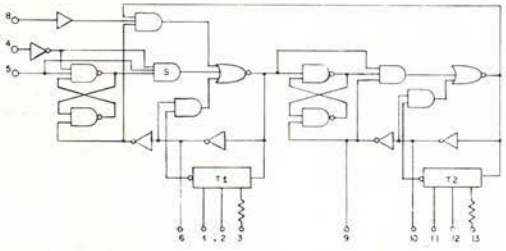
N-BIT BY 8-WORD HIGH-SPEED MEMORY

ANNOUNCEMENT OF ADDITIONAL PRODUCTS EXCLUSIVELY ITT'S

Data Sheets are being prepared on products listed below. Write for your copies.

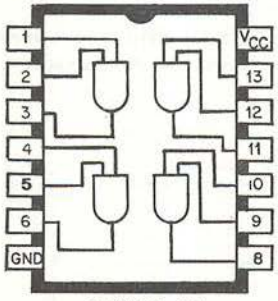
54124/74124 - UNIVERSAL PULSE GENERATOR

- Specially designed for clock and delayed pulse generation
- 2 cascaded multivibrators for delayed pulse
- Gated feedback for high stability controlled oscillation
- No jitter self-start
- Positive Schmitt trigger input



54130/74130, 54131/74131 - QUAD 2 I/P AND POWER DRIVERS

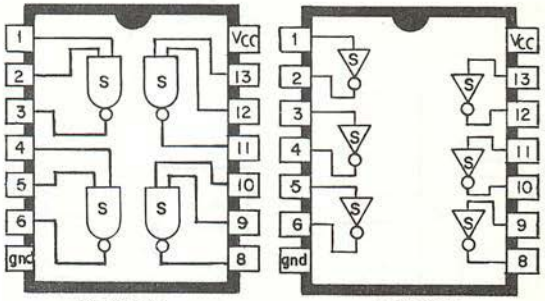
- 100 mA I_{sink}
- 54130/74130 30 V open collector rating
- 54131/74131 15 V open collector rating
- Pin compatible with 54/7408
- V_{OL} at 100 mA = 0.4 V max



54/74130-131

54135/74135, 54137/74137 - QUAD/HEX NAND SCHMITT TRIGGERS

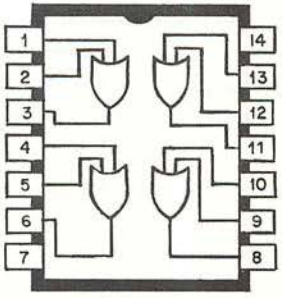
- High input impedance - compatible with 54/74L, MOS, HLL and high voltage transducers, etc.
- Temperature compensated thresholds
- Input load factor 1/4 unit load
- 15 V input rating
- 54135/74135 pin compatible with 54/7400 and 54/74132
- 54137/74137 pin compatible with 54/7404 and 54/7414



54/74135 54/74137

54138/74138, 54139/74139 - QUAD 2 I/P OR POWER DRIVERS

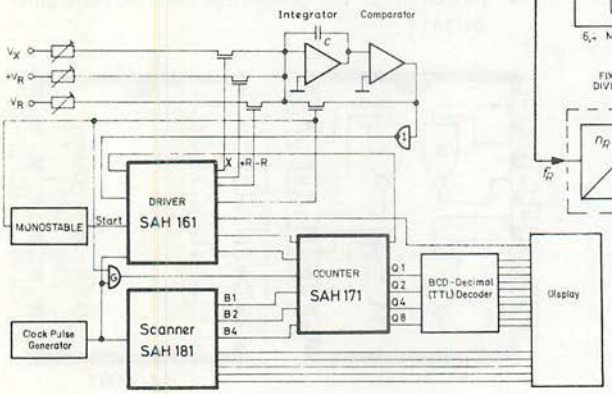
- 100 mA I_{sink}
- 54138/74138 30 V open collector rating
- 54139/74139 15 V open collector rating
- Pin compatible with 54/7432
- V_{OL} at 100 mA = 0.4 V max



54/74138-139

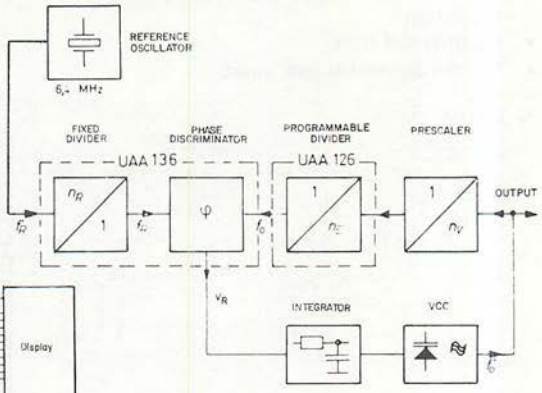
SAH 161, SAH 171, SAH 181 - DIGITAL VOLTMETER KIT

- Kit consists of 3 MOS-LSI Circuits for use in Digital Voltmeters and similar analog to Digital Convertors
- SAH 161 is the clock generator and driver circuit
- SAH 171 is the counter and memory circuit
- SAH 181 is the scanner and display driver
- The use of these three circuits together with a minimum of external components results in a low cost high performance digital voltmeter



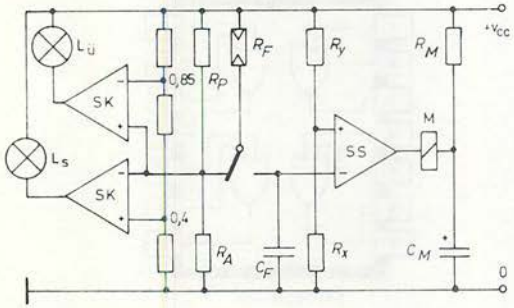
UAA 126, UAA 136 - PHASE SYNCHRONIZED MULTICHANNEL OSCILLATOR KIT

- For use as frequency synthesizer in mobile transmitters/receivers
- 410 channels spaced 25 KHz from 9.25 to 19.5 MHz
- UAA 126 is a programmable divider
- UAA 136 is a fixed divider, phase discriminator
- Can be used for other frequency ranges by using suitable pre-scalers or mixers



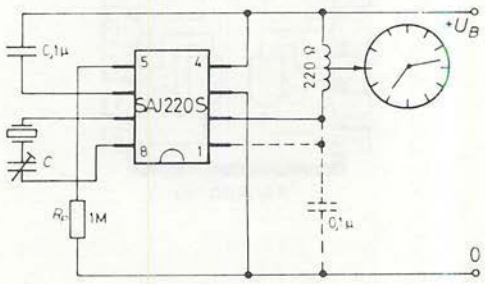
UAA 110 - STILL CAMERA CIRCUIT

- Monolithic integrated circuit for use in still cameras
- Controls exposure under varying light conditions
- Output capability to show need to use a tripod
- Battery monitor



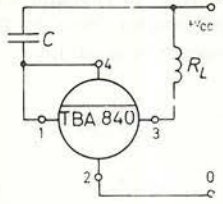
SAJ 220 - FAMILY OF QUARTZ WATCH AND CLOCK CIRCUITS

- Low power/low voltage bipolar technology
- Family offers circuits for use in watches and clocks driven from a quartz crystal
- On chip oscillator, 15 stages and output motor driver on one chip
- Available with different output pulse widths and in micro dip and mini dip packages



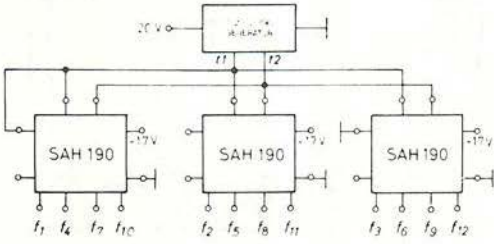
TBA 840 - SINGLE COIL WATCH REGULATOR

- Single monolithic circuit for driving and regulating watches having a single-coil movement
- For use with mercury or silver oxide monocells
- Also usable with tuning fork oscillator watches
- Available in micro-three pin packages



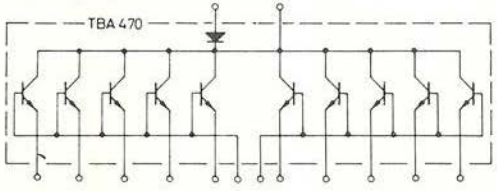
SAH 190 - MOS TOP OCTAVE ELECTRONIC ORGAN TONE GENERATOR

- High accuracy. Less than ±0.003% against tempered tone scale
- Option I allows switching to half or full tone lower
- Option II allows output frequency change by a complete octave
- A full top octave requires three identical devices
- Outputs compatible to drive SAJ 110 seven-stage divider



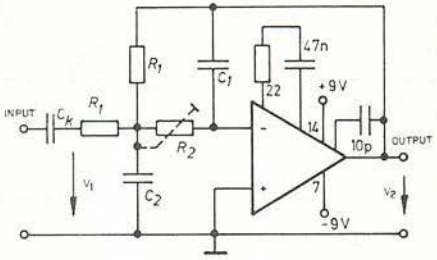
TBA 470 - TEN STAGE GATE. e. g. ELECTRONIC ORGANS

- Allows use of single mechanical contact instead of 10 per key
- Each of the ten separate emitter tone signals are summed at common collector
- Check suppression capability



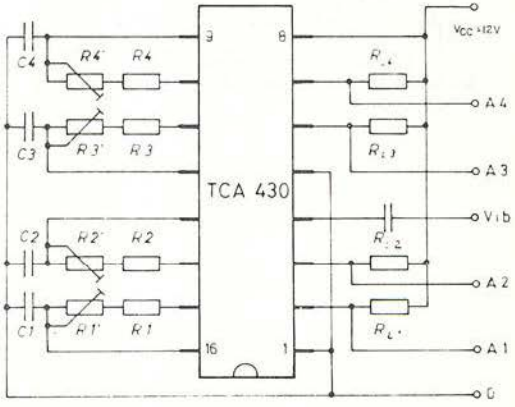
TCA 250 - DUAL ACTIVE FILTER AMPLIFIER

- Dual amplifier circuit designed specifically for active filter applications in audio frequency range
- For use in 2nd order low pass filter using one stage or as a 4th order low pass filter using both stages
- Adjustable roll-off characteristic



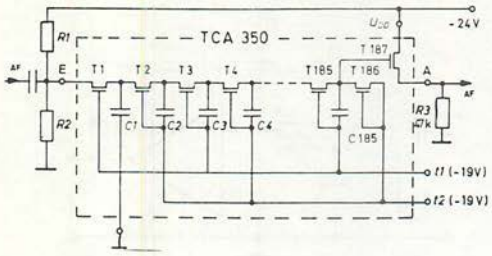
TCA 430 - QUAD-OSCILLATOR (TONE GENERATOR FOR ELECTRONIC ORGANS

- One monolithic chip contains 4 RC oscillators and designed for use in several organ applications
- Three circuits provide a low cost top octave generator with outputs compatible with the SAJ 110 seven-stage frequency divider
- TCA 430 is temperature neutral, thus, accuracy is a function of external R&C
- Separate pin for simultaneous vibrator



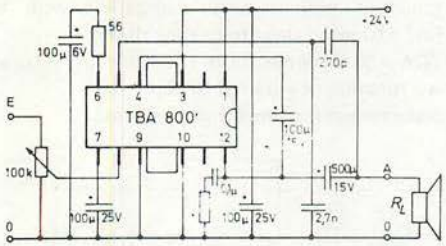
TCA 350 - ANALOG SHIFT REGISTER (DELAY LINE)

- 185 stage "bucket-brigade" delay line for audio frequency signals
- Uses symmetrical clock inputs up to 500 KHz
- Delay can be varied. $t = \frac{185}{2.fclock}$



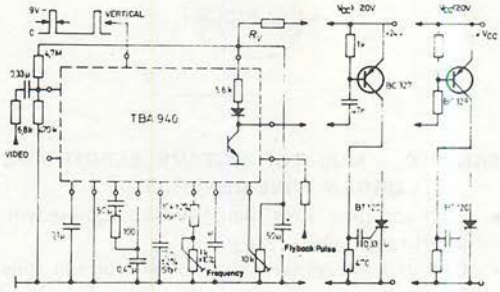
TBA 800 -5 WATTS AUDIO AMPLIFIER

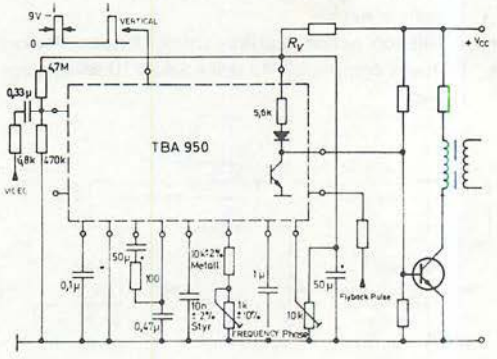
- Monolithic circuit providing 5 watts into 16 Ω at V_{CC} = 24 volts
- For use in Radio, TV and Phono applications
- Uses popular heat tab package designed for on-board heat dissipation



TBA 940, TBA 950 - TV HORIZONTAL DEFLECTION SYSTEMS

- Each circuit contains oscillator and all other functions of TV Horizontal deflection system up to driver
- TBA 940 designed for Thyristor (SCR) Deflection
- TBA 950 designed for Transistor Deflection
- Video recorder drive capability





ITT's 300 Digital Integrated Circuits are designed for applications where a high degree of DC and AC noise immunity is required. The family includes a full complement of gates, inverters, expanders, flip flops, counters and decoders.

ITT HLL is available in in both industrial and military temperature ranges, in both 12v V_{CC} and 15v V_{CC} versions.

ITT 300 Series finds application in electrostatic copy machines, industrial systems such as injection molding or automated welder control, and military systems operating under the most severe conditions where errors caused by noise are intolerable. By virtue of its 12v nominal V_{CC} with relative insensitivity to supply variations, HLL is a perfect choice for automotive applications. In general, any system which previously required relays for logic can benefit from the many capabilities of ITT 300 Series.

- 3.5v guaranteed D.C. noise margin
- 16 pin ceramic or plastic dual in line packages
- 15 volt logic swing or 12 volt logic swing available
- Buffered outputs on all elements
- Insensitivity to short noise pulses
- Choice of full or limited temperature ranges
- Interface with discrete components and Linear I.C.
- Line driving and receiving capabilities

NAND GATES/INVERTERS

ITT 321 QUAD 2 INPUT NAND GATE (ACTIVE PULL-UP)
ITT 322 DUAL 5 INPUT NAND GATE (ACTIVE PULL-UP)
ITT 323 QUAD 2 INPUT NAND GATE (OPEN COLLECTOR)
ITT 324 QUAD 2 INPUT NAND GATE (PASSIVE PULL-UP)
ITT 325 DUAL 2 INPUT, DUAL 3 INPUT NAND GATE (ACTIVE PULL-UP)
ITT 326 DUAL 2 INPUT, DUAL 3 INPUT NAND GATE (PASSIVE PULL-UP)
ITT 332 QUAD INVERTER, DUAL 2 INPUT NAND GATE (OPEN COLLECTOR)
ITT 333 QUAD INVERTER, DUAL 2 INPUT NAND GATE (PASSIVE PULL-UP)
ITT 334 HEX INVERTER WITH STROBE (OPEN COLLECTOR)
ITT 335 HEX INVERTER WITH STROBE (PASSIVE PULL-UP)

BUFFERS

ITT 301 DUAL 5 INPUT NAND BUFFER (ACTIVE PULL-UP)
ITT 302 QUAD 2 INPUT NAND BUFFER (OPEN COLLECTOR)
ITT 303 QUAD 2 INPUT NAND BUFFER (PASSIVE PULL-UP)

AND - OR - INVERT GATES

ITT 341 DUAL 2 WIDE, 2 INPUT AND-OR-INVERT GATE (ACTIVE PULL-UP)
ITT 344 DUAL 2 WIDE, 2 INPUT AND-OR-INVERT GATE (W/OUTPUT EXPANDER)

EXPANDERS

ITT 331 DUAL 5 INPUT EXPANDER

FLIP-FLOPS

ITT 311 MASTER/SLAVE FLIP-FLOP
ITT 312 DUAL J-K FLIP-FLOP
ITT 342 DUAL ONE SHOT MULTIVIBRATOR
ITT 370 QUAD D FLIP-FLOP (LATCH)

INTERFACE ELEMENTS

ITT 361 DUAL HIGH LEVEL TO DTL/TTL INTERFACE
ITT 362 DUAL DTL/TTL TO HIGH LEVEL INTERFACE
ITT 363 QUAD DTL/TTL TO HIGH LEVEL INTERFACE

DECODERS

ITT 380 ONE-OF-TEN DECODER/DRIVER
ITT 381 ONE-OF-TEN DECODER

COUNTERS

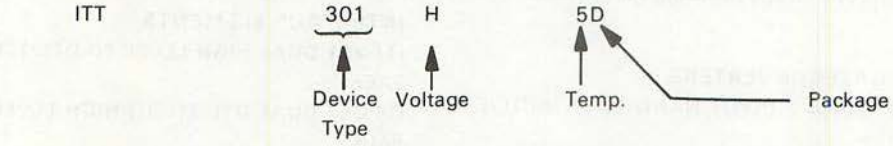
ITT 371 DECADE COUNTER
ITT 372 HEXADECIMAL COUNTER

ABSOLUTE MAXIMUM RATINGS

Characteristics	Units
Storage Temperature Range	
Ceramic	-65°C to +150 °C
Plastic	-55°C to +100 °C
Operating Temperature Range	
ITT300-1D	−55°C to +125 °C
ITT300-1D1	−55°C to +125 °C
ITT300-5D	−30°C to +85 °C
ITT300-5D1	−30°C to +75 °C
Lead Temperature, 1/16 inch from case, 10 seconds maximum	300 °C
Supply Voltage - Continuous	+16.5 Volts
Supply Voltage - Pulsed <0.1 second	+18 Volts
Input Voltage - (exclusive of expanders)	
12V Version	−0.5V to +16.5 Volts
15V Version	−0.5V to +18.0 Volts
Input Voltage - expanders	0 V to +6.0 Volts
Voltage applied to output	−0.5V to +16.5 Volts
Sink Current at T_A =25°C, continuous	
301 & 302	80 mA
All other types	15 mA
Surge Sink Current at T_A =25°C, <1 sec.	
301 & 302	100 mA
All other types	20 mA
Output Short Circuit Duration to GND	Continuous

ORDERING INFORMATION

The full type number designates temperature range, voltage and package as follows:



Part No.	TEMP RANGE	V_{CC}(Nominal)	PACKAGE	CROSS REFERENCE ITT (obsolete)	CROSS REFERENCE TELEDYNE
ITT 3xx −5N	−30°C to +85°C	12V	Plastic Dip	5N	CJ
ITT 3xxH−5N	−30°C to +70°C	15V	Plastic Dip	5N1	AJ
ITT 3xx −5D	−30°C to +85°C	12V	Ceramic Dip	5D	CL
ITT 3xxH−5D	−30°C to +70°C	15V	Ceramic Dip	5D1	AL
ITT 3xx −1D	−55°C to +125°C	12V	Ceramic Dip	1D	BL
ITT 3xxH−1D	−55°C to +125°C	15V	Ceramic Dip	1D1	ML

PARAMETER	DEFINITION	12V VERSION (V_{CC} = +12V ±1V)	15V VERSION (V_{CC} = +15V ±1V)	TEST CONDITIONS
V_{IL}	Input threshold voltage, low	5.0V MIN	5.0V MIN	Guaranteed input low threshold for all inputs except 311 T_2 = 4.8V MIN at 15V
V_{IH}	Input threshold voltage, high (except 311 $\overline{S}$ and $\overline{R}$)	6.5V MAX	6.5V MAX	Guaranteed input high threshold for all inputs (except 311 $\overline{S}$ and $\overline{R}$)
	V_{IH} of 311 $\overline{S}$ and $\overline{R}$ inputs	7.0V MAX	7.0V MAX	Guaranteed V_{IH} of 311 $\overline{S}$ and $\overline{R}$ inputs
I_{IL}	Input current, low; 1 unit load	2.1 mA MAX	2.6 mA MAX	At V_{CC} MAX with V_{IN} = V_{OL1} MAX
I_{IH}	Input leakage current; 1 unit load	10 μA MAX	10 μA MAX	At V_{CC} MAX with V_{IN} = V_{CC} MAX
V_{OL}	Output low voltage (see loading table on data sheet for applicable V_{OL}			
	V_{OL1} - generally applicable	1.5V MAX	1.8V MAX	I_{OL} = F.O. x UL
	V_{OL2} - 301 buffer only	1.8V MAX	2.0V MAX	I_{OL} = F.O. x UL At V_{CC} MIN with
	V_{OL3} - open collector types	0.4V MAX	0.4V MAX	I_{OL} = F.O. x UL V_{IL} = 5.0V, V_{IH} = 6.5V
	V_{OL4} - 380 decoder only	1.2V MAX	1.2V MAX	I_{OL} = 30 mA
V_{OH}	Output high voltage of all devices	10.0V MIN	13.0V MIN	At V_{CC} MIN, V_{IL} = 5.0V, V_{IH} = 6.5V: I_{OH} = F.O. x UL
I_{OH}	Output high source of active pullup devices current of 301	5.0mA MIN 15 mA MIN	5.0 mA MIN 15 mA MIN	At V_{CC} nominal, V_{IL} = 5.0V, V_{IH} = 6.5V: V_{OH} = 7.0V for 12V VERSION, 9.5V for 15V VERSION
V_{MAX}	Output high breakdown voltage of the following devices			At I_{MAX} of
	302 and 323 gates	13.0V MIN	16.5V MIN	4 mA At V_{CC} MAX, V_{IL} = 5.0V
	332 and 334 inverters	20.0V MIN	24.0V MIN	4 mA V_{IH} = 6.5V, with
	380 decoder	24.0V MIN	24.0V MIN	0.5 mA I_{MAX} forced into input
	381 decoder	15.0V MIN	15.0V MIN	0.5 mA
I_{CEX1}	Output high leakage current of open collector devices	25 μA MAX	25 μA MAX	At V_{CC} MAX, V_{IL} = 5.0V, V_{IN} = 6.5V: V_{CEX} = V_{CC} MAX
V_{CC} MAX	TEST SUPPLY VOLTAGE	13.0V	16.0V	
V_{CC} MIN	TEST SUPPLY VOLTAGE	11.0V	14.0V	
V_{CC} NOM	TEST SUPPLY VOLTAGE	12.0V	15.0V	

F.O. is fanout in unit loads (UL). Unit loadings are given in the pin tables on the individual data sheets. A unit load for ITT 300 Series is defined by the above input specifications.

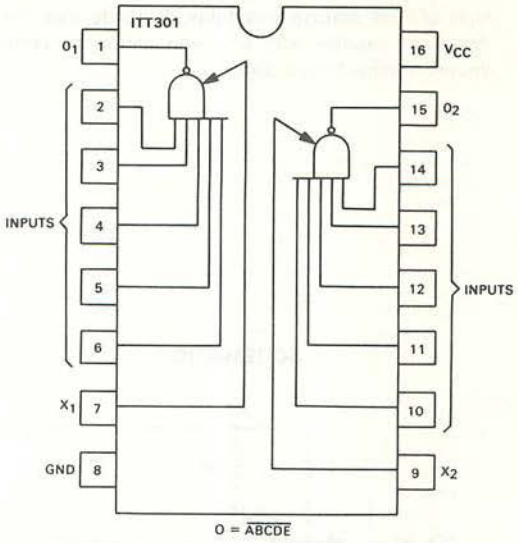
SUMMARY OF DEVICE PROPAGATION DELAYS AND WORST-CASE SUPPLY CURRENTS

Device	Delay Range (nanoseconds)		Worst-Case I_{CC}(mA) 12V	15V
301 dual 5-input power NAND gate	240	400	48	68
302 quad 2-input power NAND gate (OC)	240	600	40	60
303 quad 2-input power NAND gate (PP*)	240	600	49	70
311 master/slave flip-flop	250	820	18	25
312 dual J-K or S-R flip-flop	230	600	30	40
321 quad 2-input NAND gate	200	300	15	20
322 dual 5-input NAND gate	190	550	8	11
323 quad 2-input NAND gate (OC)	160	400	5.5	8
324 quad 2-input NAND gate (PP)	200	600	28	40
325 2,2,3,3-input NAND gate	200	300	15	20
326 2,2,3,3-input NAND gate (PP)	200	600	28	40
331 dual 5-input gate expander			4.2	5.2
332 hex inverter gate (OC)	140	350	28	42
333 hex inverter gate (PP)	140	350	42	60
334 strobed hex inverter (OC)	140	350	28	42
335 strobed hex inverter (PP)	140	350	42	60
341 dual 2-input AND-OR-INVERT gate	150	410	11	15
342 dual monostable multivibrator	160	260	17	23
344 dual exclusive-OR gate	200	600	10	14
361 dual input interface	230	325	8	11
362 dual output interface	100	400	10	13
363 quad output interface	240	600	51	64
370 quad latch	500	500	38	48
371 decade counter	200	800	41	53
372 hexadecimal counter	200	800	41	53
380 BCD to decade decoder/driver	NA	NA	30	38
381 BCD to decade decoder	300	500	30	38

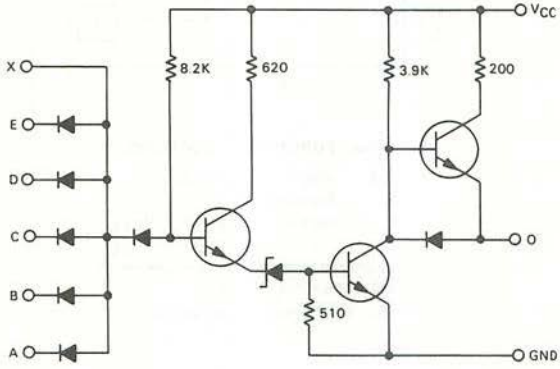
NOTE: Only the shortest and longest delays are listed for each device.
See the device data sheets for all input-output propagation delays.

The ITT 301 is an active pull-up element featuring high current capability in both the high and low state. It is an excellent choice for driving long transmission lines, as a system clock driver, or for driving any load with high capacitance or inductance.

PIN CONFIGURATION



SCHEMATIC (EACH GATE)

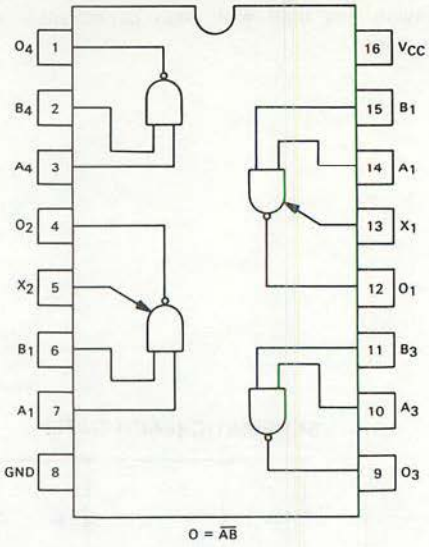


PINS	FUNCTION	LOADING
A-E	Inputs	1 UL
X	Expanders	*
O	Outputs	20 UL at V_{OL1} (12V or 15V) 30 UL at V_{OL2} (12V) 25 UL at V_{OL2} (15V)

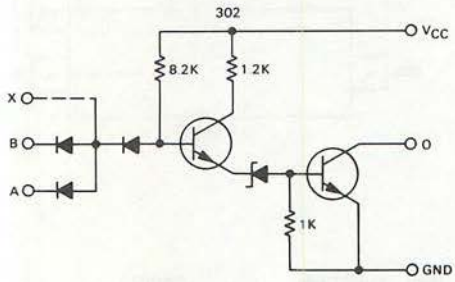
* Each diode tied to X_1 or X_2 is 1 unit load.

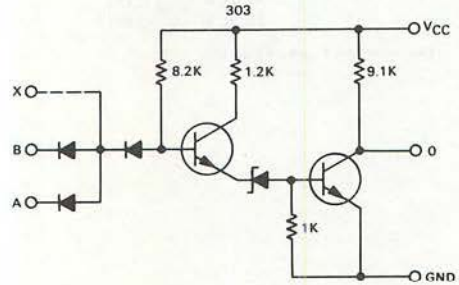
The ITT 302 and 303 are open collector and passive pull-up, respectively, power gates with high current sinking capability. Both devices are "wire-or" capable and find application as lamp drivers or high-fanout gates.

PIN CONFIGURATION



SCHEMATIC





PINS	FUNCTION	LOADING
A,B	Inputs	1 UL
X	Expanders	
O	Outputs	5 UL at V_{OL1} 20 UL at V_{OL1}

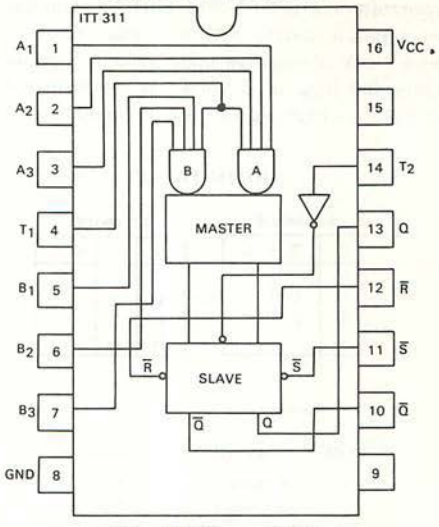
20 unit loads handled with correct external resistor

302 handles 10 TTL loads at V_{OL3}

* Each diode tied to X_1 or X_2 is 1 unit load.

The ITT 311 is a universal HLL flip-flop. It has separate clocks which allow two-phase (dual inhibit) operation, direct set and reset inputs, six data inputs, and is level sensitive. It can be operated as a J-K flip-flop by external wiring and features active outputs.

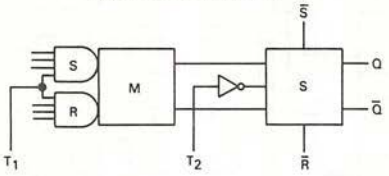
PIN CONFIGURATION



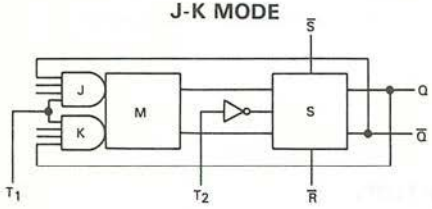
PINS	FUNCTION	LOADING
A,B	Data inputs	1 UL
T_1	Clock input	2 UL
T_2	Clock input	1 UL
$\bar{S}$,$\bar{R}$	Direct $\bar{S}$-$\bar{R}$ inputs	1 UL
Q,$\bar{Q}$	Outputs	5 UL at V_{OL1}

CIRCUIT DIAGRAM

SET-RESET MODE



J-K MODE



J-K OPERATION

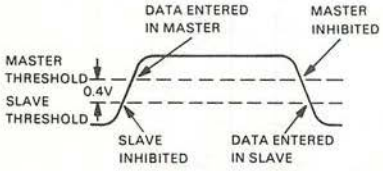
A	B	Q^{n+1}
L	L	Q^n
L	H	L
H	L	H
H	H	$\bar{Q}^n$

S-R OPERATION

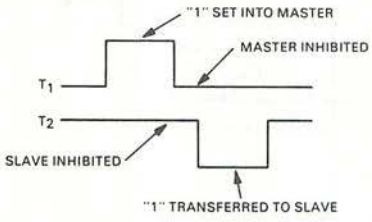
A	B	Q^{n+1}
L	L	Q^n
L	H	L
H	L	H
H	H	X

X = Undetermined

SINGLE-PHASE TIMING

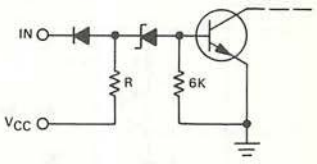


TWO-PHASE TIMING



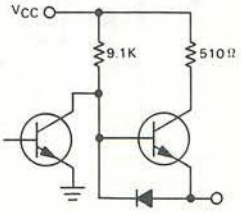
SCHEMATIC

TYPICAL INPUT



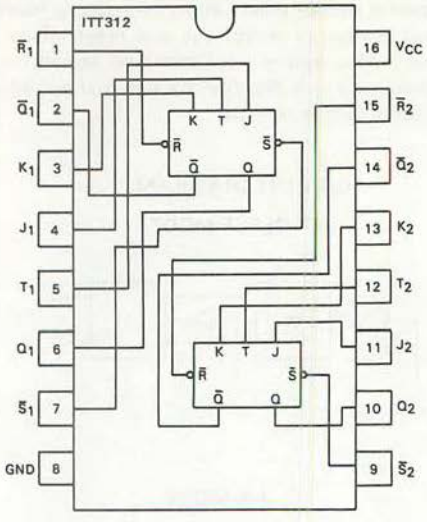
R = 8.2K ON A, B, $\bar{S}$, $\bar{R}$, T_2
R = 4.1K ON T_1

TYPICAL OUTPUT



Two completely separated J-K flip-flops are incorporated on one 312 chip. Each flip-flop has its own separate clock, set, and reset inputs. The device clock is negative edge sensitive, requiring a clock fall time of 3 volts per microsecond or faster. Active-high outputs are provided.

PIN CONFIGURATION



TRUTH TABLE

S-R MODE

$\overline{S}$	$\overline{R}$	Q
H	H	X
H	L	L
L	H	H
L	L	H

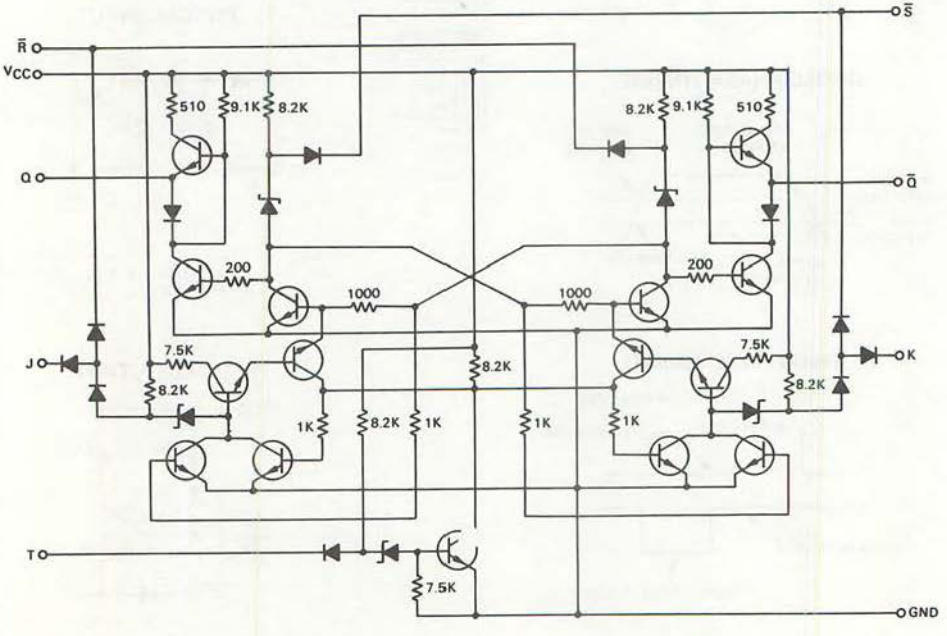
J-K MODE

J	K	Q^{n+1}
L	L	Q^n
L	H	L
H	L	H
H	H	$\overline{Q}^n$

X = Indeterminate state

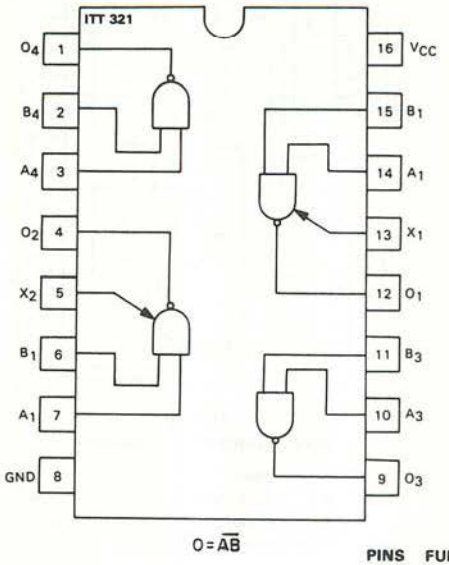
PINS	FUNCTION	LOADING
J,K	J-K inputs	1 UL
T	Clock inputs	1 UL
$\overline{S}$,$\overline{R}$	Direct $\overline{S}$-$\overline{R}$ inputs	2 UL
Q,$\overline{Q}$	Outputs	5 UL at V_{OL1}

SCHEMATIC (EACH FLIP-FLOP)



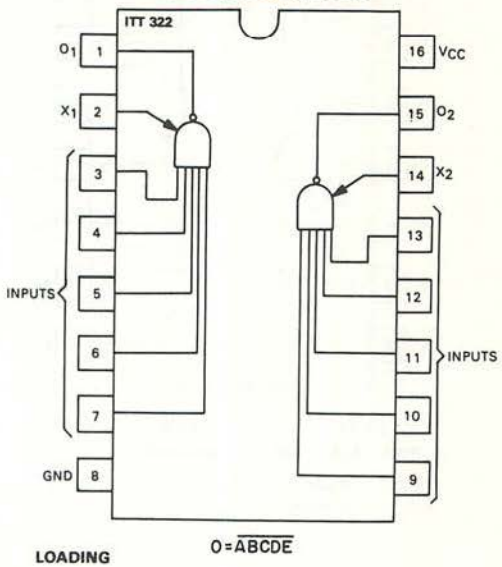
The ITT 321, 322, 325, and 341 make up the active - output group of HLL gates. Active-high outputs have high source current capability for driving lines of moderate length or high capacitance loads.

PIN CONFIGURATION



$O = \overline{AB}$

PIN CONFIGURATION

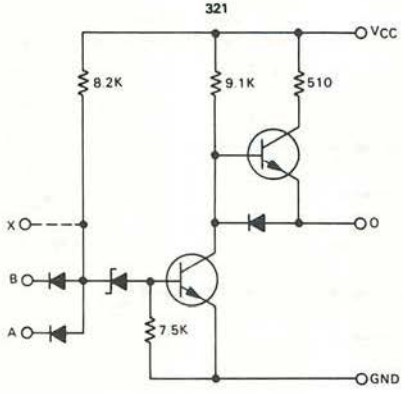


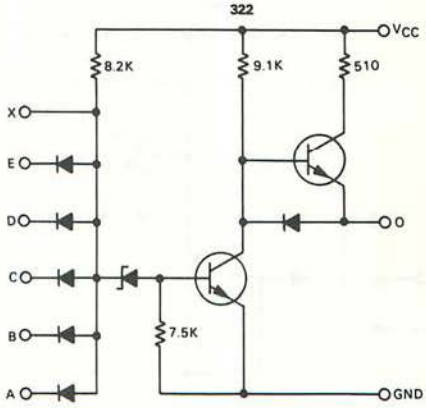
$O = \overline{ABCDE}$

PINS	FUNCTION	LOADING
A-E	Inputs	1 UL
X	Expanders	*
O	Outputs	5 UL at V_{OL1}

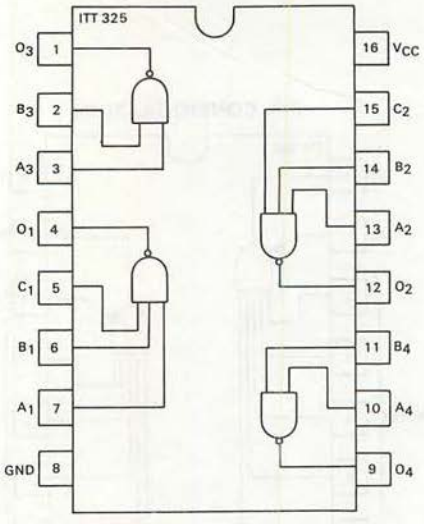
* Each diode tied to X_1 or X_2 is 1 unit load.

SCHEMATIC (EACH GATE)





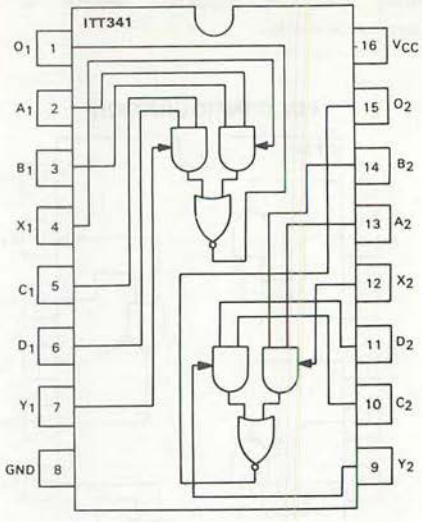
PIN CONFIGURATION



$O = \overline{AB}$ $\quad O = \overline{ABC}$

PINS	FUNCTION	LOADING
A-C	Inputs	1 UL
O	Outputs	5 UL at V_{OL1}

PIN CONFIGURATION

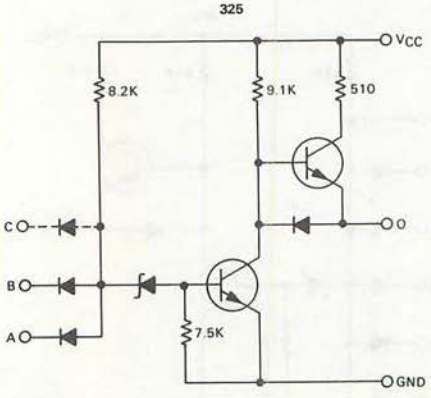


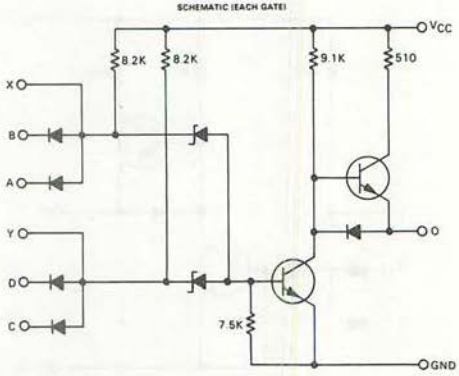
$O = \overline{AB \& CD}$

PINS	FUNCTION	LOADING
A-D	Inputs	1 UL
X	Expanders	
O	Outputs	5 UL at V_{OL1}

* Each diode tied to X_1 or X_2 is 1 unit load

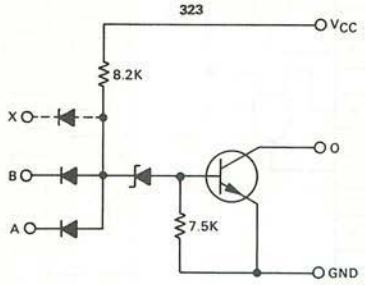
SCHEMATIC (EACH GATE)



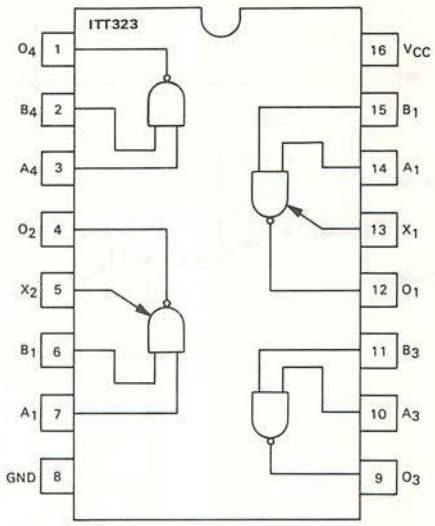


The ITT 323, 332, and 334 are HLL's open-collector gates. Open, or uncommitted, collectors can be , or connected through an appropriate pull-up resistor to a power supply other than that used for the HLL gate. This capability allows open-collector devices to interface directly to DTL, TTL, or MOS, or to drive small indicator lamps or relays directly.

SCHEMATIC



PIN CONFIGURATION

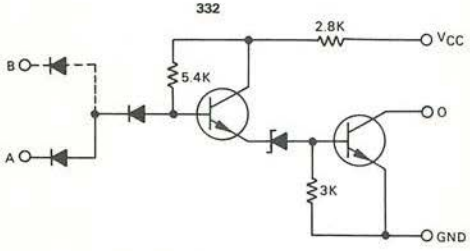


$O = \overline{AB}$

PINS	FUNCTION	LOADING
A,B	Inputs	1 UL
X	Expanders	*
O	Outputs	5 UL at V_{OL1}

* Each diode tied to X_1 or X_2 is 1 unit load

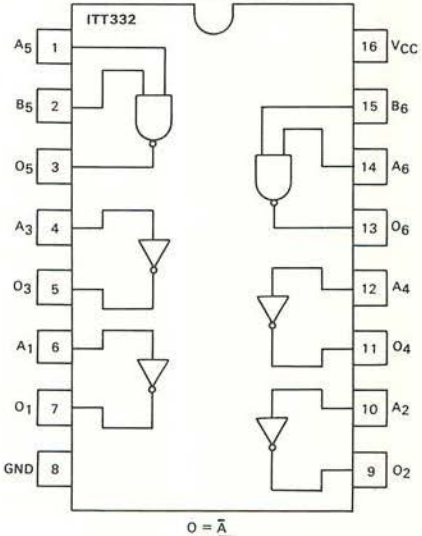
SCHEMATIC



PINS	FUNCTION	LOADING
A,B	Inputs	1 UL
O	Outputs	5 UL at V_{OL1} 7 UL at V_{OL1}

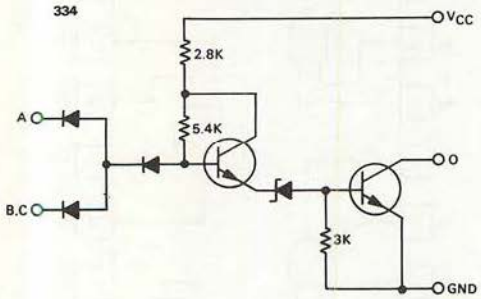
Either device handles 7 unit loads with correct external pullup resistor.

PIN CONFIGURATION

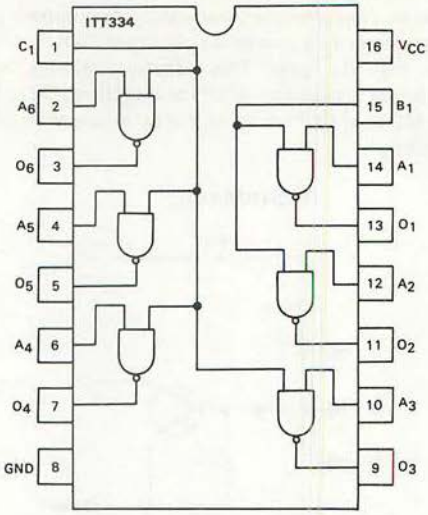


$O = \overline{A}$
$O = \overline{AB}$

SCHEMATIC



PIN CONFIGURATION

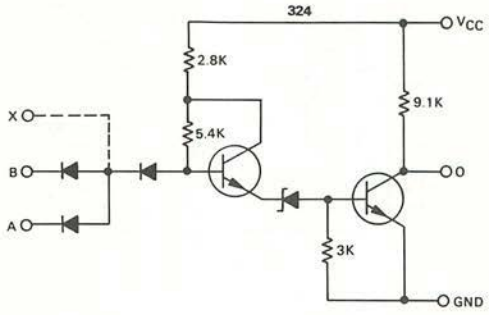


PINS	FUNCTION	LOADING
A	Data inputs	1 UL
B	Strobe input	2 UL
C	Strobe input	4 UL
O	Outputs	5 UL at V_{OL1} 7 UL at V_{OL2}

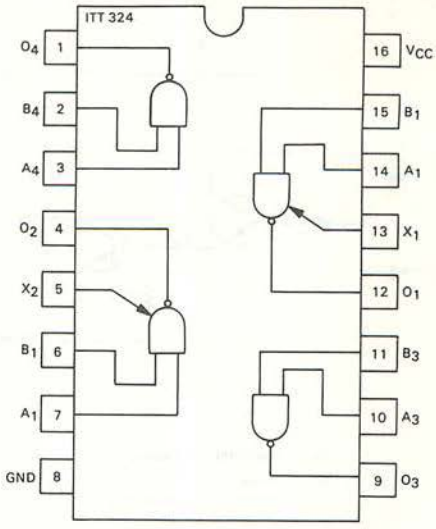
Either device handles 7 unit loads if correct external resistor is used

The ITT 324, 326, 333, and 335 employ 9.1K passive pull-up resistors on the chip. Passive pull-up has as its main advantage the wire-or capability, so these gates find wide application in internal logic systems.

SCHEMATIC



PIN CONFIGURATION



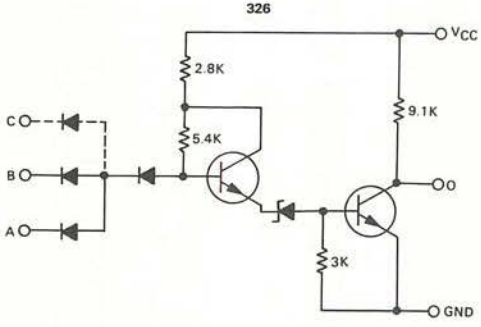
$O = \overline{AB}$

PINS	FUNCTION	LOADING
A,B	Inputs	1 UL
X	Expanders	*
O	Outputs	5 UL at V_{OL1} 7 UL V_{OL1}

* Each diode tied to X_1 or X_2 is 1 unit load

324 handles 7 unit loads with external pullup resistor.

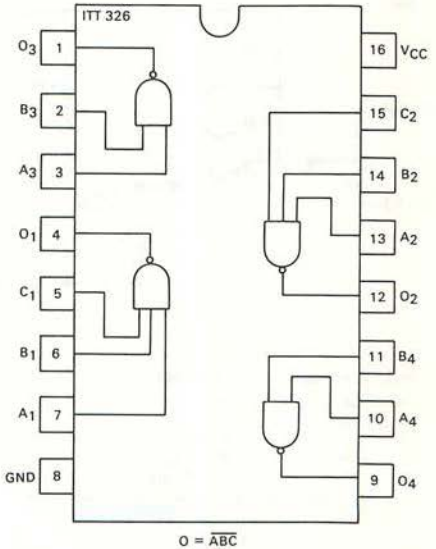
SCHEMATIC



PINS	FUNCTION	LOADING
A-C	Inputs	1 UL
O	Outputs	5 UL at V_{OL1} 7 UL at V_{OL1}

326 handles 7 unit loads with external pullup resistor.

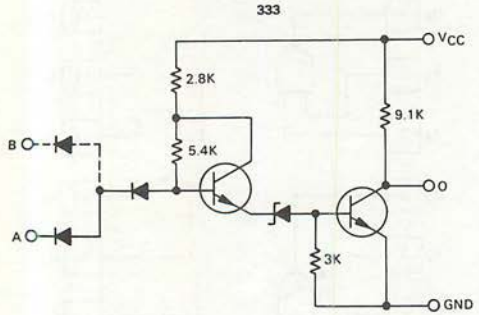
PIN CONFIGURATION



$O = \overline{ABC}$
$O = \overline{AB}$

ITT333 – QUAD INVERTER, DUAL 2-INPUT NAND GATE
ITT335 – STROBED HEX INVERTER

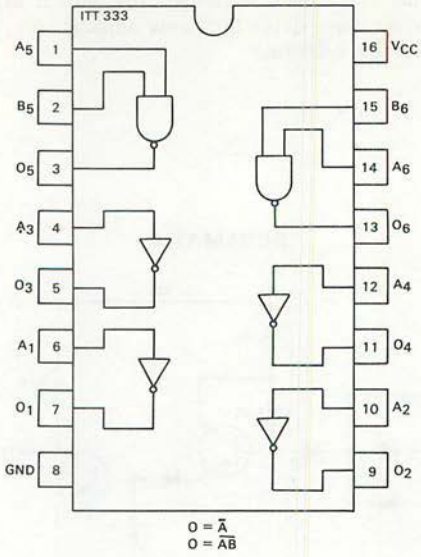
SCHEMATIC



PINS	FUNCTION	LOADING
A,B	Inputs	1 UL
O	Outputs	5 UL at V_{OL1} 7 UL at V_{OL1}

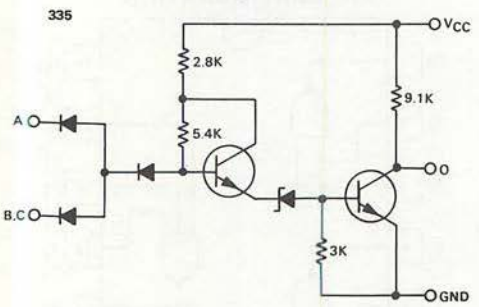
Device handles 7 unit loads if correct external resistor is used.

PIN CONFIGURATION



$O = \bar{A}$
$O = \overline{AB}$

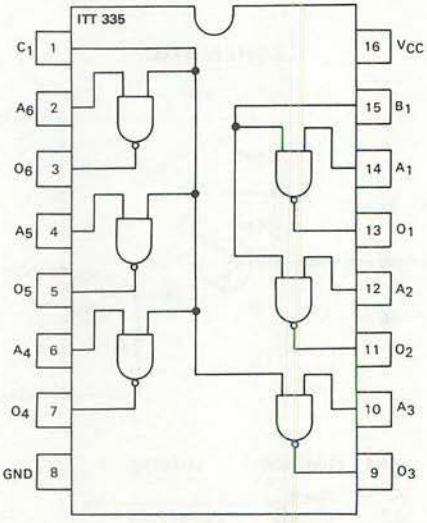
SCHEMATIC



PINS	FUNCTION	LOADING
A	Data inputs	1 UL*
B	Strobe input	2 UL
C	Strobe input	4 UL
O	Outputs	5 UL at V_{OL1} 7 UL at V_{OL2}

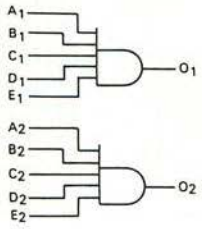
Device handles 7 unit loads if correct external resistor is used.

PIN CONFIGURATION

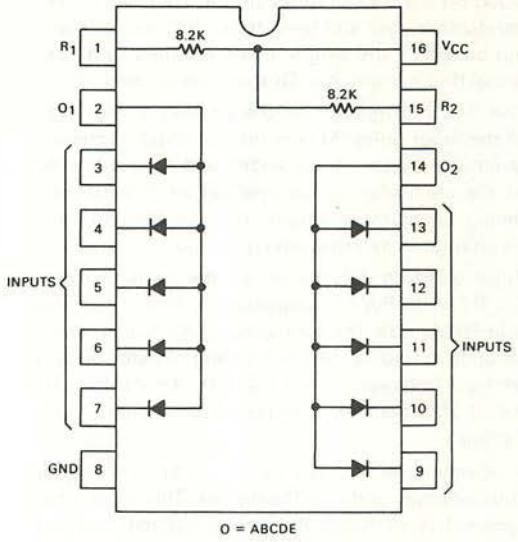


The ITT 331 consists of two arrays of HLL input diodes which are used on the expander inputs of HLL devices. Two 8.2.K nominal resistors are also available on the chip, allowing the 331 to be used as a second level dual 5-input AND gate.

LOGIC DIAGRAM



PIN CONFIGURATION



PINS	FUNCTION	LOADING
A-E	Inputs	1 UL
O	Outputs	

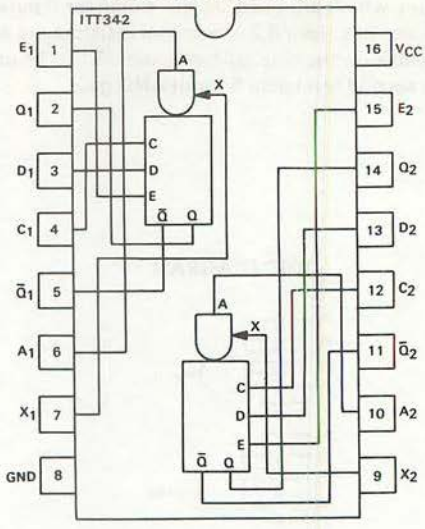
Two completely independent one-shots are provided on the 342 chip. Each one shot has an expandable trigger and provides complimentary output pulses of any length, as determined by an external timing capacitor. Outputs are active-high.

The 342 is triggered on the positive going edge of the input pulse. Maximum operating frequency is limited by the pulse width and recovery time of the particular circuit application. An external timing capacitor is required in conjunction with an internal or external timing resistor.

Pulse width is determined by the formula PW~ 0.7 RC, with PW in Nanoseconds, R in ohms, and C in Picofarads. The timing capacitor C has no restriction on value, but the timing resistor should be held between 2 and 62 KΩ. An internal 20 Km ±25% resistor is provided for normal applications.

Recovery time is given by $T_R = 3C$ with T_R in Nanoseconds and C in Picofarads. This is the time required to recharge the timing capacitor to the proper voltage.

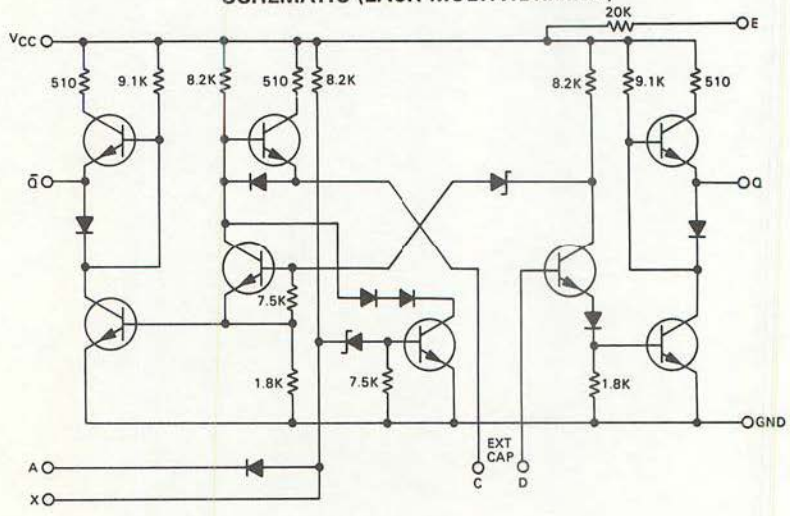
PIN CONFIGURATION



PINS	FUNCTION	LOADING
A	Trigger inputs	1 UL
C-E	Timing network	N.A.
X	Expanders	
Q,Q̄	Outputs	5 UL at V_{OL1}

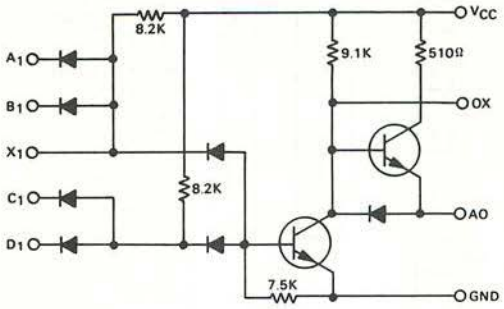
* Each diode tied to X_1 or X_2 is 1 unit load.

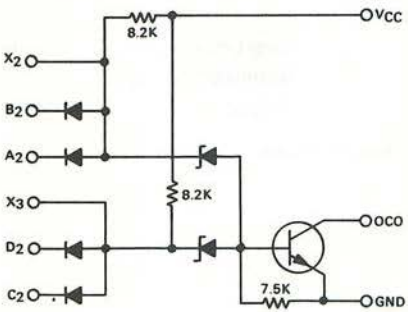
SCHEMATIC (EACH MULTIVIBRATOR)



The ITT 344 is an extremely versatile gate. The output expander allows the device to be wired-or with other passive pullup or open-collector devices, and still retain the desirable characteristics of an active-pullup output.

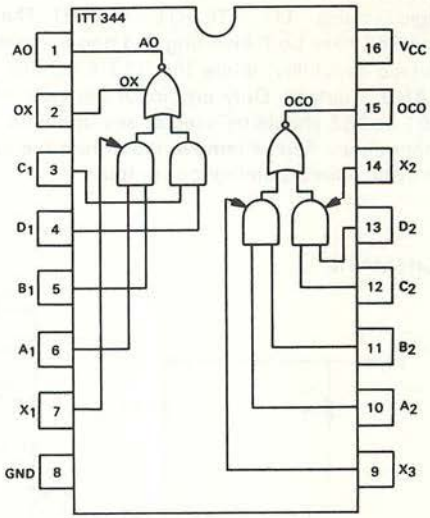
SCHEMATIC





V_{CC} and ground are shown separated in the schematic for clarity. The device has common V_{CC} and ground pins.

PIN CONFIGURATION

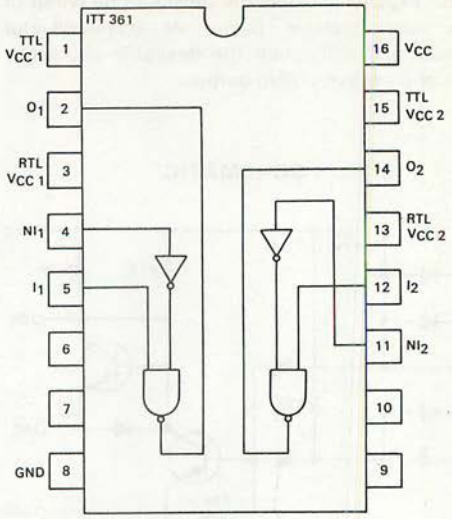


O = AB AND CD

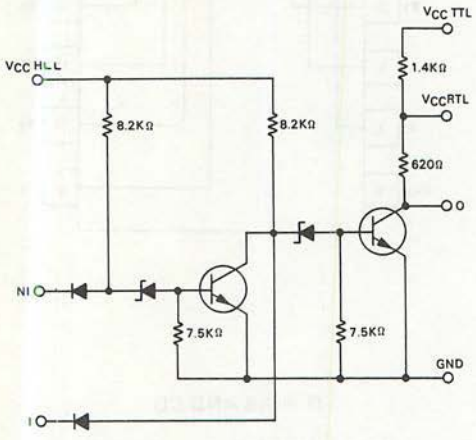
PINS	FUNCTIONS	LOADING
A-D	Inputs	1 UL
AO	Active output	5 UL at V_{OL1}
OX	Output expander	5 UL at V_{OL1}
OCO	Open collector	N.A. 5 UL at V_{OL1} 7 UL at V_{OL2}

The ITT 361, 362 and 363 are designed to directly interface HLL with other, low threshold logic families - TTL, DTL, RTL and DCTL. The 361 and 362 have both inverting and non-inverting interface capability, while the 363 functions as a NAND interface. Only one input per gate of the 361 or 362 should be used at any one time, with other inputs tied to remove them from the circuit to avoid possible ambiguous outputs.

PIN CONFIGURATION



SCHEMATIC



PINS	FUNCTION	LOADING
I	Inverting input	1 UL
NI	Noninverting input	1 UL
O	Output	*

*See specifications

361 INTERFACE SPECIFICATIONS

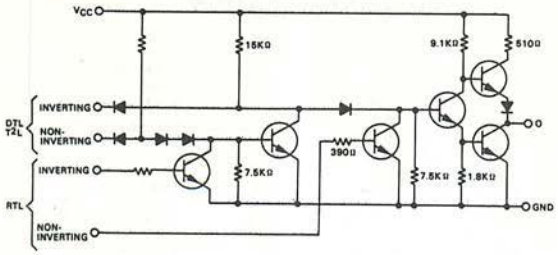
Outputs connected for TTL, over applicable temperature range

V_{OL} = 0.4V at I_{OL} = 6.4 mA, V_{CC} = 5.5V
V_{OH} = 2.4V at I_{OH} = −160 va, V_{CC} = 4.5V

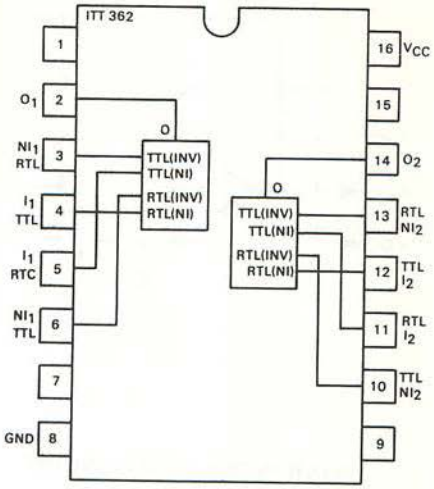
Outputs connected for RTL — V_{CC} = 3.0V

	Full Temp Range			Limited Temp Range		
Temp °C	−55	+25	+125	−30	+25	+85
V_{OL} @ 6 mA	0.33V	0.3V	0.35V	0.33V	0.3V	0.35V
H_{OH}	1.01V	0.85V	0.675V	0.9	0.85	0.76
I_{OH}	−2.5 mA	−2.5 mA	−2.3 mA	−2.3 mA	−2.2 mA	−2.0 mA

SCHEMATIC



PIN CONFIGURATION



362 INTERFACE SPECIFICATIONS

Inputs connected for TTL, over applicable temp range

I_R = 10Ua
$-I_F$ = −1.6 mA
V_{IH} = 2.0V
V_R = 4.0V
V_F = 0.4V
V_{IL} = 0.8V

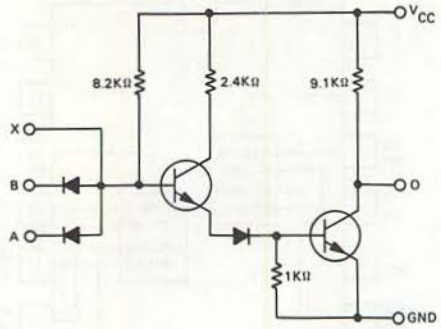
PINS	FUNCTIONS	LOADING
O	Output	5 UL*
Inputs	See schematic	See specs

*Fanout is 5 HLL unit loads at V_{OH} = 8.5V and V_{CC} = 11.0V, or at V_{OH} = 11.5V and V_{CC} = 14.0V.

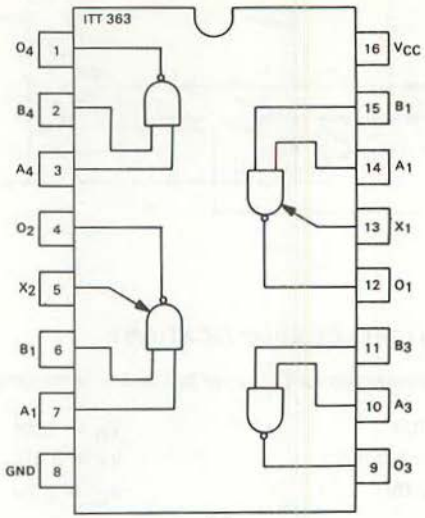
Inputs connected for RTL

	°C Full Temp Range			°C Limited Temp Range		
	−55	+25	+125	−30°	+25°	+85°
I_R(Ua)	495	440	470	460	440	470
V_R	1.01V	0.85V	0.675V	0.95	0.85	0.70
V_F	0.71	0.5	0.32	0.6	0.5	0.38
$-I_F$	−1.0Ua	−1.0Va	−10.0Ua	−1.0Ua	−1.0Va	−10.0Ua

SCHEMATIC



PIN CONFIGURATION



INTERFACE SPECIFICATIONS

$I_R = 10\ U_a$	$V_R = 4.0V$	$V_{CC} = 13V$ OR $16V$
$-I_F = 2.4mA$	$V_F = 0.4V$	$V_{CC} = 13V$
$-I_F = 3.0mA$	$V_F = 0.4V$	$V_{CC} = 16V$
$V_{IL} = 0.8V$	$V_{IH} = 2.0V$	

features active outputs.

PINS	FUNCTIONS	LOADING
A,B	TTL inputs	1 TTL load
X	Expanders	*
O	Outputs	5 UL at V_{OL1} 20 UL at V_{OL1}

*TTL expander input loading applies

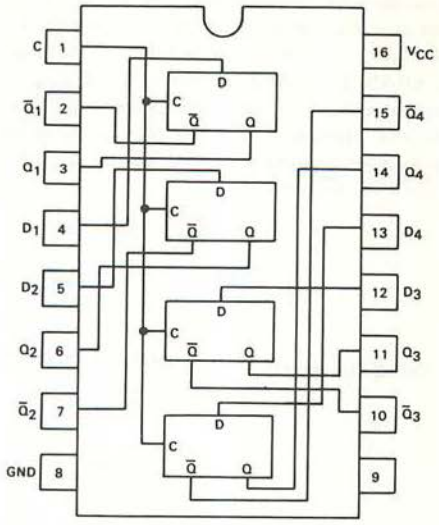
Four D-type flip-flops utilizing a common clock line make up the 370. Each flip-flop has complimentary passive pull up outputs with a single D input. This circuit is ideal as a quad latch for temporary storage of 4-bit binary numbers.

Data is transferred from D inputs to outputs when the clock line is low. With the clock line high, output data is held and D inputs are ignored.

TRUTH TABLE

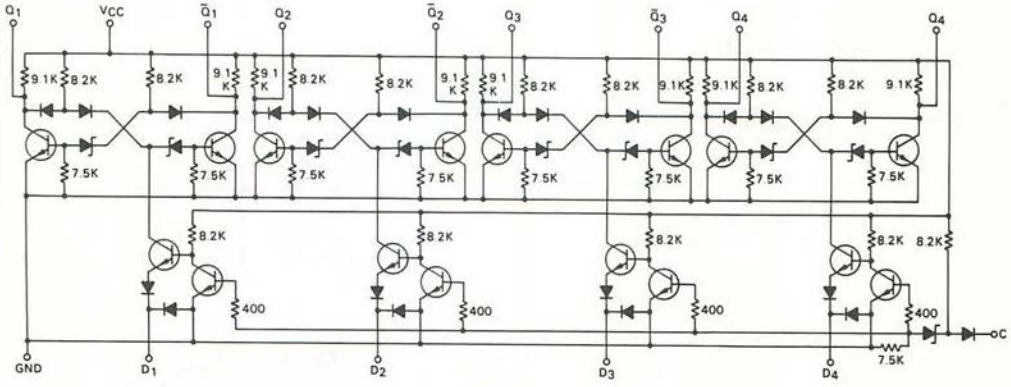
C	D	Q^{n+1}
1	1	Q^n
1	0	Q^n
0	1	1
0	0	0

PIN CONFIGURATION



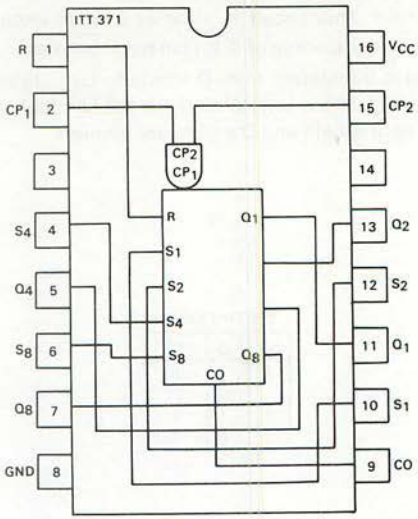
PINS	FUNCTION	LOADING
D	Data inputs	2 UL
C	Clock input	1 UL
Q,$\bar{Q}$	Outputs	5 UL at V_{OL1}

SCHEMATIC



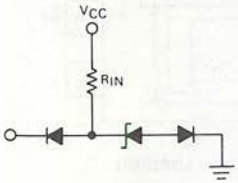
The ITT 371 HLL MS1 counter generates BCD on its outputs. It has direct set inputs for each of its four internal flip-flops and a common reset. Two clock inputs are provided, facilitating the input ENABLE function. A ninth count output is provided as a carry output for cascading 371's so a decimal number of any size may be generated. The passive outputs are ideal inputs to the 380 Series BCD decoders.

PIN CONFIGURATION

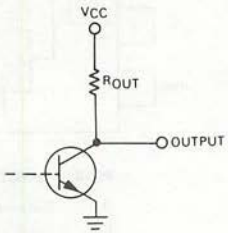


PINS	FUNCTION	LOADING
CP	Clock inputs	2 UL
R	Direct reset input	1 UL
S	Direct set input	1/2 UL
CO	Carry output	2 UL
Q	Outputs	5 UL at V_{OL1}

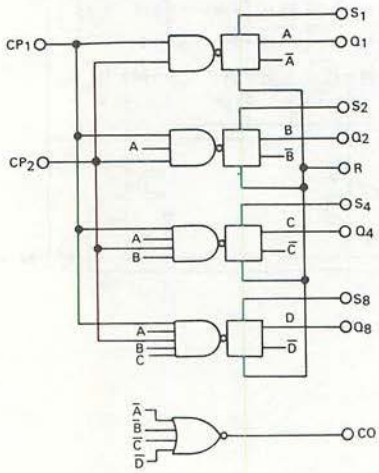
TYPICAL INPUT



TYPICAL OUTPUT



LOGIC DIAGRAM



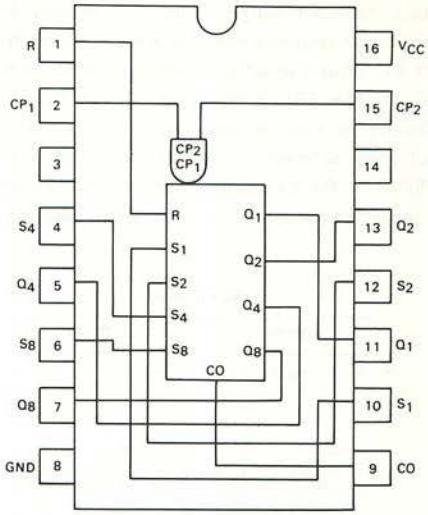
INPUT	R_{IN}
CP_1 CP_2	5 KΩ TYP.
RESET	5 KΩ TYP.
ALL SETS	20 KΩ TYP.

OUTPUT	R_{OUT}
Q_1 Q_2	9.1 KΩ TYP.
$Q_3 + Q_4$ CO	9.1 KΩ TYP.

The ITT 372 is identical to the ITT 371 except its outputs are coded in the standard 4-bit binary (1-2-4-8) code.
Operation of the 372 is identical to that of the 371. Internal construction produces divide-by-sixteen operation.

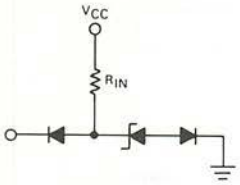
The 371 is level sensitive, counting as the clock goes low. Holding either clock low will inhibit the count sequence. Direct set or reset is accomplished by switching the desired input high. All unused direct set and reset inputs must be grounded.

PIN CONFIGURATION

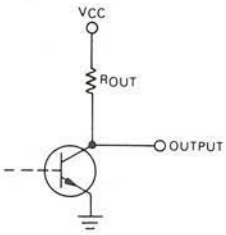


PINS	FUNCTION	LOADING
CP	Clock inputs	2 UL
R	Direct reset input	1 UL
S	Direct set input	1/2 UL
CO	Carry output	2 UL
Q	Outputs	5 UL at V_{OL1}

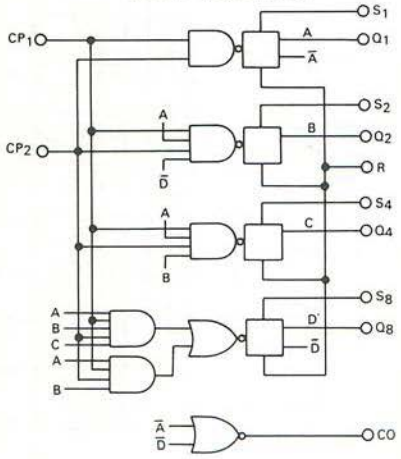
TYPICAL INPUT



TYPICAL OUTPUT



LOGIC DIAGRAM



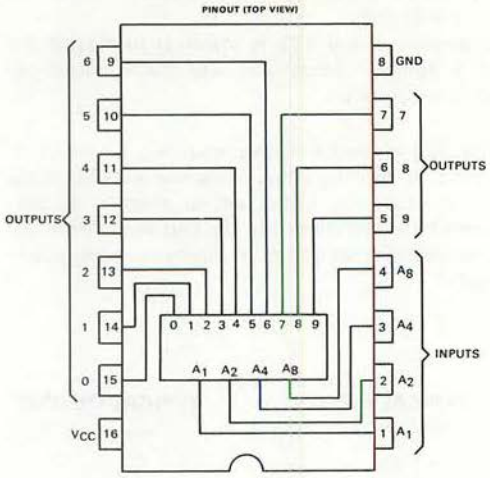
INPUT	R_{IN}
CP_1 CP_2	5 KΩ TYP.
RESET	5 KΩ TYP.
ALL SETS	20 KΩ TYP.

OUTPUT	R_{OUT}
Q_1 Q_2	9.1 KΩ TYP.
$Q_3 + Q_4$ CO	9.1 KΩ TYP.

ITT380, ITT381 — BCD TO DECIMAL DECODER

The 380 and 381 decode standard BCD (1-2-4-8) inputs to produce a low state on one of the ten open collector outputs. Internal design insures that no ambiguous outputs are produced, turning off all outputs when addressed by input codes for 10-15. The 380 is intended to drive small lamps directly or can be used with various interface buffering schemes. The 381 is identical to the 380 with the exception of its output ratings and is intended for use as an internal circuit element.

PIN CONFIGURATION



TRUTH TABLE

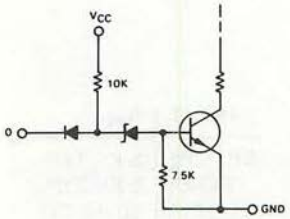
INPUTS				OUTPUTS								
A_1	A_2	A_4	A_8	0	1	2	3	4	5	6	7	8	9
0	0	0	0	0	1	1	1	1	1	1	1	1	1
1	0	0	0	1	0	1	1	1	1	1	1	1	1
0	1	0	0	1	1	0	1	1	1	1	1	1	1
1	1	0	0	1	1	1	0	1	1	1	1	1	1
0	0	1	0	1	1	1	1	0	1	1	1	1	1
1	0	1	0	1	1	1	1	1	0	1	1	1	1
0	1	1	0	1	1	1	1	1	1	0	1	1	1
1	1	1	0	1	1	1	1	1	1	1	0	1	1
0	0	0	1	1	1	1	1	1	1	1	1	0	1
1	0	0	1	1	1	1	1	1	1	1	1	1	0
0	1	0	1	1	1	1	1	1	1	1	1	1	1
1	1	0	1	1	1	1	1	1	1	1	1	1	1
0	0	1	1	1	1	1	1	1	1	1	1	1	1
1	0	1	1	1	1	1	1	1	1	1	1	1	1
0	1	1	1	1	1	1	1	1	1	1	1	1	1
1	1	1	1	1	1	1	1	1	1	1	1	1	1

Table on Page 54

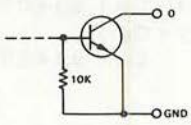
PINS	FUNCTION	LOADING
A	BCD inputs	1 UL
0-9	Outputs	

*Unit loading does not apply

TYPICAL INPUT



TYPICAL OUTPUT



LOGIC DIAGRAM